

MAS1016B

AM Receiver IC

- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**

DESCRIPTION

The MAS1016B AM Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in.

The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary. WWVB in USA and JJY in Japan require use of AGC control procedure, which is simplified in MAS1016B.

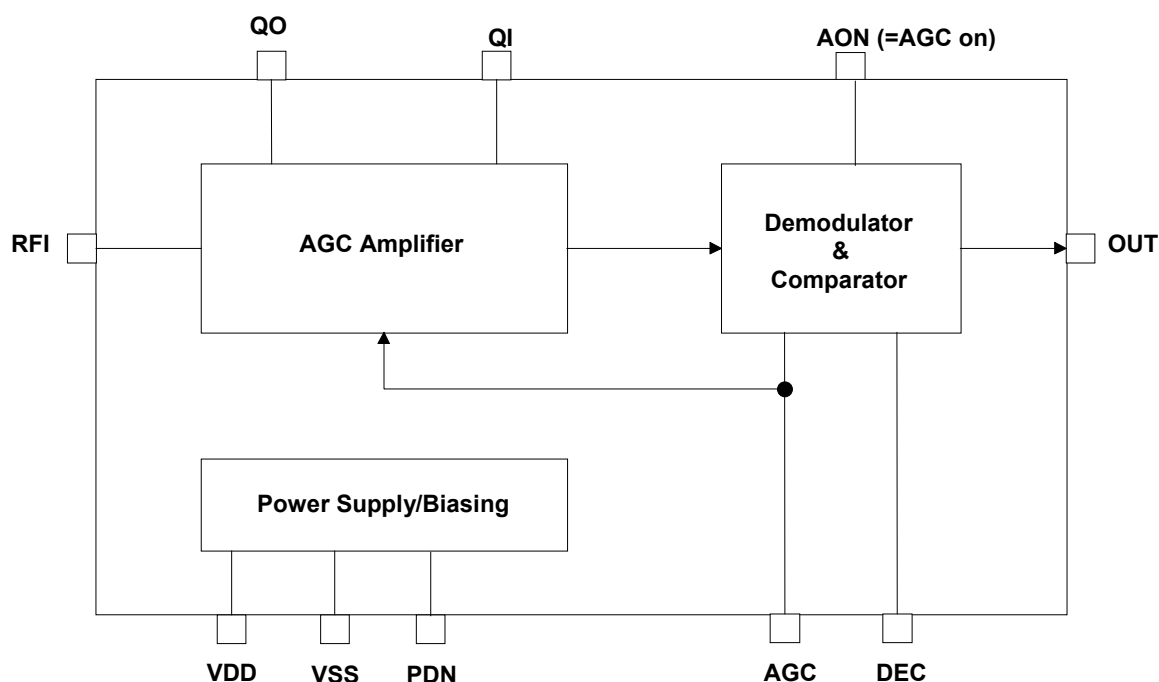
FEATURES

- Highly Sensitive AM Receiver, 0.5 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption 50 μA typ.
- Power Down Control
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Die and TSSOP-16 Package

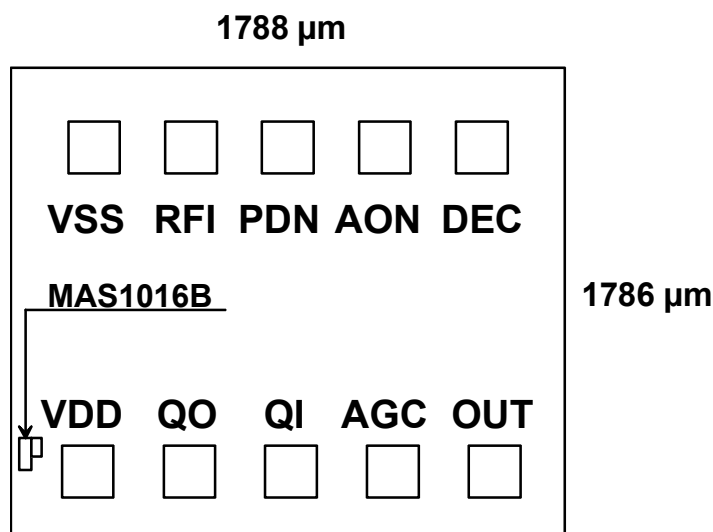
APPLICATIONS

- Time Signal Receiver Designed for MSF (UK), WWVB (USA), JJY (Japan) and DCF77 (Germany)
- Receiver for ASK Modulated Data Signals

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 1.79 x 1.79 mm; PAD size = 100 x 100 μm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in the center of VDD pad

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	0 μm	0 μm	
Quarz Filter Output	QO	306 μm	19 μm	
Quarz Filter Input	QI	587 μm	19 μm	
AGC Capacitor	AGC	866 μm	19 μm	
Receiver Output	OUT	1143 μm	19 μm	1
Demodulator Capacitor	DEC	1111 μm	1436 μm	
AGC On Control	AON	868 μm	1436 μm	2
Power Down Input	PDN	551 μm	1436 μm	3
Receiver Input	RFI	309 μm	1436 μm	
Power Supply Ground	VSS	16 μm	1415 μm	

Notes:

- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
 - the output is a current source/sink with $|I_{\text{OUT}}| > 5 \mu\text{A}$
 - at power down the output is high impedance
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
 - Internal pull-up with current $< 1 \mu\text{A}$ which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off

ABSOLUTE MAXIMUM RATINGS

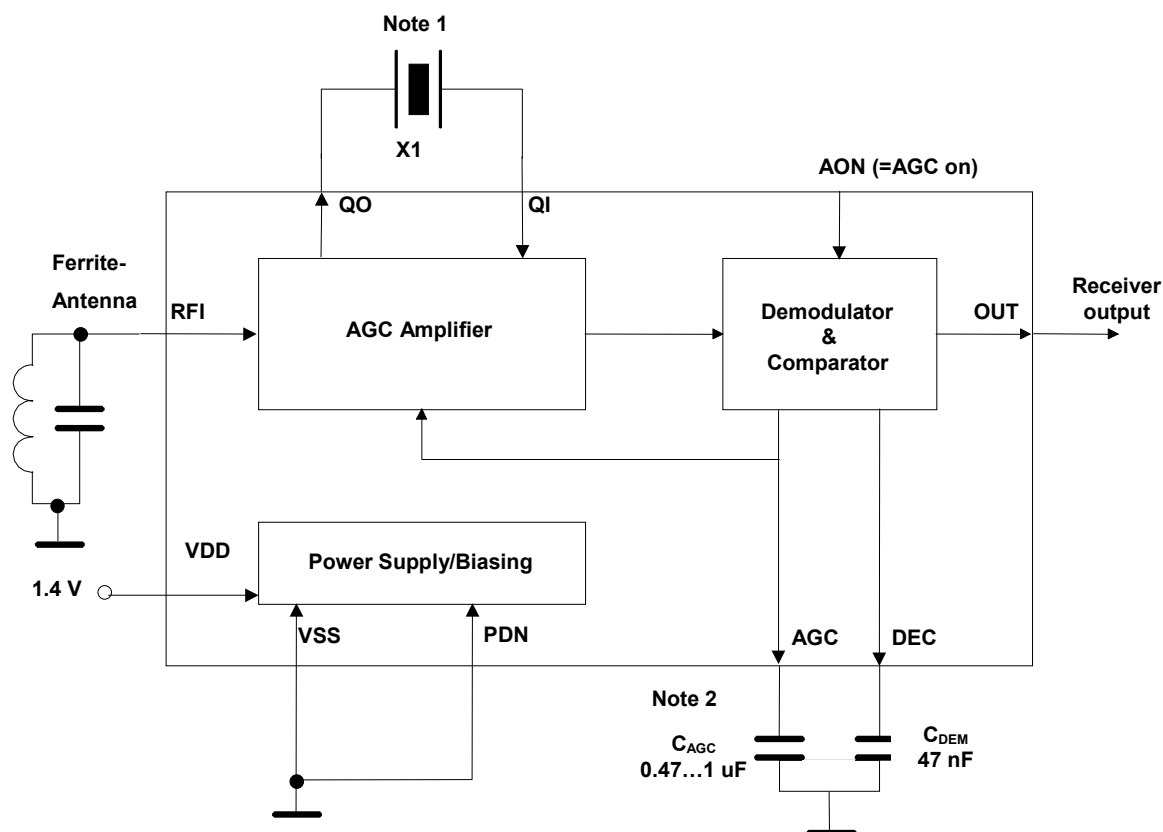
Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	$V_{DD}-V_{SS}$		-0.3	5.0	V
Input Voltage	V_{IN}		$V_{SS}-0.3$	$V_{DD}+0.3$	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-20	70	°C
Storage Temperature	T_{ST}		-40	120	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: $V_{DD} = 1.4V$, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		3.60	V
Current Consumption	I_{DD}			50	100	μA
Stand-By Current	I_{DDoff}				0.1	μA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.5	1	μVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Input Levels $ I_{IN} < 0.5\ \mu A$	V_{IL} V_{IH}		$0.8\ V_{DD}$		$0.2\ V_{DD}$	V
Output Current $V_{OL} < 0.2\ V_{DD}; V_{OH} > 0.8\ V_{DD}$	$ I_{OUT} $		5			μA
Output Pulse	T_0	$1\ \mu Vrms \leq V_{IN} \leq 20\ mVrms$	50		140	ms
	T_1	$1\ \mu Vrms \leq V_{IN} \leq 20\ mVrms$	150		230	ms
Startup Time	T_{Start}			8		s
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION



Note 1: Crystal

The crystal as well as ferrite antenna frequencies are chosen according to the time signal system. Ferrite antenna frequencies and recommended crystal frequencies are presented in table 1. For more details about crystal selection see DAEV1016B.

Table 1 Time-Signal System Frequencies

Time-Signal System	Location	Frequency	Recommended Crystal Frequency	Unit
DCF77	Germany	77.5	77.503	kHz
MSF	United Kingdom	60	60.003	kHz
WWVB	USA	60	60.003	kHz
JJY	Japan	40 and 60	40.003 and 60.003	kHz

Note 2: AGC Capacitor

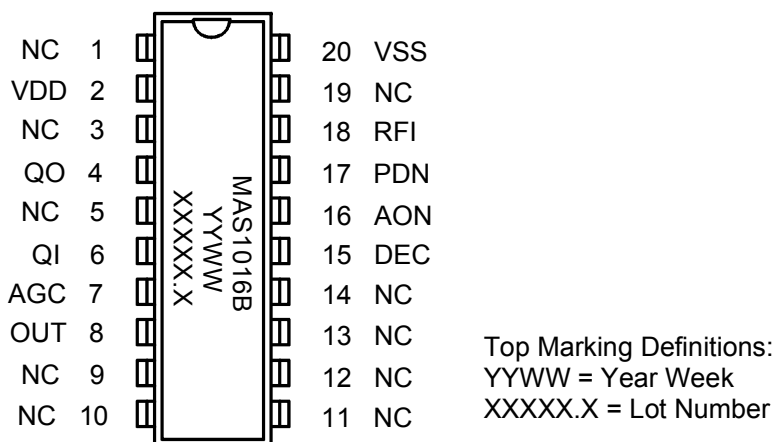
The AGC capacitor value is also chosen according to time-signal system. Recommended capacitor values are presented in table 2. WWVB and JJY systems require external control of AON (=AGC on) pin to receive pulses correctly. For more details about required control of AON in WWVB and JJY systems see DAEV1016B.

The AGC and DEC capacitors should have low leakage currents due to very small 40 nA signal currents through the capacitors. The insulation resistance of these capacitors should be higher than 70 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins.

Table 2 Recommended AGC Capacitor Value

Time-Signal System	Recommended AGC Capacitor Value
DCF77	470nF
MSF	1uF
WWVB	220nF + Special AGC Control
JJY	220nF + Special AGC Control

SAMPLES IN SBDIL 20 PACKAGE



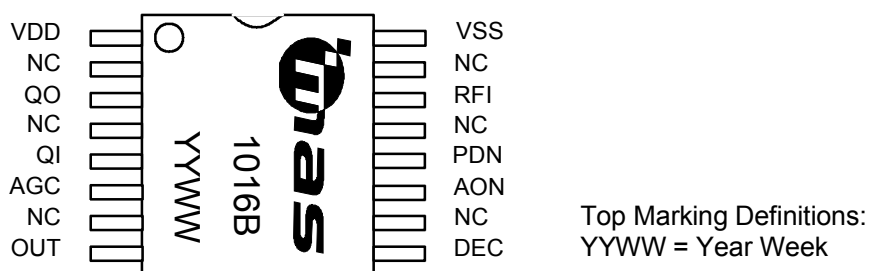
PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
NC	3			
QO	4	AO	Quartz Filter Output	
NC	5			1
QI	6	AI	Quartz Filter Input	
AGC	7	AO	AGC Capacitor	
OUT	8	DO	Receiver Output	2
NC	9			
NC	10			
NC	11			
NC	12			
NC	13			
NC	14			
DEC	15	AO	Demodulator Capacitor	
AON	16	DI	AGC On Control	3
PDN	17	AI	Power Down Input	4
RFI	18	AI	Receiver Input	
NC	19			
VSS	20	G	Power Supply Ground	

Notes:

- Pin 5 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
 - the output is a current source/sink with $|I_{OUT}| > 5 \mu A$
 - at power down the output is high impedance
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
 - Internal pull-up (to AGC on) with current $< 1 \mu A$ which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off

PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



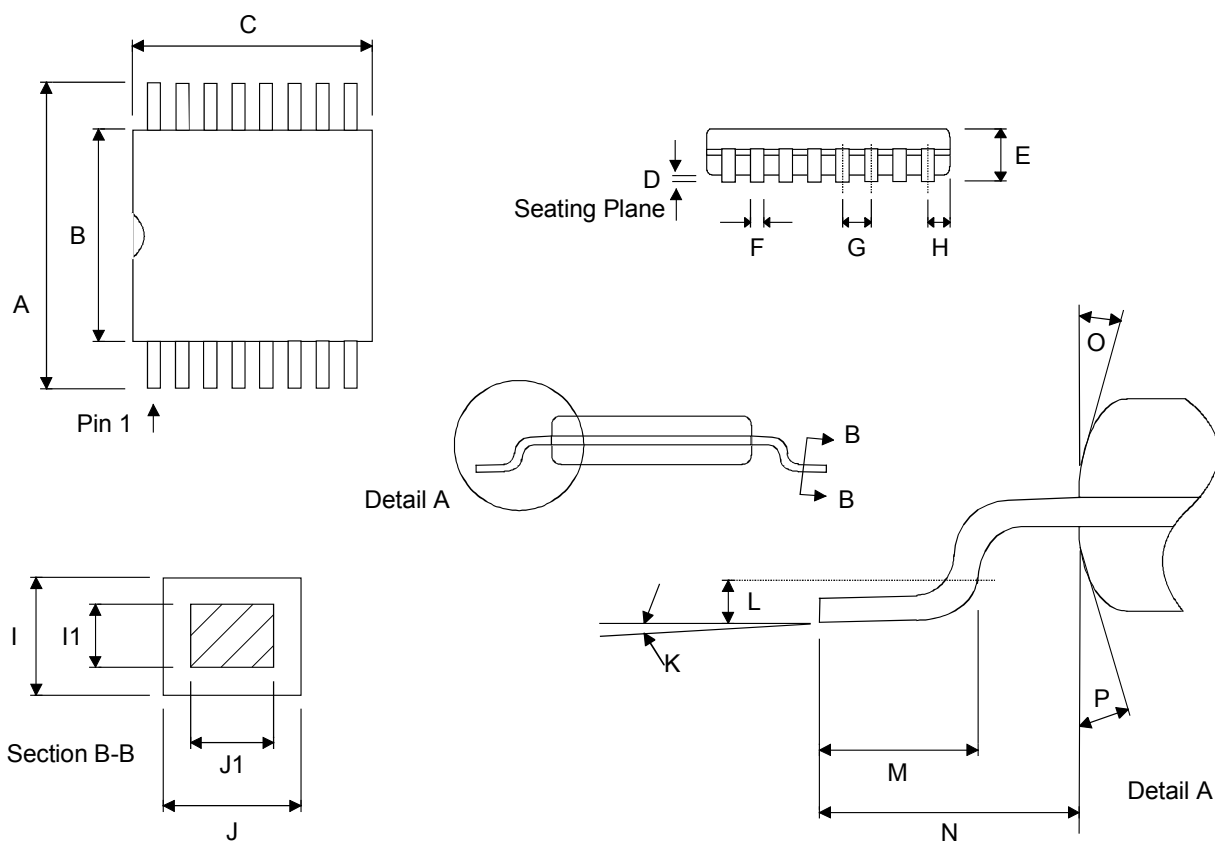
PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
NC	2			
QO	3	AO	Quartz Filter Output	
NC	4			1
QI	5	AI	Quartz Filter Input	
AGC	6	AO	AGC Capacitor	
NC	7			
OUT	8	DO	Receiver Output	2
DEC	9	AO	Demodulator Capacitor	
NC	10			
AON	11	DI	AGC On Control	3
PDN	12	AI	Power Down Input	4
NC	13			
RFI	14	AI	Receiver Input	
NC	15			
VSS	16	G	Power Supply Ground	

Notes:

- Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
 - the output is a current source/sink with $|I_{OUT}| > 5 \mu A$
 - at power down the output is high impedance
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
 - Internal pull-up (to AGC on) with current $< 1 \mu A$ which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off

PACKAGE (TSSOP16) OUTLINES



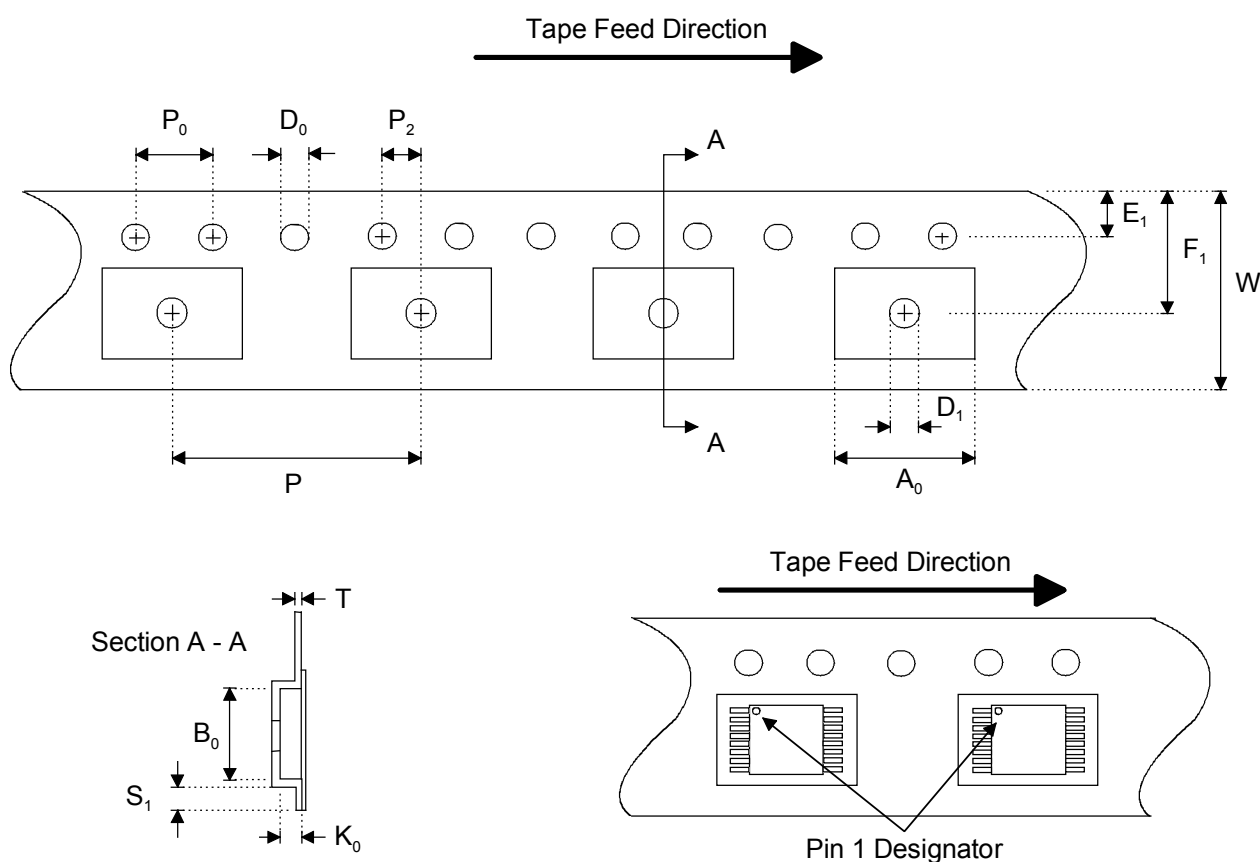
Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

SOLDERING INFORMATION

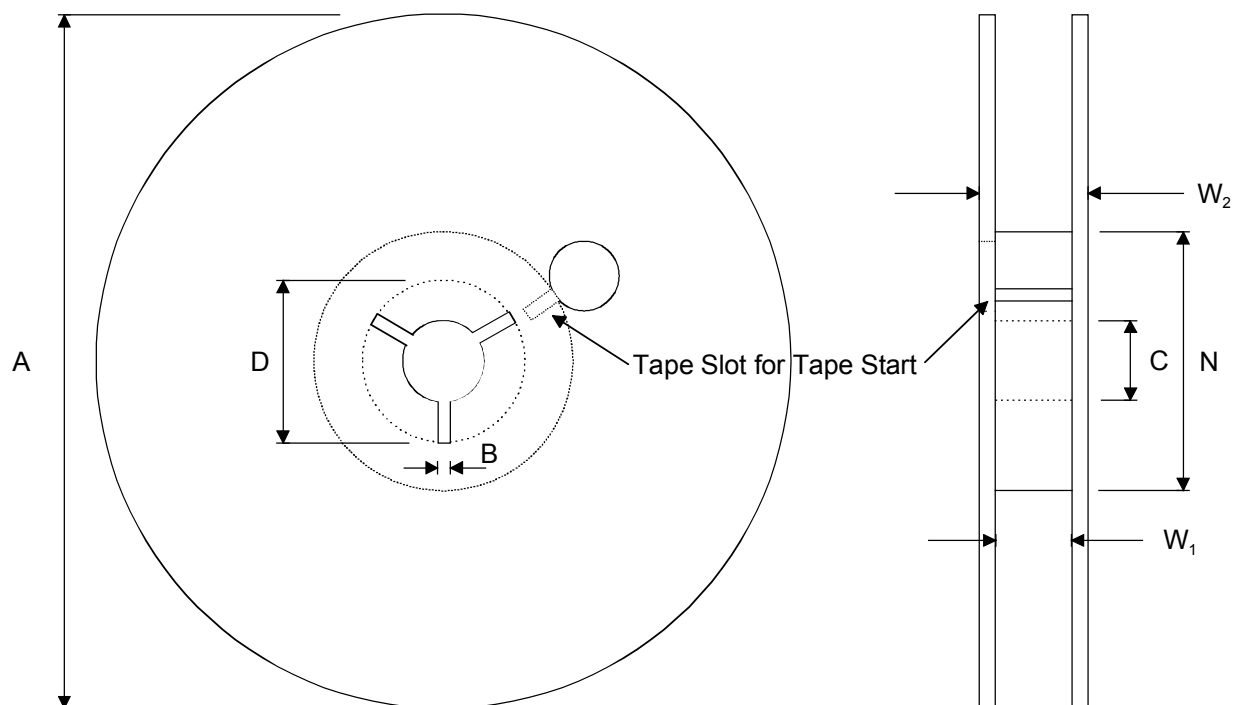
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

EMBOSSED TAPE SPECIFICATIONS



Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

REEL SPECIFICATIONS

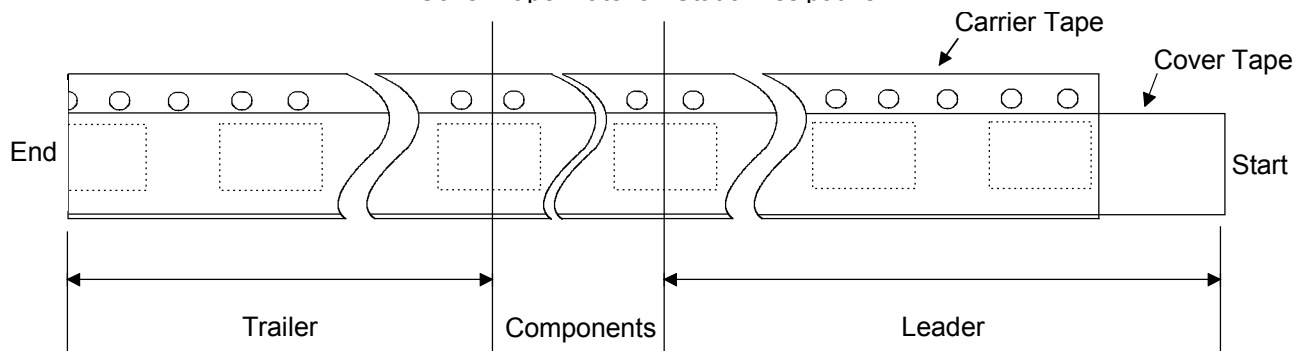


2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative

Carrier Tape Material: Conductive

Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W ₁ (measured at hub)	12.4	14.4	mm
W ₂ (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS1016BTB1	MAS1016B AM Receiver IC	Wafer, EWS tested	Thickness 480 µm
MAS1016BTC1	MAS1016B AM Receiver IC	Wafer, EWS tested	Thickness 400 µm
MAS1016BUA1-T	MAS1016B AM Receiver IC	TSSOP-16	Tape & Reel

Please contact Micro Analog Systems Oy for other wafer thickness options.

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