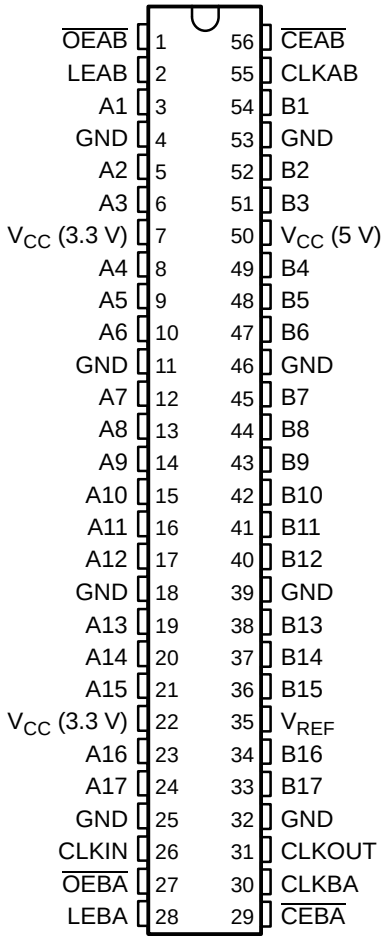
SN74GTL16616
17-BIT LVTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS

SCBS481H – JUNE 1994 – REVISED APRIL 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **GTL Buffered CLKAB Signal (CLKOUT)**
- **Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Supports Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **Equivalent to '16601 Function**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**

DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL16616 is a 17-bit UBT™ transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. Combined D-type flip-flops and D-type latches allow for transparent, latched, clocked, and clocked-enabled modes of data transfer identical to the '16601 function. Additionally, this device provides for a copy of CLKAB at GTL/GTL+ signal levels (CLKOUT) and conversion of a GTL/GTL+ clock to LVTTL logic levels (CLKIN). This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTL16616DL	GTL16616
		Tape and reel	SN74GTL16616DLR	GTL16616
	TSSOP – DGG	Tape and reel	SN74GTL16616DGGR	GTL16616

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus, UBT, OEC are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1994–2005, Texas Instruments Incorporated

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port. V_{CC} (5 V) supplies the internal and GTL circuitry, while V_{CC} (3.3 V) supplies the LVTTL output buffers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

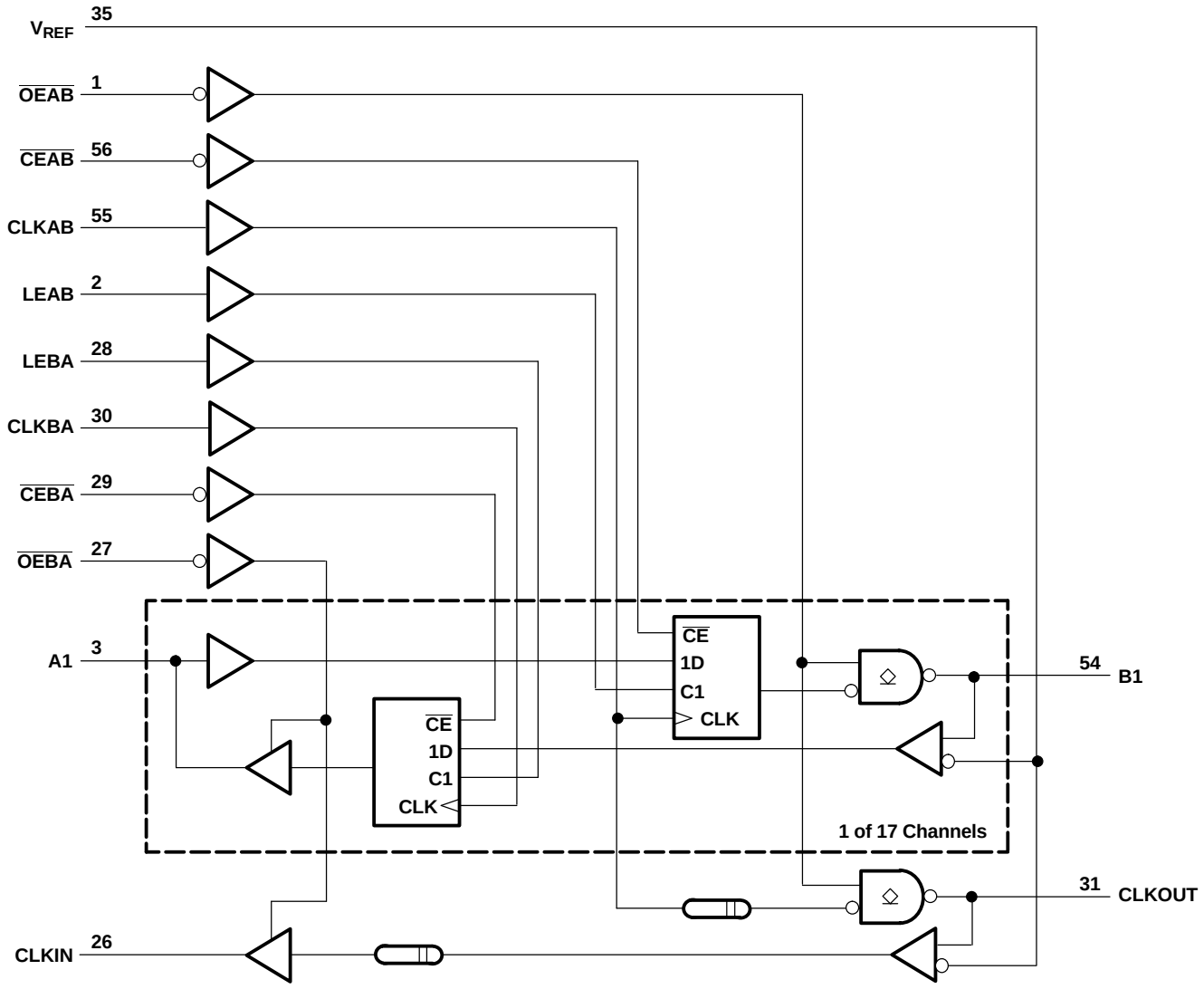
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE(1)

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0(2)	Latched storage of A data
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

(1) A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.
(2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	3.3 V	–0.5	4.6	V
		5 V	–0.5	7	
V_I	Input voltage range[2]	A-port and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state[2]	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		128	mA
		B port		80	
I_O	Current into any A-port output in the high state[3]			64	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance[4]	DGG package		64	°C/W
		DL package		56	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1][2][3][4]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–32	mA
I_{OL}	Low-level output current	A port			64	mA
		B port			40	
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V,		I_{OH} = –100 μA	V_{CC} – 0.2			V
		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			
				I_{OH} = –32 mA	2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OL} = 100 μA			0.2	V
				I_{OL} = 16 mA			0.4	
				I_{OL} = 32 mA			0.5	
				I_{OL} = 64 mA			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_{OL} = 40 mA			0.4	
I_I	Control inputs	V_{CC} = 0 or 3.45 V,	V_{CC} (5 V) = 0 or 5.25 V,	V_I = 5.5 V			10	μA
	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20	
				V_I = V_{CC} (3.3 V)			1	
				V_I = 0			–30	
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5	
				V_I = 0			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				100	μA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			μA
				V_I = 2 V	–75			
				V_I = 0 to V_{CC} (3.3 V)(2)			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 3 V			1	μA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0.5 V			–1	μA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0.4 V			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND		Outputs high			1	mA
				Outputs low			5	
				Outputs disabled			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND		Outputs high			120	mA
				Outputs low			120	
				Outputs disabled			120	
ΔI_{CC}(3)		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A-port or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V					1	mA
C_i	Control inputs	V_I = 3.15 V or 0				3.5		pF
C_{io}	A port	V_O = 3.15 V or 0				12		pF
	B port	Per IEEE Std 1194.1					5	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.5		
t_{su}	Setup time	A before CLKAB↑	1.3		ns
		B before CLKBA↑	2.5		
		A before LEAB↓	0		
		B before LEBA↓	1.1		
		$\overline{CEAB}$ before CLKAB↑	2.2		
		$\overline{CEBA}$ before CLKBA↑	2.7		
t_h	Hold time	A after CLKAB↑	1.6		ns
		B after CLKBA↑	0.4		
		A after LEAB↓	4		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.1		
		$\overline{CEBA}$ after CLKBA↑	0.9		

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
f_{max}			95			MHz
t_{PLH}	A	B	1.7	3	4.4	ns
t_{PHL}			1.4	2.8	4.5	
t_{PLH}	LEAB	B	2.3	3.8	5.4	ns
t_{PHL}			2.2	3.7	5.3	
t_{PLH}	CLKAB	B	2.4	4	5.7	ns
t_{PHL}			2.1	3.7	5.4	
t_{PLH}	CLKAB	CLKOUT	4.7	6.1	8.1	ns
t_{PHL}			5.7	7.9	11.3	
t_{PHL}	$\overline{OEAB}$	B or CLKOUT	2.1	3.6	5.1	ns
t_{PLH}			2.1	3.8	5.6	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.2		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.7		ns
t_{PLH}	B	A	1.7	4	6.7	ns
t_{PHL}			1.4	2.9	4.7	
t_{PLH}	LEBA	A	2.4	3.8	5.8	ns
t_{PHL}			2	3	4.6	
t_{PLH}	CLKBA	A	2.6	4	6	ns
t_{PHL}			2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.4	10	14.4	ns
t_{PHL}			6.1	8.1	11.7	
t_{en}	$\overline{OEBA}$	A or CLKIN	2.8	5.3	7.8	ns
t_{dis}			2.7	4.3	6.4	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.5		
t_{su}	Setup time	A before CLKAB↑	1.3		ns
		B before CLKBA↑	2.3		
		A before LEAB↓	0		
		B before LEBA↓	1.3		
		$\overline{CEAB}$ before CLKAB↑	2.2		
		$\overline{CEBA}$ before CLKBA↑	2.7		
t_h	Hold time	A after CLKAB↑	1.6		ns
		B after CLKBA↑	0.6		
		A after LEAB↓	4		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.1		
		$\overline{CEBA}$ after CLKBA↑	0.9		

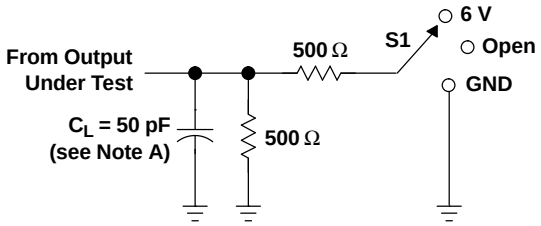
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

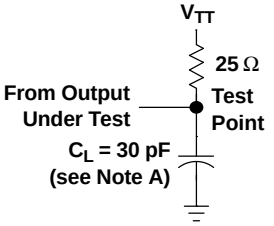
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
f_{max}			95			MHz
t_{PLH}	A	B	1.7	3	4.4	ns
t_{PHL}			1.4	2.9	4.6	
t_{PLH}	LEAB	B	2.3	3.8	5.4	ns
t_{PHL}			2.2	3.7	5.4	
t_{PLH}	CLKAB	B	2.4	4	5.7	ns
t_{PHL}			2.1	3.8	5.5	
t_{PLH}	CLKAB	CLKOUT	4.7	6.1	8.1	ns
t_{PHL}			5.7	8	11.4	
t_{PLH}	$\overline{OEAB}$	B or CLKOUT	2.1	3.6	5.1	ns
t_{PHL}			2.1	3.8	5.7	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.4		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			1		ns
t_{PLH}	B	A	1.6	3.9	6.6	ns
t_{PHL}			1.3	2.8	4.5	
t_{PLH}	LEBA	A	2.4	3.8	5.8	ns
t_{PHL}			2	3	4.6	
t_{PLH}	CLKBA	A	2.6	4	6	ns
t_{PHL}			2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.3	9.9	14.3	ns
t_{PHL}			6	8	11.5	
t_{en}	$\overline{OEBA}$	A or CLKIN	2.8	5.3	7.8	ns
t_{dis}			2.7	4.3	6.4	

(1) All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+

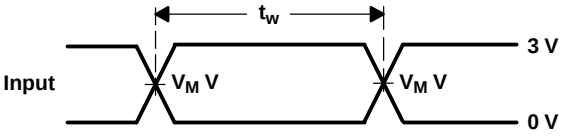


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

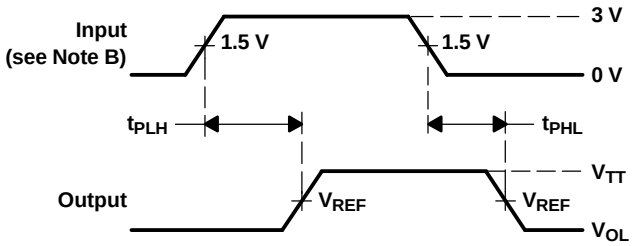


LOAD CIRCUIT FOR A OUTPUTS

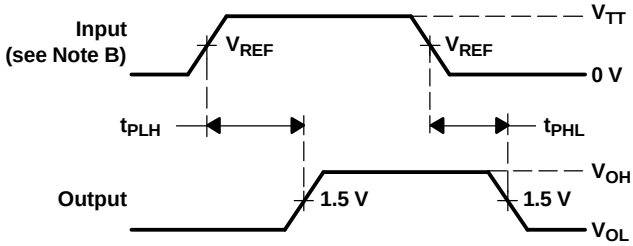
LOAD CIRCUIT FOR B OUTPUTS



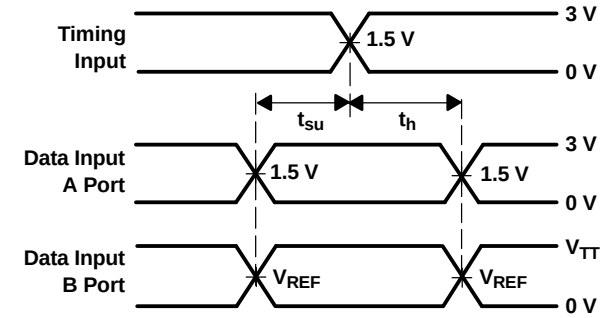
VOLTAGE WAVEFORMS
PULSE DURATION
(V_M = 1.5 V for A port and V_{REF} for B port)†



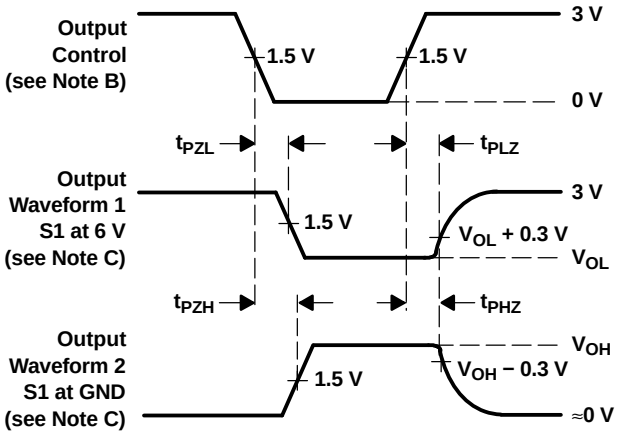
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port and CLKIN)

† All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74GTL16616DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL16616DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL16616DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL16616DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL16616DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL16616DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

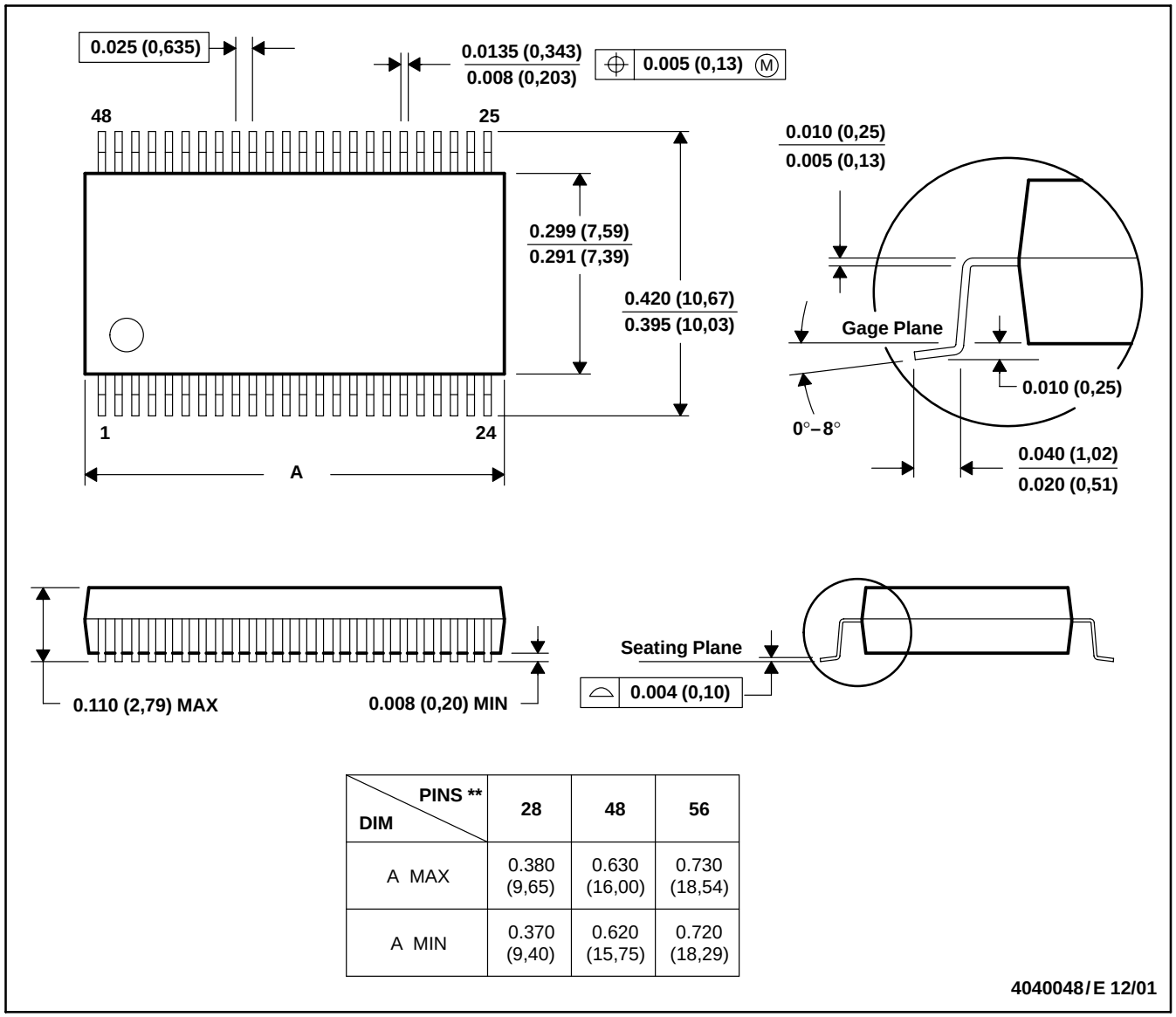
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



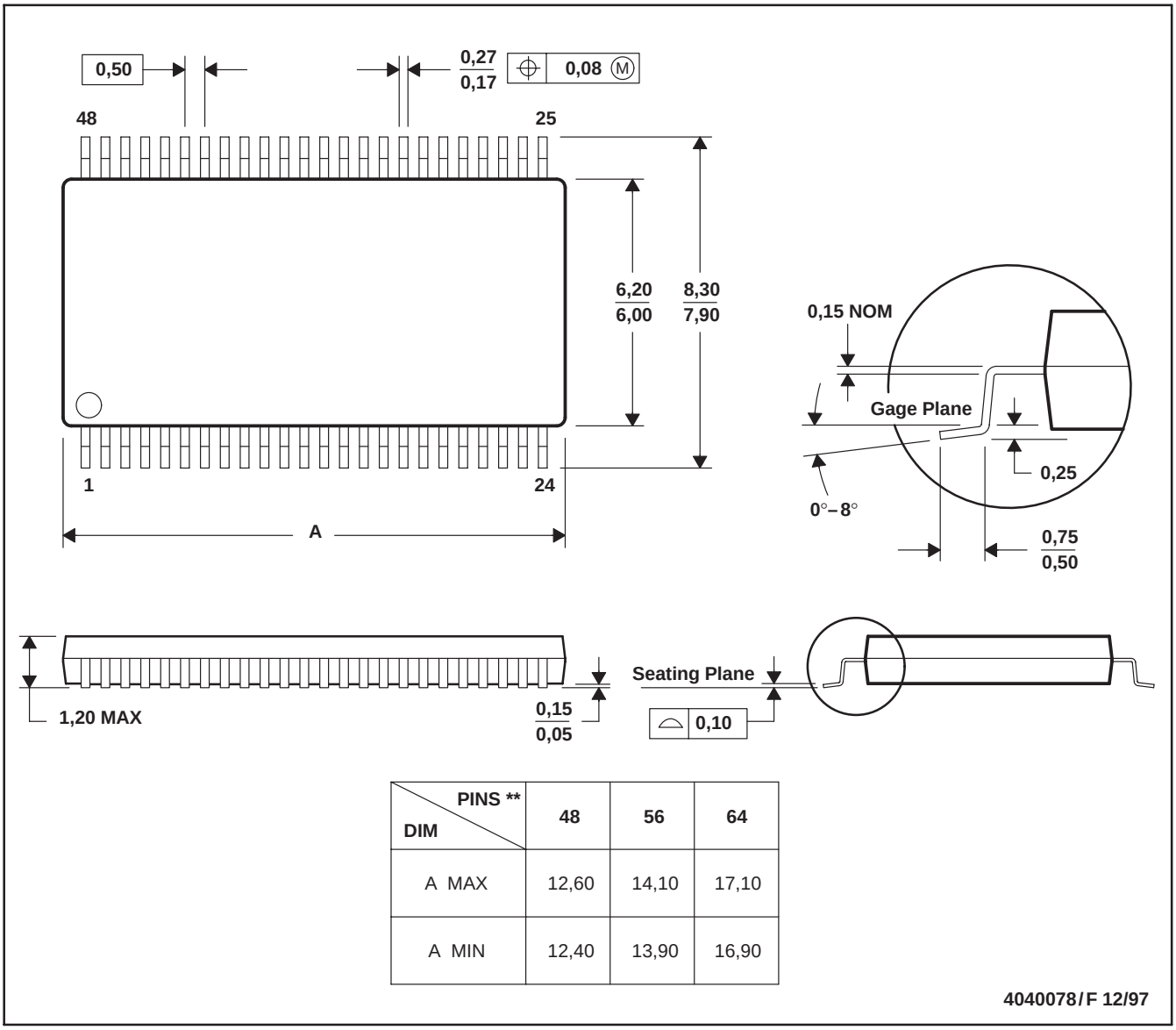
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated