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ISL89367

High Speed, Dual Channel, 6A, MOSFET Driver With Programmable Rising and Falling Edge Delay Timers

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The ISL89367 is a high-speed, 6A, 2 channel MOSFET driver optimized for synchronous rectifier applications. Internal timers can be programmed with resistors to delay the rising and/or falling edges of the outputs. Logically ANDed dual inputs are also provided. One input is for the PWM signal and the second can be used as an enable. A third control input is used to optionally invert the logical polarity of the driver outputs.

Comparator like logical inputs allows this driver to be configured for any logic level from 3.3V to 10 VDC. The precision logic thresholds provided by the comparators allow the use of external RC circuits to generate longer time delays than are possible with the internal timers. The comparators also allow the driver to be configured with a low output voltage that is negative relative to the logic ground if desired. This is useful for applications that require a negative turn-off gate drive voltage for driving FETs with logic thresholds.

At high switching frequencies, these MOSFET drivers use very little bias current. Separate, non-overlapping drive circuits are used to drive each CMOS output FET to prevent shoot-thru currents in the output stage.

The start-up sequence is design to prevent unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor between the output and ground helps to keep the output voltage low. When ~1V < V_{DD} < UV, both outputs are driven low with very low resistance and the logic inputs are ignored. This insures that the driven FETs are off. When V_{DD} > UVLO, and after a short delay, the outputs now respond to the logic inputs.

Features

- 2 outputs with 6A peak drive currents (sink and source) with output voltage range of 4.5V to 16V
- Typical ON-resistance <1Ω
- Specified Miller plateau drive currents
- EPAD provides very low thermal impedance (θ_{JC} = 3°C/W)
- Dual logic inputs with hysteresis for high noise immunity
- Rising and/or falling output edge delays programmed with resistors
- 20ns rise and fall time driving a 10nF load
- Flexible logic options available by use of INVA and INVB pins

Applications

- Synchronous Rectifier (SR) Driver
- Switch mode power supplies
- Motor Drives, Class D amplifiers, UPS, Inverters
- Pulse Transformer Driver
- Clock/Line Driver

Related Literature

- AN1603 “ISL6752/54EVAL1Z ZVS DC/DC Power Supply with Synchronous Rectifiers User Guide”

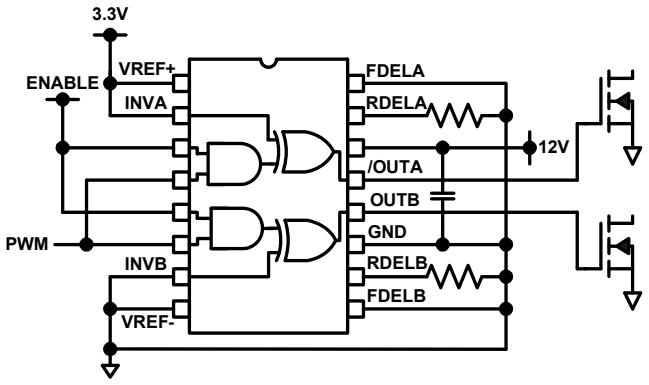


FIGURE 1. TYPICAL APPLICATION

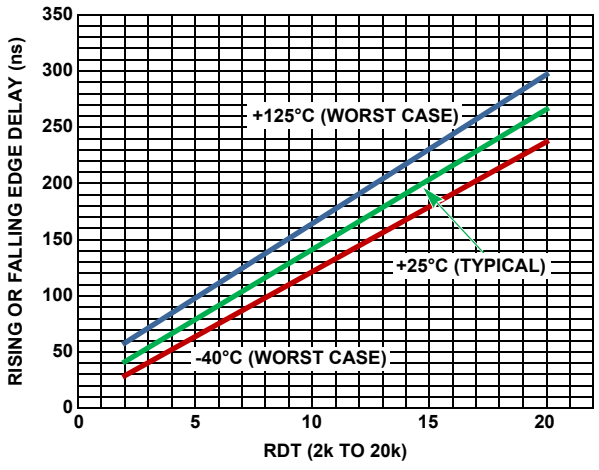
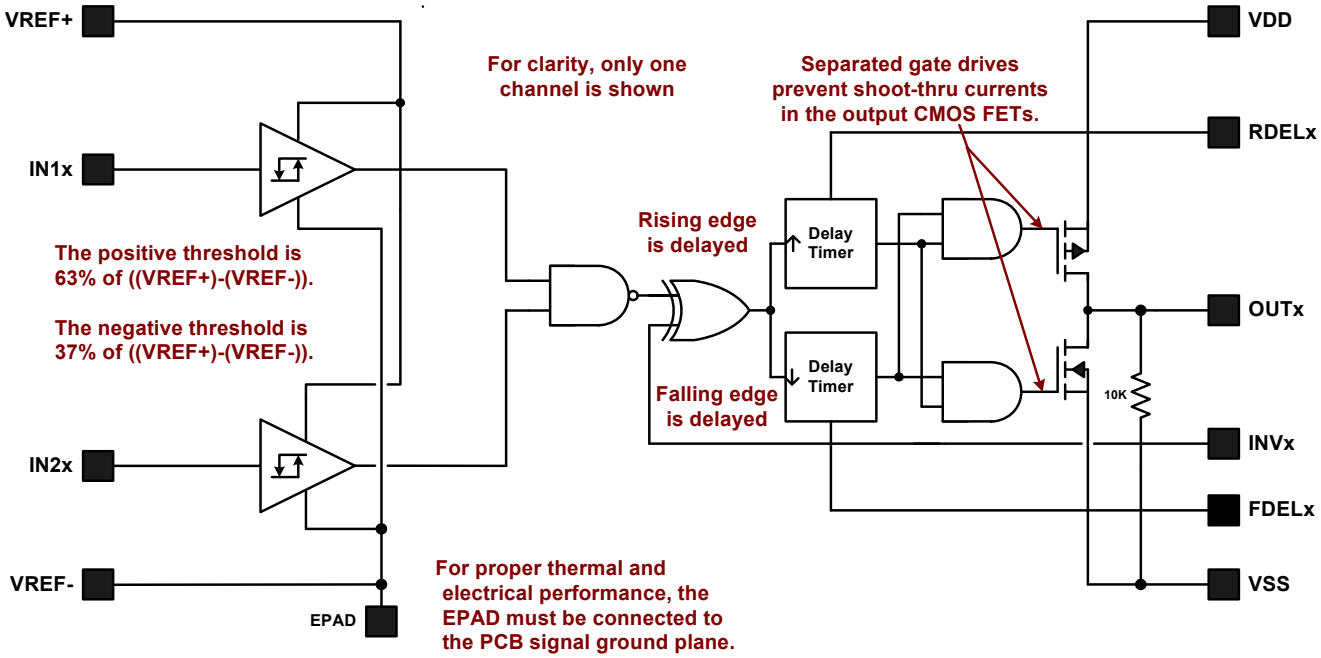


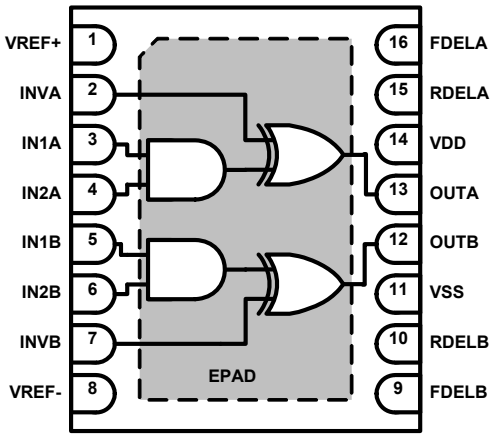
FIGURE 2. PROGRAMMABLE TIME DELAYS

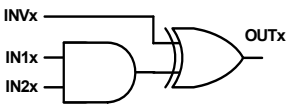
Block Diagram



Pin Configurations

ISL89367
(16 LD TDFN, EPSOIC)
TOP VIEW





TRUTH TABLE

INVx	IN1x	IN2x	OUTx
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 8	VREF+ VREF-	VREF+ and VREF- are the reference voltages for the IN1A, IN1B, IN2A, and IN2B logic inputs. VREF+ is normally connected to the positive bias voltage of the input logic. VREF- is normally connected to the ground reference of the input logic.
2, 7	INVA or INVB	Connect these pins to VDD to invert the corresponding output. Connect to VSS to not invert the corresponding output.
3, 4, 5, 6	IN1A, IN2A, IN1B, IN2B	ANDed logical inputs. One input to each channel can be used as an enable. Logic high threshold is 63% of [(VREF+) - (VREF-)]. Logic low threshold is 37% of [(VREF+) - (VREF-)].
9, 16	FDELB, FDELA	Connect a resistor between these pins and VSS to program the duration of the falling edge propagation delay of the corresponding output relative to the logic inputs.
10, 15	RDELB, RDELA	Connect a resistor between these pins and VSS to program the duration of the rising edge propagation delay of the corresponding output relative to the logic inputs.
11, 14	VSS, VDD	Output bias voltage. (VDD to VSS) range is 4.5V to 16V. VSS may be negative relative to VREF-.
12, 13	OUTB, OUTA	6A peak outputs. Output voltage swing is between VDD and VSS.
	EPAD	Must be connected to logic ground (VREF-).

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	INPUT CONFIGURATION	PACKAGE (Pb-Free)	PKG. DWG. #
ISL89367FRTAZ	9367A	-40 to +125	Non-inverting	16 Ld 3x5 TDFN	L16.5x3

NOTES:

1. Add “-T”, suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL89367. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

Supply Voltage, V_{DD} Relative to V_{SS} ..... -0.3V to 18V
V_{REF+} Relative to V_{DD} ..... -0.3V to V_{DD} + 0.3V
V_{REF-} Relative to V_{SS} ..... +4.0V to V_{SS} - 0.3V
INVx (Note 4) ..... V_{SS} - 0.3V to V_{DD} + 0.3V
INnx (Note 5) Relative to V_{REF-} ..... (V_{REF-}) - 0.3V to (V_{REF+}) + 0.3V
V_{REF+} Relative to V_{SS} ..... -0.3V to 18V
V_{REF+} Relative to V_{REF-} ..... -0.3V to 18V
Average Output Current (Note 8) 150mA
ESD Ratings
Human Body Model Class 2 (Tested per JESD22-A114E) 2000V
Machine Model Class B (Tested per JESD22-A115-A) 200V
Charged Device Model Class IV 1000V
Latch-Up
(Tested per JESD-78B; Class 2, Level A)
Output Current 500mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TDFN Package (Notes 6, 7)	36	3

Max Power Dissipation at +25°C in Free Air 2.8W
Max Power Dissipation at +25°C with Copper Plane 33.3W
Storage Temperature Range ..... -65°C to +150°C
Operating Junction Temp Range ..... -40°C to +125°C

Maximum Recommended Operating Conditions

Junction Temperature ..... -40°C to +125°C
Supply Voltage, V_{DD} Relative to V_{SS} ..... 0V to 16V
V_{REF-} Relative to V_{SS} ..... +4.0V to V_{SS}
INVx (Note 4) ..... V_{SS} or V_{DD}
INnx (Note 5) Relative to V_{REF-} ..... V_{REF-} to V_{REF+}
V_{REF+} Relative to V_{SS}, ... 3.0V to 10V
V_{REF+} Relative to V_{REF-}, ... 3.0V to 10V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Substitute INVA or INVB for INVx.
5. Substitute IN1A, IN2A, IN1B, or IN2B for INnx
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
8. The average output current, when driving a power MOSFET or similar capacitive load, is the average of the **rectified** output current (sinking and sourcing). The peak output currents of this driver are self limiting by transconductance or $r_{DS(ON)}$ and do not required any external components to minimize the peaks. If the output is driving a non-capacitive load, such as an LED, maximum output current must be limited by external means to less than the specified absolute average output current.

DC Electrical Specifications

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, RDELA = RDELB = FDELA = FDELB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
POWER SUPPLY								
Voltage Range (V_{DD} relative to V_{SS})	V_{DD}		-	-	-	**4.5**	**16**	V
V_{DD} Quiescent Current	I_{DD}	INx = GND	-	5	-	-	-	mA
		INA = INB = 1MHz, square wave	-	25		-	-	mA
V_{REF+} AND V_{REF-} BIAS								
V_{REF+} Relative to V_{SS}	V_{P-S}		3	-	10	**3**	**10**	V
V_{REF-} Relative to V_{SS}	V_{N-S}		0	-	4	**0**	**4**	V
V_{REF+} Relative to V_{REF-}	V_{P-N}		3	-	10	**3**	**10**	V
V_{REF+} Quiescent Current	I_{PP}	V_{P-N} = 12V	-	200	-	**100**	**300**	µA
UNDERVOLTAGE								
VDD Undervoltage Lock-out (Note 11)	V_{UV}	INnx = True (Note 12)	-	3.3	-	-	-	V
Hysteresis			-	~25	-	-	-	mV

DC Electrical Specifications

V_{DD} = 12V, GND = 0V, No load on OUTA or OUTB, RDELA = RDELB = FDELA = FDELB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
INPUTS								
Input Range for IN1A, IN2A, IN1B, IN2B	V_{IN}	V_{IN} is referenced to V_{REF-}	-	-	-	**Vref-**	**Vref+**	V
Input Range for INVA, INVB	V_{INV}	V_{INV} is referenced to V_{SS}	-	-	-	**V_{SS}**	**V_{DD}**	V
Logic 0 Threshold for IN1A, IN2A, IN1B, IN2B	V_{IL}	Nominally 37% x ((V_{REF+}) - (V_{REF-}))	-	37	-	**34**	**40**	%
Logic 1 Threshold for IN1A, IN2A, IN1B, IN2B	V_{IH}	Nominally 63% x ((V_{REF+}) - (V_{REF-}))	-	63	-	**60**	**66**	%
Logic 0 Threshold for INVA, INVB	V_{ILV}	V_{ILV} is referenced to V_{SS}	-	0.9	-	**1**	**1.2**	V
Logic 1 Threshold for INVA, INVB	V_{IHV}	V_{IHV} is referenced to V_{SS}	-	1.5	-	**1.5**	**1.7**	V
Input Capacitance of IN1A, IN2A, IN1B, 1N2B, INVA, INVB	C_{IN}		-	2	-	-	-	pF
Input Bias Current for IN1A, IN2A, IN1B, IN2B	I_{IN}	$V_{REF-} < V_{IN} < V_{REF+}$	-	-	-	**-10**	**+10**	µA
Input Bias Current for INVA, INVB	I_{INV}	$V_{SS} < V_{INV} < V_{DD}$	-	-	-	**-40**	**+40**	µA
OUTPUTS								
High Level Output Voltage	V_{OHA} V_{OHB}		-	-	-	**V_{DD} - 0.1**	**V_{DD}**	V
Low Level Output Voltage	V_{OLA} V_{OLB}		-	-	-	**GND**	**GND + 0.1**	V
Peak Output Source Current	I_O	V_O (initial) = 0V, C_{LOAD} = 10nF	-	-6	-	-	-	A
Peak Output Sink Current	I_O	V_O (initial) = 12V, C_{LOAD} = 10nF	-	+6	-	-	-	A

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. This parameter is taken from the simulation models for the input FET. The actual capacitance on this input will be dominated by the PCB parasitic capacitance.
11. A 400µs delay further inhibits the release of the output state when the UV positive going threshold is crossed. See Figure 9.
12. The true state of a specific part number is defined by the input logic symbol.

AC Electrical Specifications

V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, RDELA = RDELB = FDELA = FDELB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS /NOTES	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
Output Rise Time (see Figure 4)	t_R	C_{LOAD} = 10nF, 10% to 90%	-	20	-	-	**40**	ns
Output Fall Time (see Figure 4)	t_F	C_{LOAD} = 10nF, 90% to 10%	-	20	-	-	**40**	ns
Output Rising Edge Propagation Delay (see Figure 3)	t_{RDLYA}, t_{RDLYB}		-	25	-	-	**50**	ns

AC Electrical Specifications

V_{DD} = 12V, GND = 0V, No Load on OUTA or OUTB, RDELA = RDELB = FDELA = FDELB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS /NOTES	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
Output Falling Edge Propagation Delay (see Figure 3)	t_{FDLYA}, t_{FDLYB}		-	25	-	-	**50**	ns
Rising Propagation Matching (see Figure 3)	t_{RM}	RDELx = 0kΩ, FDELx = 0kΩ	-	<1	-	-	-	ns
Falling Propagation Matching (see Figure 3)	t_{FM}	RDELx = 0kΩ, FDELx = 0kΩ	-	<1	-	-	-	ns
Rising Edge Timer Delay (Note 13)	t_{RTDLY}	RDELx = 20kΩ, No load	-	270	-	**237**	**297**	ns
		RDELx = 2.0kΩ, No load	-	45	-	**29**	**58**	ns
Falling Edge Timer Delay (Note 13)	t_{TDLY}	FDELx = 20kΩ, No load	-	270	-	**237**	**297**	ns
		FDELx = 2.0kΩ, No load	-	45	-	**29**	**58**	ns
Miller Plateau Sink Current (See Test Circuit Figure 5)	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 5V	-	6	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER} = 3V	-	4.7	-	-	-	A
	$-I_{MP}$	V_{DD} = 10V, V_{MILLER}= 2V	-	3.7	-	-	-	A
Miller Plateau Source Current (See Test Circuit Figure 6)	I_{MP}	V_{DD} = 10V, V_{MILLER} = 5V	-	5.2	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 3V	-	5.8	-	-	-	A
	I_{MP}	V_{DD} = 10V, V_{MILLER} = 2V	-	6.9	-	-	-	A

NOTE:

13. Delays for timing resistors < 2.0kΩ or > 20kΩ are not specified and are not recommended. The resistors tolerances (including the boundary values of 2.0kΩ and 20.0kΩ) are recommended to be 1% or better.

Test Waveforms and Circuits

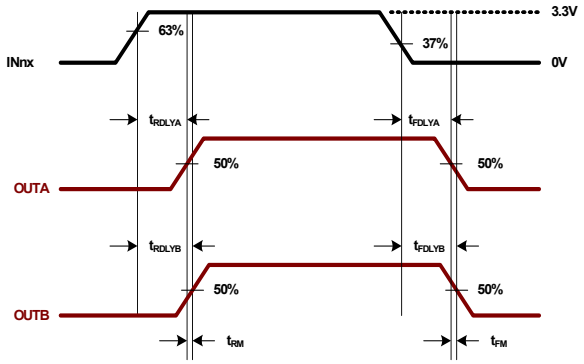


FIGURE 3. PROP DELAYS AND MATCHING

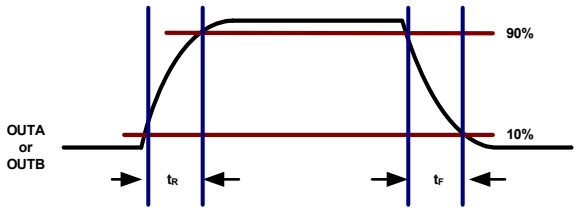


FIGURE 4. RISE/FALL TIMES

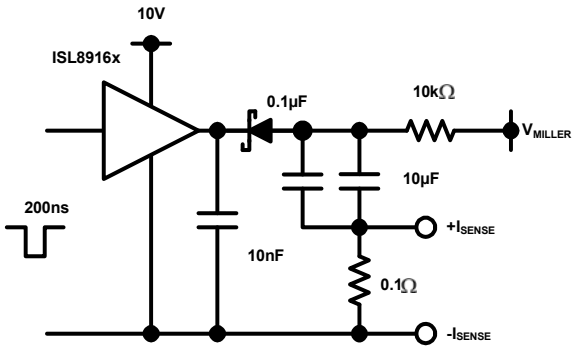


FIGURE 5. MILLER PLATEAU SINK CURRENT TEST CIRCUIT

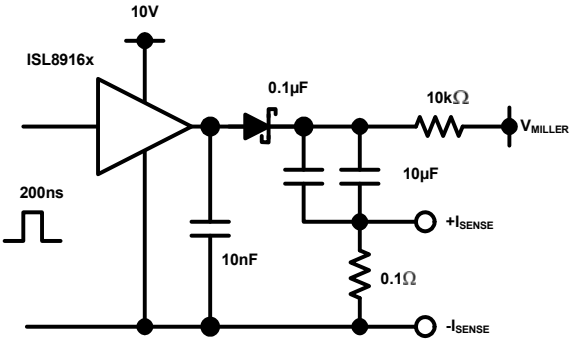


FIGURE 6. MILLER PLATEAU SOURCE CURRENT TEST CIRCUIT

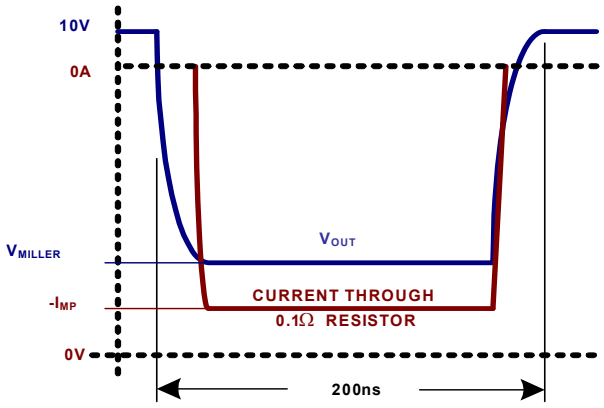


FIGURE 7. MILLER PLATEAU SINK CURRENT

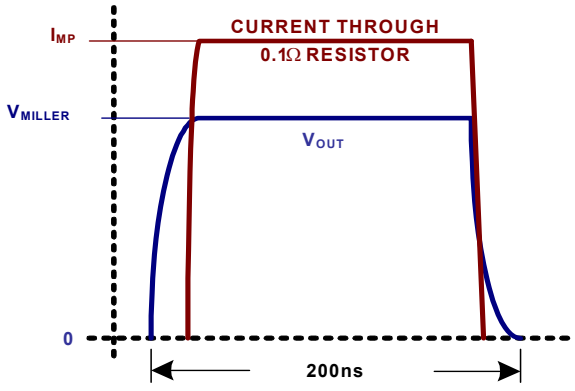


FIGURE 8. MILLER PLATEAU SOURCE CURRENT

Test Waveforms and Circuits (Continued)

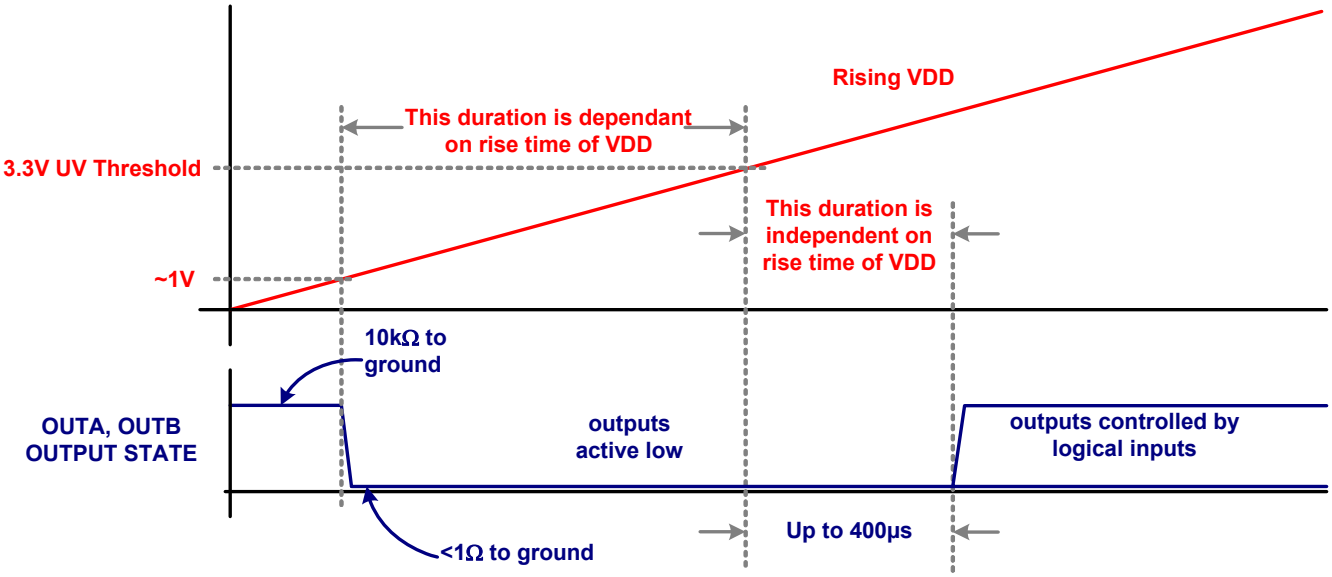


FIGURE 9. START-UP SEQUENCE

Typical Performance Curves

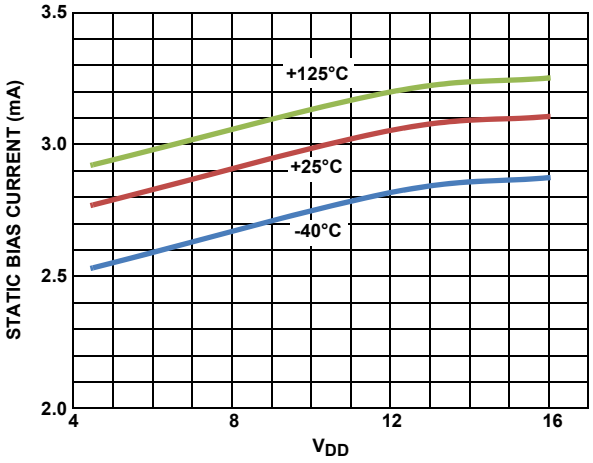


FIGURE 10. I_{DD} vs V_{DD} (STATIC)

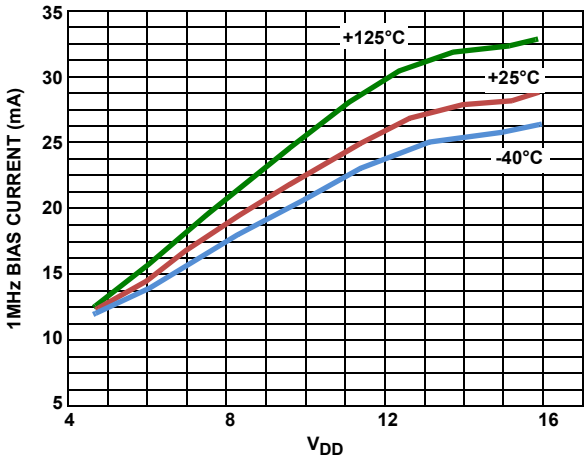


FIGURE 11. I_{DD} vs V_{DD} (1MHz)

Typical Performance Curves (Continued)

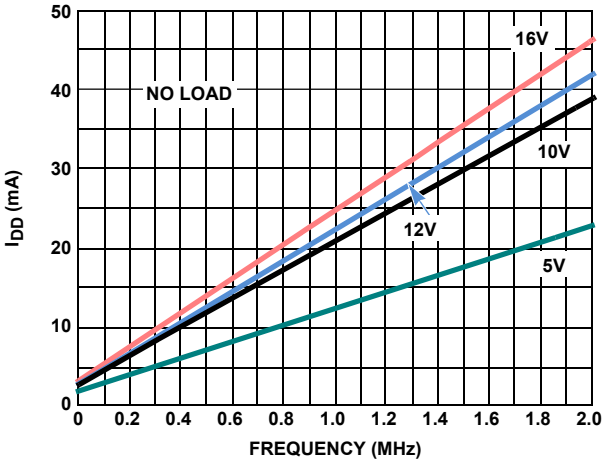


FIGURE 12. I_{DD} vs FREQUENCY (+25°C)

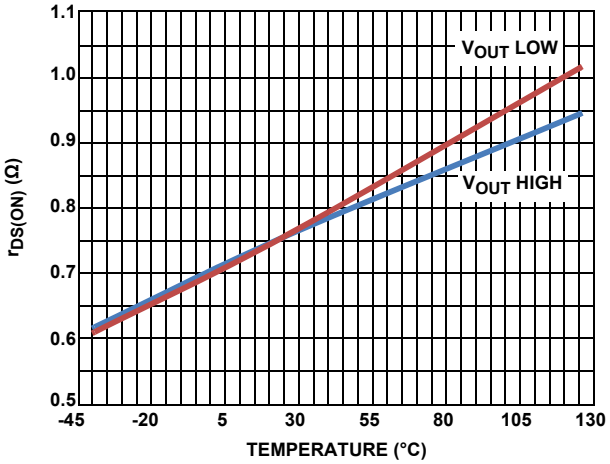


FIGURE 13. $r_{DS(ON)}$ vs TEMPERATURE

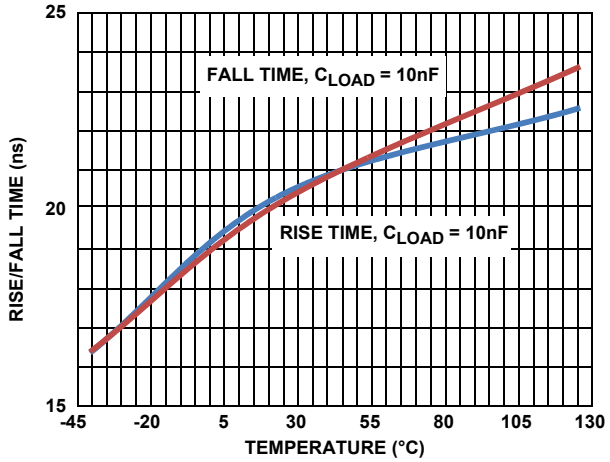


FIGURE 14. OUTPUT RISE/FALL TIMES

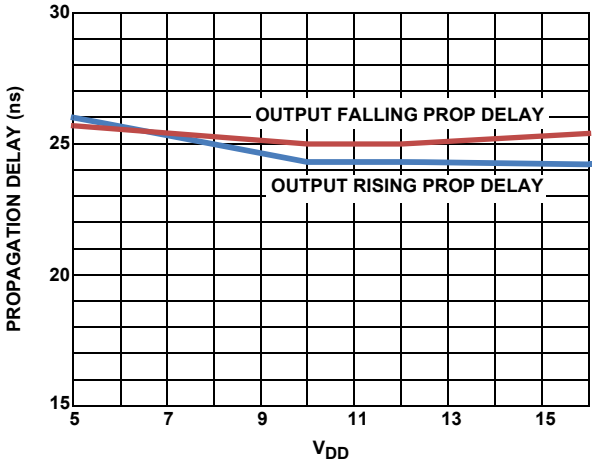


FIGURE 15. PROPAGATION DELAY vs V_{DD}

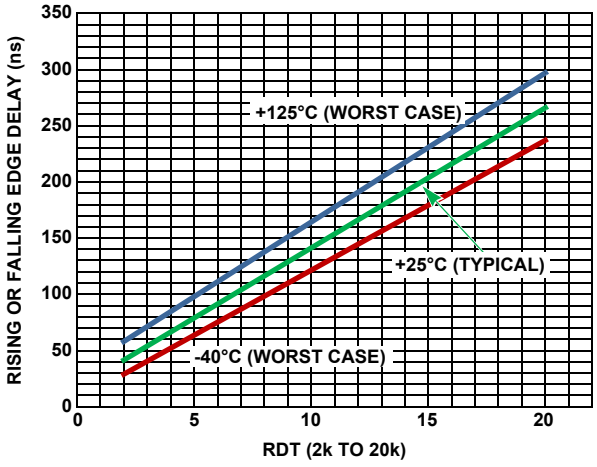


FIGURE 16. PROGRAMMABLE DELAY vs RDEL AND FDEL

Functional Description

Overview

Note: In the following discussion, when a lower case “n” or “x” is used in a pin name, the “n” can be replaced by “1” or “2” and “x” can be replaced by “A” or “B”.

The ISL89367 drivers are designed specifically for Synchronous Rectifier (SR) applications but can also be used for any MOSFET driver application especially when a precision propagation time delay is required for the output rising for falling edge (or both).

The fast rising (or falling) output drive current of the ISL89367 minimizes the turn-on (or off) delay due to the input capacitance of the driven FET. The switching transition period at the Miller plateau is also minimized by the high amplitude drive currents. (See the specified Miller plateau currents in the AC Electrical Specifications on page 6).

The start-up sequence for is designed to prevent unexpected glitches when V_{DD} is being turned on or turned off. When V_{DD} < ~1V, an internal 10kΩ resistor connected between the output and ground, help to keep the gate voltage close to ground. When ~1V < V_{DD} < UV, both outputs are driven low while ignoring the logic inputs. This low state has the same current sinking capacity as during normal operation. This insures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates via the Miller capacitance. When V_{DD} > UVLO, and after a 400µs delay, the outputs now respond to the logic inputs. See Figure 9 for complete details.

For the negative transition of V_{DD} through the UV lockout voltage, the outputs are active low when V_{DD} < ~3.2V_{DC} regardless of the input logic states.

Input Logic Voltage Levels

The input logic (INnx) has thresholds of 37% (falling input) and 63% (rising input). The maximum V_{REF+} relative to V_{REF-} is 10V_{DC}. For typical 5V logic applications V_{REF+} = 5V, V_{REF-} = 0V. In a similar manner, applications with 3.3V logic V_{REF+} = 3.3V and V_{REF-} = 0V. Note that the INVx inputs have TTL compatible thresholds, are V_{DD} tolerant, and do not have precision thresholds.

Programmable Delays

The propagation time delays are programmed by resistors connected between RDELx or FDELx and VSS. A resistor connected to RDELx delays the rising edge of OUTx. Likewise, a resistor connected to FDELx delays the falling edge of OUTx. The resistors should be connected as close as possible to the pins to prevent noise coupling into these connections. In extremely noisy applications, it may be necessary to bypass the resistors with a 0.01µF or smaller decoupling capacitor. The time delay varies linearly between ~40ns and ~265ns for values from 2kΩ to 20kΩ. If no time delay is required, short RDELx and FDELx to VSS. Programmed delays for resistor values <2k are not specified or recommended. Resistor values >20k are also not recommended.

Delays Greater than 270ns

For application requiring delay durations longer than 270ns, the ISL89367 also offers a solution. The input logic pins have precision thresholds which are designed for precision time delays of either the rising of falling edge of OUTx by using the time constant of a resistor and capacitor. The logic inputs pins of the driver, INnx, are connected to the positive inputs of the input comparators. The positive and negative transition threshold voltages are established on the negative inputs of these comparator by a resistor divider that is biased by V_{REF+} and V_{REF-}. If V_{REF+} is connected to the bias voltage of the input logic and if V_{REF-} is connected to the ground of the input logic, then the threshold transitions are proportional to the bias voltage of the input logic. Consequently, the time delays are independent of the accuracy of the input logic bias voltage.

Figure 17 illustrates a circuit that is used to delay the rising edge of OUTA relative to the rising edge of the signal source. The value of C should also be substantially larger than the input capacitance of the input pin of the ISL89367, the parasitic capacitance associated with the traces, and the output capacitance, C_{DS} of the signal FET Q1.

If the signal source is TTL or open drain, R_a is required but not for CMOS.

The calculation of the rising delay is simply shown by Equation 1:

$$t_{delay} = R_b \times C \quad \text{(EQ. 1)}$$

This is a consequence of the 37%/63% thresholds.

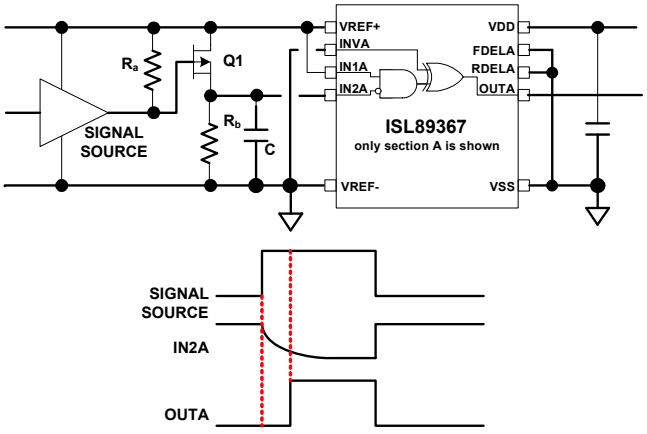


FIGURE 17. RISING OUTA TIME DELAY

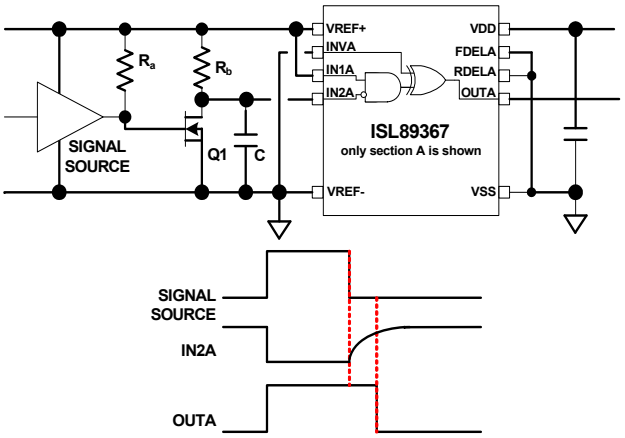


FIGURE 18. FALLING OUTA TIME DELAY

Figure 18 is used to delay the falling edge of OUTx. In this case the rising time constant is R_b x C.

Logic States

The combinational control logic of the ISL89367 is very flexible. The state of OUTx is the ANDed logic of both inputs, IN1x and IN2x. The INVx input to the exclusive-OR gate is used to invert the logic state of OUTx. Frequently, for SR applications, it is desirable to have a logic control that can force OUTA = 0 for the purpose of diode emulation. This “enable” control input can be either of the IN1x or IN2x inputs of one channel. In Figure 1 on page 1, IN1A is used as the enabled input for channel A. When this input is tied to V_{REF+}, OUTA follows the state of IN2x. If INA1 is connected to V_{REF-}, with INVA = 0, OUTA remains low no matter what state IN2A is in.

Paralleling Outputs to Double the Peak Drive Currents

The typical propagation matching of the ISL89367 is less than 1ns. **Note that the propagation matching is only valid when FDELA = RDELA = 0kΩ and FDELB = RDELB = 0kΩ.** The matching is so precise that carefully matched and calibrated scopes probes and scope channels must be used to make this measurement. Because of this excellent performance, these driver outputs can be safely paralleled to double the current drive capacity. It is important that the INA and INB inputs be connected together on the PCB with the shortest possible trace. This is also required of OUTA and OUTB.

Power Dissipation and Die Temp

The following is an example of how to calculate the power dissipated by the ISL89367 driver. These calculations are intended to give an approximate temperature rise of the die junction. Because operating conditions such as air flow can influence the actual temperatures, it is absolutely necessary to confirm the operating temperatures in a specific application by measuring the ISL89367 temperatures with an infra-red temperature sensor or camera. Using a thermal couple to measure the temperature of small devices is not recommended because the thermal couple wire will act as a heat sink reducing the temperature of the measured device to values less than what will actually occur. See Tech Brief TB379 for more information.

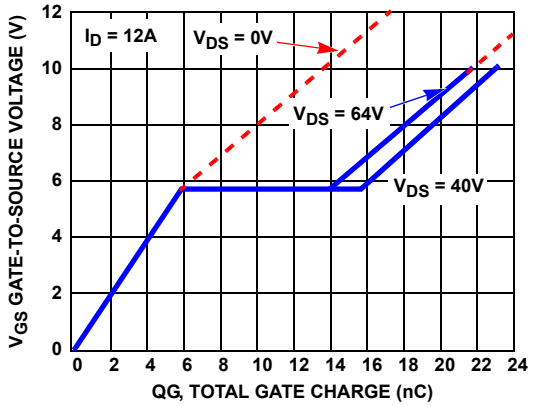


FIGURE 19. CHARGE OF A TYPICAL MOSFET

Figure 19 illustrates how the gate charge varies with gate voltage, V_{GS}, and the V_{DS} of the driven MOSFET. Because an SR is switched on and off when V_{DS} = 0 and if we use V_{GS} = 12V, from the graph, Q_G = 13.5nC. In this example the dissipation of the driver with frequency = 1MHz is shown by Equation 2:

$$P_{gate} = 2 \times Qg \times freq \times V_{GS} = 2 \times 17nC \times 1MHz \times 12 = 0.408W \quad \text{(EQ. 2)}$$

Notice that the dissipation of the driver is not a function of the peak drive rating of the driver. Also if an external gate resistor is used to limit the peak current output, the dissipation is proportionally shared between the value of the gate resistor and the $r_{DS(ON)}$ of the ISL89367 output.

Another parameter that must be considered is the dissipation resulting from the bias current at the frequency of operation. For the ISL89367 the bias current @ V_{DD} = 12V and 1MHz is 24mA.

$$P_{bias} = V_{DS} \times I_{bias} = 12V \times 24mA = 0.288W \quad \text{(EQ. 3)}$$

$$P_{total} = P_{gate} + P_{bias} + 0.408W + 0.288W = 0.696W \quad \text{(EQ. 4)}$$

The Thermal impedances of the ISL89367 are:

θ_{JC} = 3°C/W

θ_{JA} = 36°C/W

The temperature rise is:

$$T_{riseJC} = \theta_{JC} \times P_{total} = 2.09\Delta C \quad \text{(EQ. 5)}$$

T_{riseJC} is the temperature rise referenced to the temperature of the PCB ground plane under the part.

$$T_{riseJA} = \theta_{JA} \times P_{total} = 25\Delta C \quad \text{(EQ. 6)}$$

In this example the temperature rise is relatively small for θ_{JC} and θ_{JA}. Obviously the ISL89367 could drive significantly larger FETs than what is used in this example.

Output Current Rating

While the ISL89367 has a very high peak output current rating of 6A sourcing and sinking, there are limitations to the average output current. With the high peak output current of the ISL89367, it is tempting to use the driver as a general purpose switch to drive loads that are not capacitive as are the gates of MOSFETs. It is important to note that the maximum average output current rating of the ISL89367 of 150mA must not be

overlooked. While this value seems low, it is more than adequate to drive very high gate charge values at high frequencies.

The average output current (sinking or sourcing) into a capacitive load is:

I_{avg} = Qg x freq

or Qg = I_{avg}/freq

for a frequency of 1MHz and for the maximum average current of 150mA:

$$Q_g = 150mA/1MHz = 150nC \quad \text{(EQ. 7)}$$

This charge is approximately 10x the value of the gate charge as in the example of Figure 2 on page 1. Obviously, with lower frequencies, this margin is even greater. It is likely that the greater limitation of driving a large capacitive load could be the power dissipation. If the driver dissipation is recalculated with a value of 150nC, then:

$$P_{gate} = 2 \times 150nC \times 1MHz \times 12V = 3.6W \quad \text{(EQ. 8)}$$

$$T_{riseJA} = 33 \times 3.6W = 119\Delta C \quad \text{(EQ. 9)}$$

PCB Layout Guidelines

The AC performance of the ISL89367 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDD and GND leads. To be effective, these caps must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on OUTA and OUTB. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL89367.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This will inject di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) will have internal parasitic inductance which cannot be eliminated.
  This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.

EPAD Heatsinking Considerations

The thermal pad is electrically connected to the GND supply through the IC substrate. The EPAD of the ISL89367 has two main functions: to provide a quiet GND for the input threshold comparators and to provide heat sinking for the IC. The EPAD must be connected to a ground plane and no switching currents from the driven FET should pass through the ground plane under the IC.

Figure 20 is a PCB layout example of how to use vias to remove heat from the IC through the EPAD.

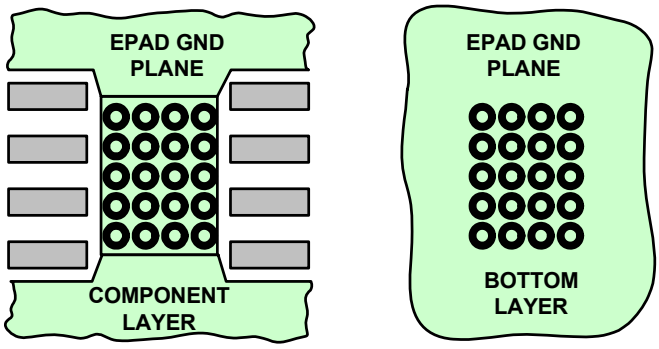


FIGURE 20. TYPICAL PCB PATTERN FOR THERMAL VIAS

For maximum heatsinking, it is recommended that a ground plane, connected to the EPAD, be added to both sides of the PCB. A via array, within the area of the EPAD, will conduct heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the ISL89367, the air flow and the maximum temperature of the air around the IC.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 2, 2012	FN7727.1	(page 1) Related literature added (AN1603) (page 1) Last paragraph of the product description is changed to better describe the improved turn on characteristics. (page 1) Features list is revised to improve readability and to add new product specific features. (page 4) Note and figure references are added to the VDD Under-voltage lock-out parameter. (page 4) Thermal Information, removed Pb-Free Reflow link. (page 5) Note 11 is revised to more clearly describe the turn-on characteristics. (page 6) Test conditions added to the rising and falling propagation matching parameters. (page 8) Figure 9 added to clearly define the startup characteristics. (page 10) The paragraphs of the Functional Description Overview describing the turn-on sequence is replaced by 3 paragraphs to more clearly describe the under voltage and turn-on and turn-off characteristics. (page 11) A new section is added to the application information describing how the drivers outputs can be paralleled.
January 31, 2011	FN7727.0	Initial Release

Products

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To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

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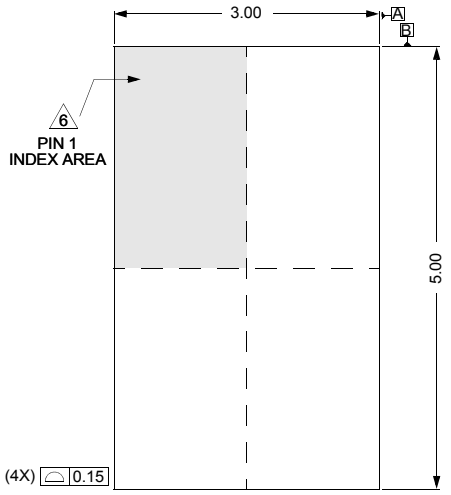
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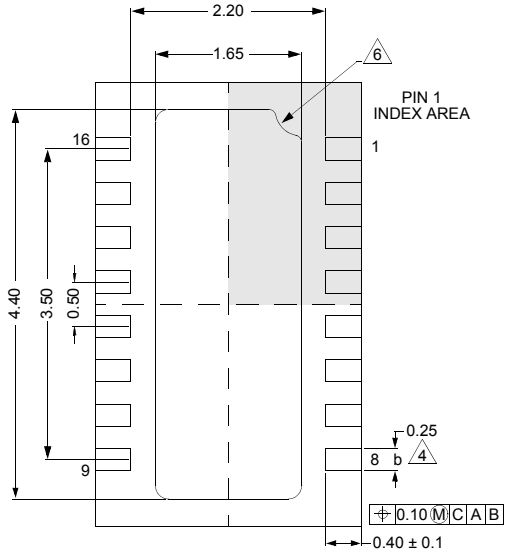
Package Outline Drawing

L16.5x3

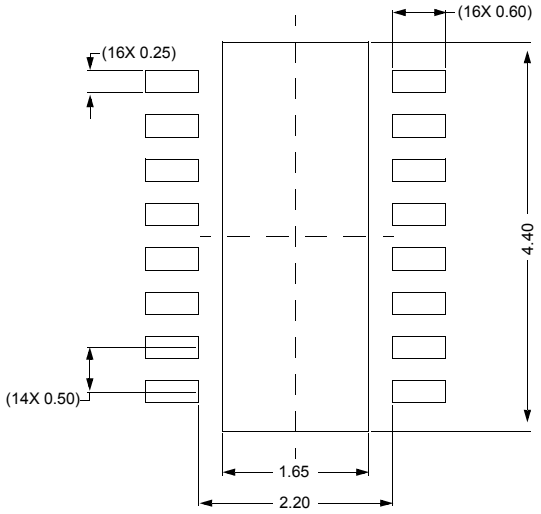
16 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 05/07



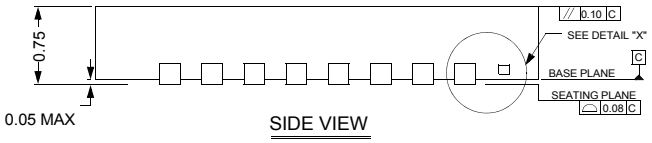
TOP VIEW



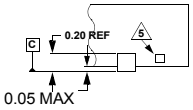
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.