

TPS3610U18, TPS3610T50 BATTERY-BACKUP SUPERVISORS FOR RAM RETENTION

SLVS327B – DECEMBER 2000 – REVISED DECEMBER 2002

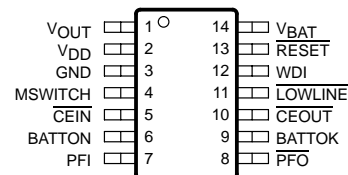
features

- Supply Current of 40 μ A (Max)
- Battery Supply Current of 100 nA (Max)
- Precision Supply-Voltage Monitor, 1.8 V, 5 V; Other Options on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed V_{DD}
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Battery-OK Output
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Chip-Enable Gating . . . 3 ns (at $V_{DD} = 5$ V)
Max Propagation Delay
- Battery-Freshness Seal
- 14-pin TSSOP Package
- Temperature Range . . . -40°C to 85°C

typical applications

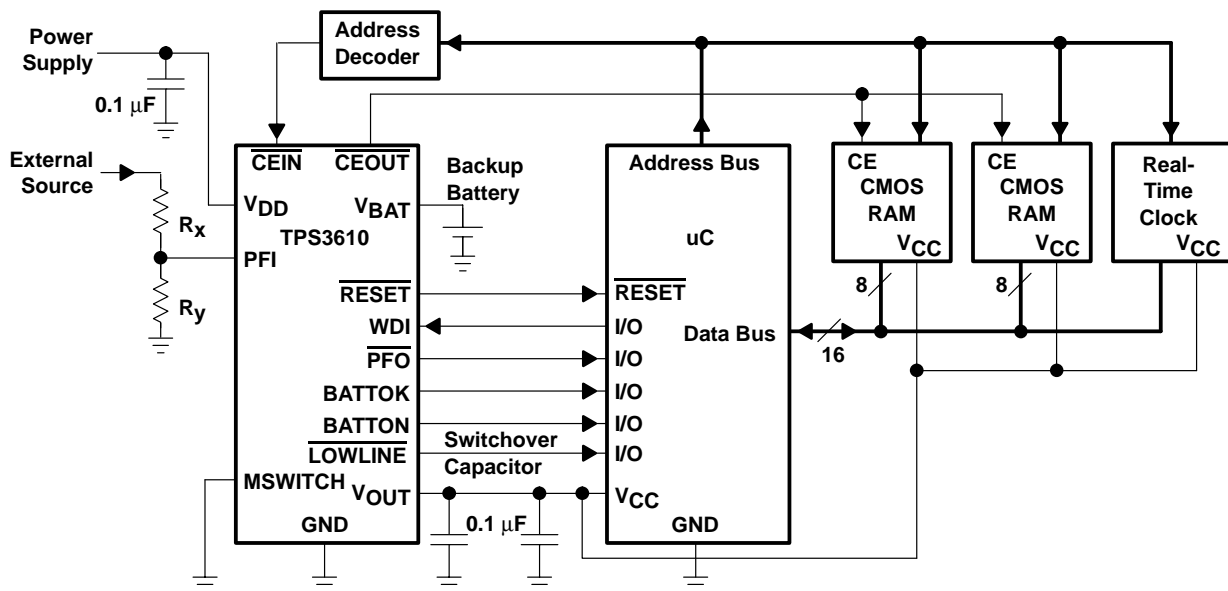
- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery-Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point of Sale Equipment

TPS3610
TSSOP (PW) Package
(TOP VIEW)



ACTUAL SIZE
(5,10mm x 6,60mm)

typical operating circuit



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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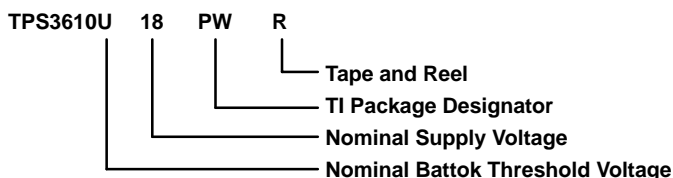
description

The TPS3610 family of supervisory circuits monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM. Other features include an additional power-fail comparator, low-line indication, watchdog function, battery-status indicator, manual switchover, and write protection for CMOS RAM.

The TPS3610 family allow usage of 3-V or 3.6-V lithium batteries as the backup supply in systems with, e.g., $V_{DD} = 1.8$ V. During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply-voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage V_{IT} . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT} . When the supply voltage drops below the threshold voltage V_{IT} , the output becomes active (low) again.

The product spectrum is designed for supply voltages of 1.8 V and 5 V. The circuits are available in a 14-pin TSSOP package. TPS3610 devices are characterized for operation over a temperature range of -40°C to 85°C .

standard and application-specific versions (see Note 1)



APPLICATION-SPECIFIC VERSIONS, NOMINAL SUPPLY AND BATTOK VOLTAGE			
T_A	NOMINAL SUPPLY VOLTAGE, $V_{DD}(\text{NOM})$ (V)	NOMINAL BATTOK THRESHOLD VOLTAGE, $V_{IT}(\text{BOK})$ (V)	PACKAGED DEVICES TSSOP (PW) [†]
-40°C to 85°C	1.8	1.6	TPS3610U18PWR
	5	2.4	TPS3610T50PWR

[†] The PW package is only available taped and reeled (indicated by the R suffix on the device type).

NOTE 1: For other NOMINAL and BATTOK voltage versions, contact your local TI sales office for availability and order lead time.



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TRUTH TABLES

INPUTS				OUTPUTS				
$V_{DD} > V_{LL}$	$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	MSWITCH	V_{OUT}	BATTON	$\overline{LOWLINE}$	\overline{RESET}	\overline{CEOUT}
0	0	0	0	V _{BAT}	1	0	0	DIS
0	0	0	0	V _{BAT}	1	0	0	DIS
0	0	0	1	V _{BAT}	1	0	0	DIS
0	0	0	1	V _{BAT}	1	0	0	DIS
0	0	1	0	V _{DD}	0	0	0	DIS
0	0	1	0	V _{DD}	0	0	0	DIS
0	0	1	1	V _{BAT}	1	0	0	DIS
0	0	1	1	V _{BAT}	1	0	0	DIS
0	1	0	0	V _{DD}	0	0	1	DIS
0	1	0	0	V _{DD}	0	0	1	EN
0	1	0	1	V _{BAT}	1	0	1	DIS
0	1	0	1	V _{BAT}	1	0	1	EN
0	1	1	0	V _{DD}	0	0	1	DIS
0	1	1	0	V _{DD}	0	0	1	EN
0	1	1	1	V _{BAT}	1	0	1	DIS
0	1	1	1	V _{BAT}	1	0	1	EN
1	1	0	0	V _{DD}	0	1	1	DIS
1	1	0	0	V _{DD}	0	1	1	EN
1	1	0	1	V _{BAT}	1	1	1	DIS
1	1	0	1	V _{BAT}	1	1	1	EN
1	1	1	0	V _{DD}	0	1	1	DIS
1	1	1	0	V _{DD}	0	1	1	EN
1	1	1	1	V _{BAT}	1	1	1	DIS
1	1	1	1	V _{BAT}	1	1	1	EN

BATTOK		POWER-FAIL		CHIP-ENABLE	
$V_{BAT} > V_{BOK}$	BATTOK	$PFI > V_{(PFI)}$	\overline{PFO}	\overline{CEIN}	\overline{CEOUT}
0	0	0	0	0	0
1	1	1	1	1	1

Condition: $V_{DD} > V_{IT}$

Condition: $V_{DD} > V_{DDmin}$

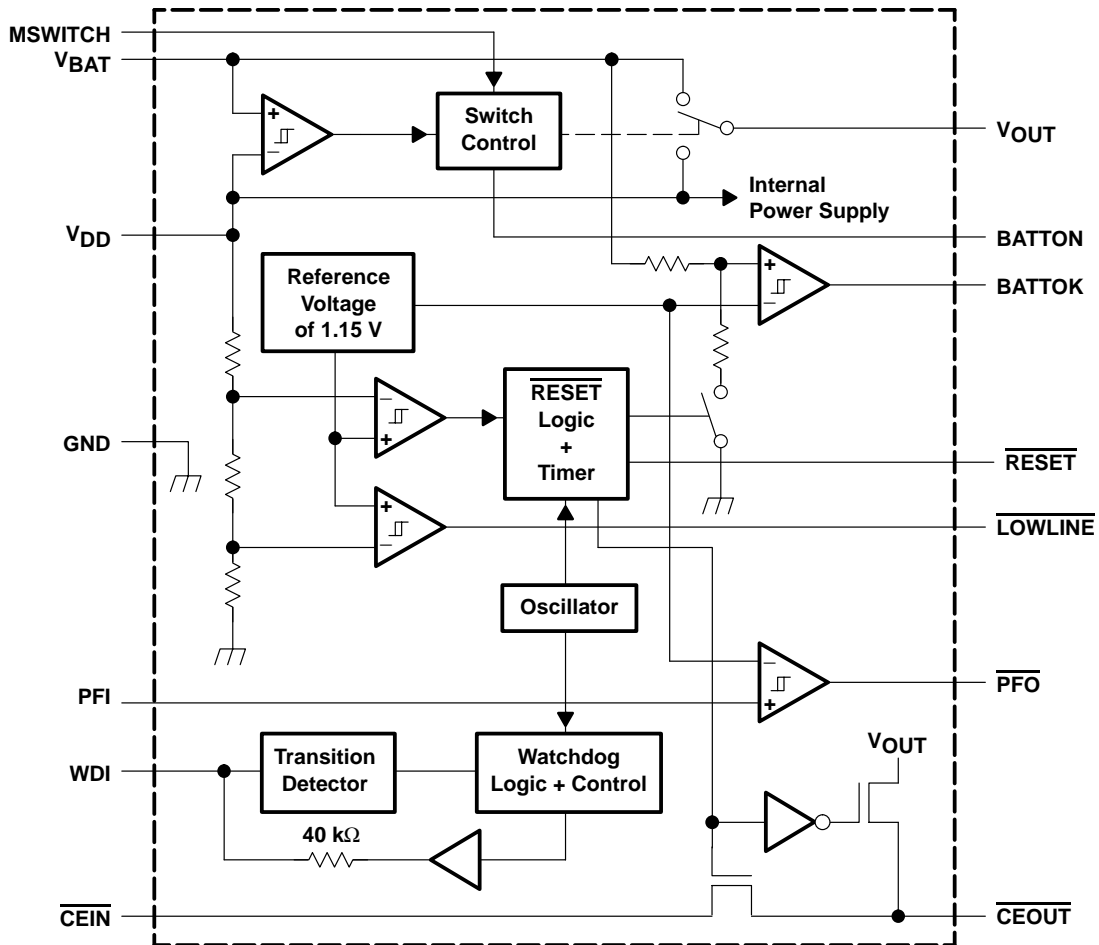
Condition: Enabled



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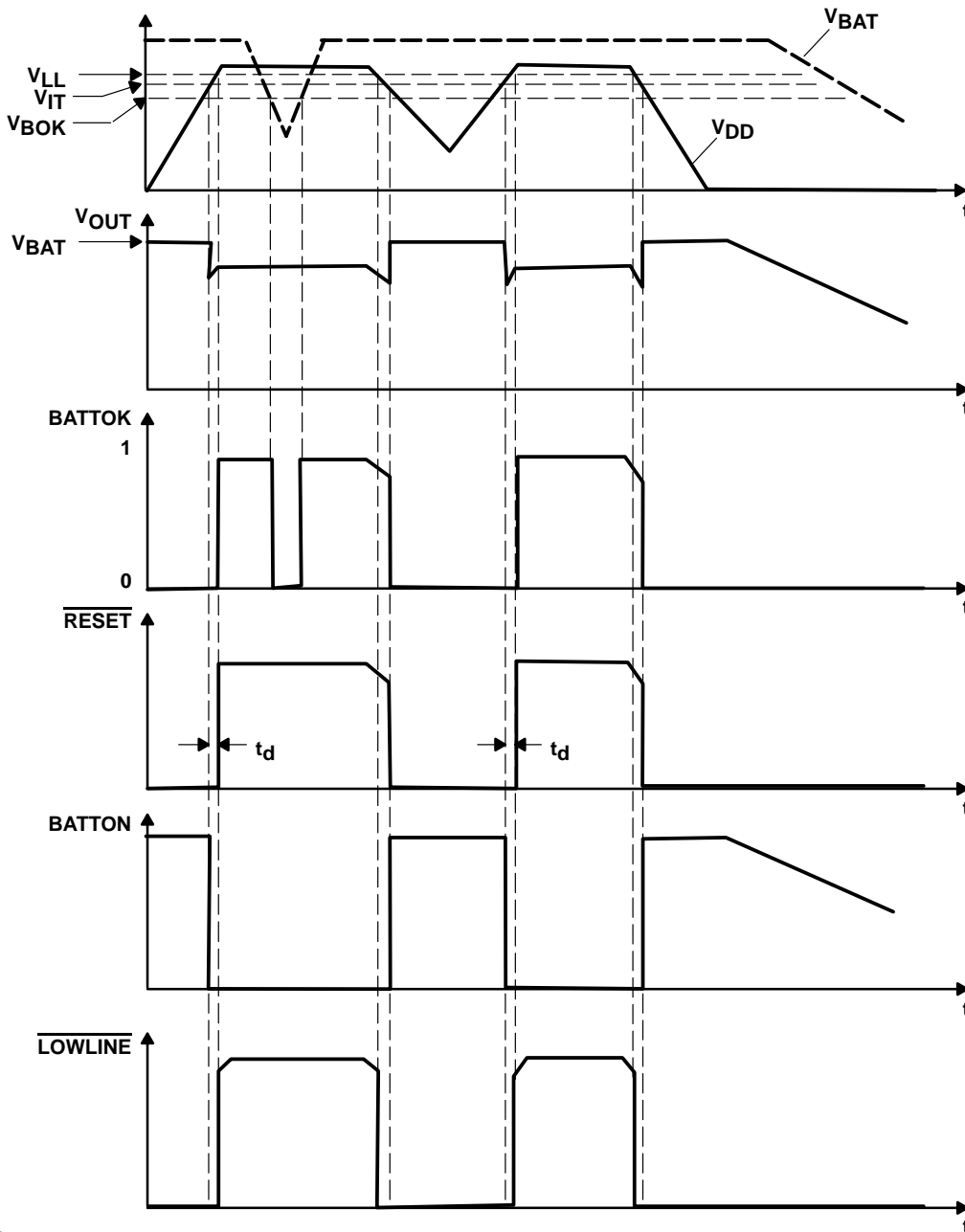
functional block diagram



TPS3610U18, TPS3610T50 BATTERY-BACKUP SUPERVISORS FOR RAM RETENTION

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timing diagram



† MSWITCH = 0

Timing diagram shown under operation, not in freshness seal mode.

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BATTOK	9	O	Battery status output
BATTON	6	O	Logic output/external bypass switch driver output
$\overline{\text{CEIN}}$	5	I	Chip-enable input
$\overline{\text{CEOUT}}$	10	O	Chip-enable output
GND	3	I	Ground
$\overline{\text{LOWLINE}}$	11	O	Early power-fail warning output
MSWITCH	4	I	Manual switch to force device into battery-backup mode
V _{OUT}	1	O	Supply output
PFI	7	I	Power-fail comparator input
$\overline{\text{PFO}}$	8	O	Power-fail comparator output
$\overline{\text{RESET}}$	13	O	Active-low reset output
V _{BAT}	14	I	Backup-battery input
V _{DD}	2	I	Input supply voltage
WDI	12	I	Watchdog timer input

detailed description

battery freshness seal

The battery freshness seal of the TPS3610 family disconnects the backup battery from internal circuitry until it is needed. This function ensures that the backup battery connected to V_{BAT} is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} (V_{BAT} > V_{BATmin})
2. Ground $\overline{\text{PFO}}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply (V_{DD} > V_{IT}) and keep connected for 5 ms < t < 35 ms

The battery freshness seal mode is disabled by the positive-going edge of $\overline{\text{RESET}}$ when V_{DD} is applied.

BATTOK output

BATTOK is a logic feedback of the device to indicate the status of the backup battery. The supervisor checks the battery voltage every 200 ms with a voltage divider load of approximately 100 kΩ and a measurement cycle on-time of 25 μs. The measurement cycle starts after the reset is released. If the battery voltage V_{BAT} is below the negative-going threshold voltage V_{IT(BOK)}, the indicator BATTOK does a high-to-low transition. Otherwise it retains its status to V_{DD} level.

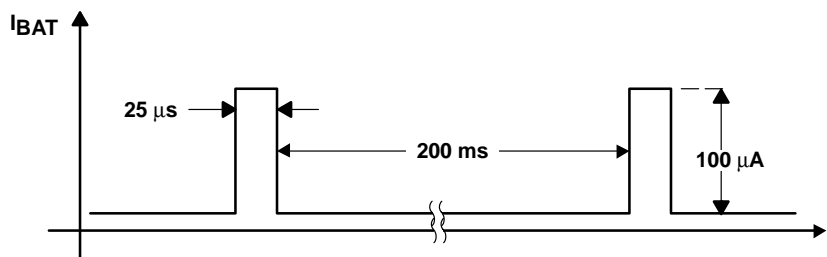


Figure 1. BATTOK Timing



detailed description (continued)

chip-enable signal gating

The internal gating of chip-enable signals, CE, prevents erroneous data from corrupting CMOS RAM during an undervoltage condition. The TPS3610 use a series transmission gate from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$. During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{\text{CEIN}}$ to $\overline{\text{CEOUT}}$ enables TPS3610 devices to be used with most processors.

The CE transmission gate is disabled and $\overline{\text{CEIN}}$ is high-impedance (disable mode) while reset is asserted. During a power-down sequence, when V_{DD} crosses the reset threshold, the CE transmission gate is disabled and $\overline{\text{CEIN}}$ immediately becomes high impedance if the voltage at $\overline{\text{CEIN}}$ is high. If $\overline{\text{CEIN}}$ is low while reset is asserted, the CE transmission gate is disabled at the same time $\overline{\text{CEIN}}$ goes high, or 15 μs after $\overline{\text{RESET}}$ asserts, whichever occurs first. This allows the current write cycle to complete during power-down. When the CE transmission gate is enabled, the impedance of $\overline{\text{CEIN}}$ appears as a resistor in series with the load at $\overline{\text{CEOUT}}$. The overall device propagation delay through the CE transmission gate depends on V_{OUT} , the source impedance of the device connected to $\overline{\text{CEIN}}$ and the load at $\overline{\text{CEOUT}}$. To achieve minimum propagation delay, the capacitive load at $\overline{\text{CEOUT}}$ should be minimized, and a low-output-impedance driver should be used.

During disable mode, the transmission gate is off and an active pullup connects $\overline{\text{CEOUT}}$ to V_{OUT} . The pullup turns off when the transmission gate is enabled.

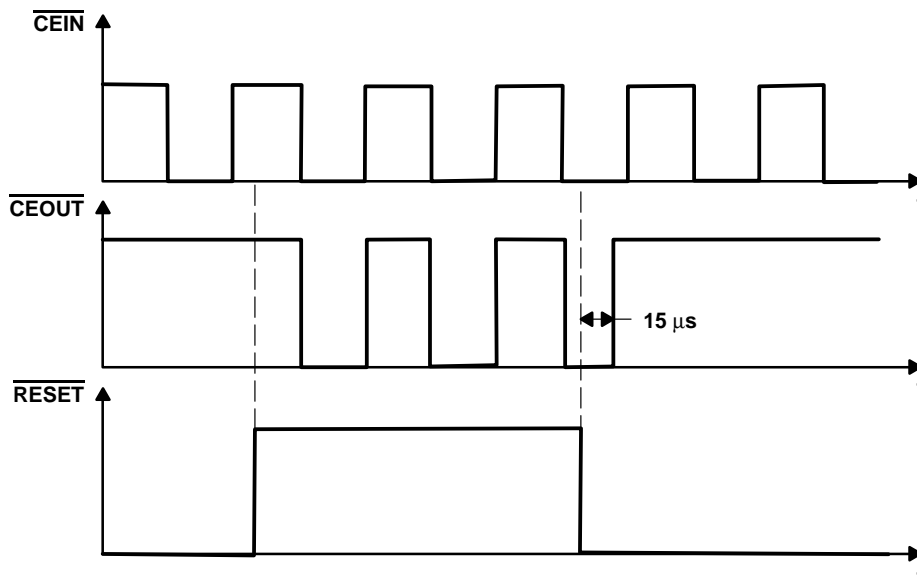


Figure 2. Chip-Enable Timing

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detailed description (continued)

power-fail comparator (PFI and $\overline{\text{PFO}}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold $V_{\text{IT(PFI)}}$ of typical 1.15 V, the power-fail output ($\overline{\text{PFO}}$) goes low. If $V_{\text{IT(PFI)}}$ goes above $V_{\text{(PFI)}}$, plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{\text{(PFI)}}$. The sum of both resistors should be about 1 M Ω , to minimize power consumption and also to assure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, PFI should be connected to ground and $\overline{\text{PFO}}$ left unconnected.

LOWLINE

The lowline comparator monitors V_{DD} with a threshold voltage typically 2% above the reset threshold (V_{IT}). For normal operation (V_{DD} above the reset threshold), $\overline{\text{LOWLINE}}$ is pulled to V_{DD} . $\overline{\text{LOWLINE}}$ can be used to provide a nonmaskable interrupt (NMI) to the processor when power begins to fall. In most battery-operated portable systems, reserve energy in the battery provides enough time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must also contend with a more rapid V_{DD} fall time, such as when the main battery is disconnected or a high-side switch is opened during normal operation, a capacitor can be used on the V_{DD} line to provide enough time for executing the shutdown routine. First, the worst-case settling time (t_{sd}) required for the system to perform its shutdown routine needs to be defined. Then, using the worst-case load current (I_{L}) that can be drained from the capacitor, and the minimum reset threshold voltage (V_{ITmin}), the capacitor value (C_{H}) can be calculated as follows:

$$C_{\text{H}} = \frac{I_{\text{L}} \times t_{\text{sd}}}{V_{\text{ITmin}} \times 0.012}$$

BATTON

Most often BATTON is used as a gate drive for an external pass transistor for high-current applications. In addition, it can be used as a logic output to indicate the battery switchover status. BATTON is high when V_{OUT} is connected to V_{BAT} .

BATTON can be connected directly to the gate of a PMOS transistor (see Figure 3). No current-limiting resistor is required. If a PMOS transistor is used, it must be connected in the reverse of the traditional method (see Figure 3), which orients the body diode from V_{DD} to V_{OUT} and prevents the backup battery from discharging through the FET when its gate is high.

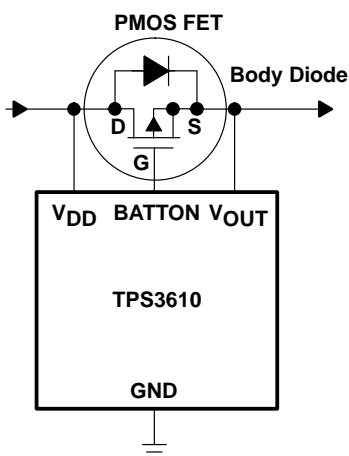


Figure 3. Driving an External MOSFET Transistor With BATTON

detailed description (continued)

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup-battery is installed at V_{BAT} , the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup-battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD} , these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD} . V_{BAT} only connects to V_{OUT} (through a 15- Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD} . When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT} , or until V_{DD} rises above the reset threshold V_{IT} . V_{OUT} connects to V_{DD} through a 1- Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

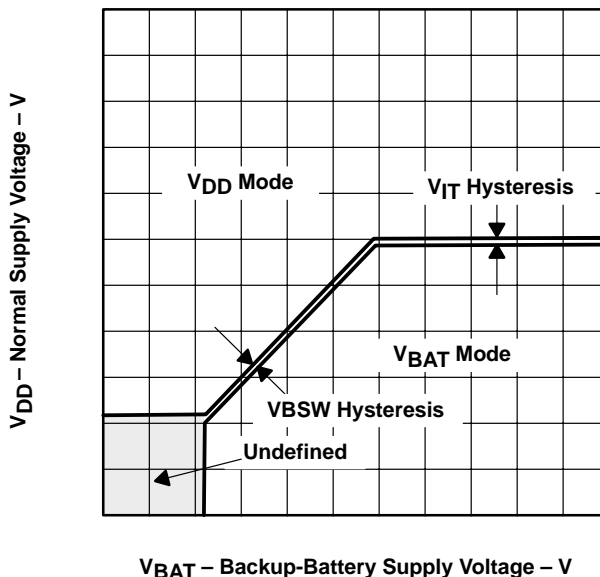


Figure 4. Normal Supply Voltage vs Backup-Battery Supply Voltage

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detailed description (continued)

manual switchover (MSWITCH)

While operating in the normal mode from V_{DD} , the device can be forced manually to operate in battery-backup mode by connecting MSWITCH to V_{DD} . Refer to Table 1 for different switchover modes.

Table 1. Switchover Modes

	MSWITCH	STATUS
V_{DD} mode	GND	V_{DD} mode
	V_{DD}	Switch to battery-backup mode
Battery-backup mode	GND	Battery-backup mode
	V_{DD}	Battery-backup mode

If the manual switchover feature is not used, MSWITCH *must* be connected to ground.

watchdog

In a microprocessor- or DSP-based system, it is important not only to supervise the supply voltage, but also to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller or DSP has to toggle the watchdog input within typically 0.8 s to avoid the occurrence of a time-out. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and is retriggered internally.

saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then the input momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), WDI should be left low for the majority of the watchdog time-out period, and pulsed low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, a current of, e.g., $5\text{ V}/40\text{ k}\Omega \approx 125\text{ }\mu\text{A}$, can flow into WDI.

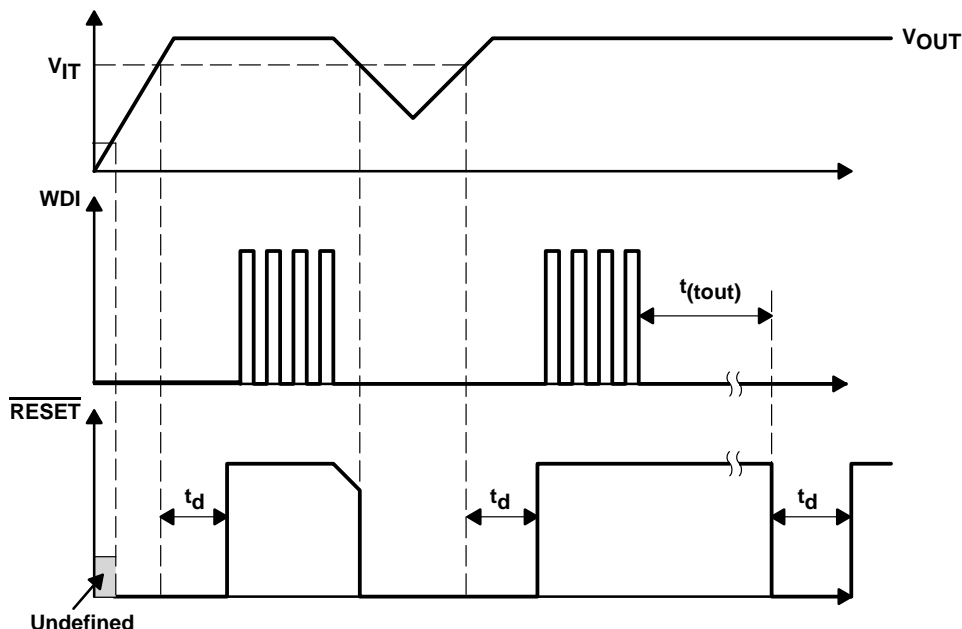


Figure 5. Watchdog Timing

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 2)	7 V
All other pins (see Note 2)	–0.3 V to 7 V
Continuous output current at V_{OUT} , $I_O(V_{OUT})$	400 mA
Continuous output current (all other pins) I_O	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than $t=1000h$ continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PW	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	$V_{DD}+0.3$	V
High-level input voltage, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL}		$0.3 \times V_{DD}$	V
Continuous output current at V_{OUT} , I_O		300	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$		100	ns/V
Slew rate at V_{DD} or V_{BAT}		1	V/ μs
Operating free-air temperature range, T_A	–40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	$\overline{\text{RESET}}$, BAT _{TOK}	V _{DD} = 1.8 V, I _{OH} = -400 μA	V _{DD} -0.2 V			V
			V _{DD} = 3.3 V, I _{OH} = -2 mA	V _{DD} -0.4 V			
			V _{DD} = 5 V, I _{OH} = -3 mA				
	BAT _{TON}	V _{OUT} = 1.8 V, I _{OH} = -400 μA	V _{OUT} -0.2 V				
		V _{OUT} = 3.3 V, I _{OH} = -2 mA	V _{OUT} -0.4 V				
		V _{OUT} = 5 V, I _{OH} = -3 mA					
	$\overline{\text{LOWLINE}}$, P _{F0}	V _{DD} = 1.8 V, I _{OH} = -20 μA	V _{DD} -0.3 V				
		V _{DD} = 3.3 V, I _{OH} = -80 μA,	V _{DD} -0.4 V				
		V _{DD} = 5 V, I _{OH} = -120 μA					
	$\overline{\text{CEOUT}}$, Enable mode, CE _{IN} = V _{OUT}	V _{OUT} = 1.8 V, I _{OH} = -1 mA	V _{OUT} -0.2 V				
		V _{OUT} = 3.3 V, I _{OH} = -2 mA	V _{OUT} -0.3 V				
		V _{OUT} = 5 V, I _{OH} = -5 mA					
$\overline{\text{CEOUT}}$, Disable mode	V _{OUT} = 3.3 V, I _{OH} = -0.5 mA	V _{OUT} -0.4 V					
V _{OL}	Low-level output voltage	$\overline{\text{RESET}}$, $\overline{\text{PFO}}$, BAT _{TOK} , $\overline{\text{LOWLINE}}$	V _{DD} = 1.8 V, I _{OL} = 400 μA			0.2	V
			V _{DD} = 3.3 V, I _{OL} = 2 mA			0.4	
			V _{DD} = 5 V, I _{OL} = 3 mA				
	BAT _{TON}	V _{OUT} = 1.8 V, I _{OL} = 500 μA			0.2		
		V _{OUT} = 3.3 V, I _{OL} = 3 mA			0.4		
		V _{OUT} = 5 V, I _{OL} = 5 mA					
	$\overline{\text{CEOUT}}$, Enable mode, CE _{IN} = 0 V	V _{OUT} = 1.8 V, I _{OL} = 1 mA			0.2		
		V _{OUT} = 3.3 V, I _{OL} = 2 mA			0.3		
		V _{OUT} = 5 V, I _{OL} = 5 mA					
Power-up reset voltage (see Note 3)		I _{OL} = 20 μA,	V _{BAT} > 1.1 V, OR V _{DD} > 1.1 V,			0.4	V
V _{OUT}	Normal mode	I _O = 8.5 mA, V _{BAT} = 0 V	V _{DD} = 1.8 V,	V _{DD} -50 mV			V
		I _O = 125 mA, V _{BAT} = 0 V	V _{DD} = 3.3 V,	V _{DD} -150 mV			
		I _O = 200 mA, V _{BAT} = 0 V	V _{DD} = 5 V,	V _{DD} -200 mV			
	Battery-backup mode	I _O = 0.5 mA, V _{BAT} = 1.5 V	V _{DD} = 0 V,	V _{BAT} -20 mV			
		I _O = 7.5 mA, V _{BAT} = 3.3 V	V _{DD} = 0 V,	V _{BAT} -113 mV			

NOTE 3: The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. t_r , V_{DD} ≥ 15 μs/V



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IT}	Negative-going input threshold voltage (see Note 4)	TPS3610U18	T _A = -40°C to 85°C	1.68	1.71	1.74	V
		TPS3610T50		4.46	4.55	4.64	
V(PFI)		PFI		1.13	1.15	1.17	
V(BOK)		TPS3610T50		2.33	2.4	2.47	
		TPS3610U18		1.55	1.6	1.65	
V(LL)		LOWLINE			V _{IT} +1.2%	V _{IT} +2%	V _{IT} +2.8%
V _{hys}	Hysteresis	V _{IT}	1.65 V < V _{IT} < 2.5 V	20		mV	
			2.5 V < V _{IT} < 3.5 V	40			
			3.5 V < V _{IT} < 5.5 V	60			
		LOWLINE	1.65 V < V(LL) < 2.5 V	20			
			2.5 V < V(LL) < 3.5 V	40			
			3.5 V < V(LL) < 5.5 V	60			
		BAT TOK	1.65 V < V(BOK) < 2.5 V	20			
			2.5 V < V(BOK) < 3.5 V	40			
			3.5 V < V(BOK) < 5.5 V	60			
		PFI		12			
V _{BSW} (see Note 5)	V _{DD} = 1.8 V	55					
I _{IH}	High-level input current	WDI	WDI = V _{DD} = 5 V	150		μA	
I _{IL}	Low-level input current	(see Note 6)	WDI = 0 V, V _{DD} = 5 V	-150			
I _I	Input current	PFI, MSWITCH		-25	25		nA
I _{OS}	Short-circuit output current	PFO	PFO = 0 V	V _{DD} = 1.8 V	-0.3		mA
				V _{DD} = 3.3 V	-1.1		
				V _{DD} = 5 V	-2.4		
I _{DD}	Supply current at V _{DD}	V _{OUT} = V _{DD}		40		μA	
		V _{OUT} = V _{BAT}		40			
I _{BAT}	Supply current at V _{BAT}	V _{OUT} = V _{DD}		-0.1	0.1		μA
		V _{OUT} = V _{BAT}		0.5			
I _{Ikg}	Leakage current at \overline{CEIN}	Disable mode, V _I < V _{DD}		±1		μA	
r _{DS(on)}	V _{DD} to V _{OUT} on-resistance	V _{DD} = 5 V		0.6	1		Ω
	V _{BAT} to V _{OUT} on-resistance	V _{BAT} = 3.3 V		8	15		
C _i	Input capacitance	V _I = 0 V to 5 V		5		pF	

- NOTES: 4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.
5. For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}
6. For details on how to optimize current consumption when using WDI. Refer to detailed description section, *watchdog*.



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timing requirements at $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = -40^\circ\text{C}$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	At V_{DD}	$V_{IH} = V_{IT} + 0.2\text{ V}$, $V_{IL} = V_{IT} - 0.2\text{ V}$	6		μs
		At WDI	$V_{DD} = V_{IT} + 0.2\text{ V}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100		ns

switching characteristics at $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = -40^\circ\text{C}$ to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time	$V_{DD} > V_{IT} + 0.2\text{ V}$	60	100	140	ms
$t_{(tout)}$	Watchdog timeout	(see timing diagram)	0.48	0.8	1.12	s
t_{PLH}	Propagation (delay) time, low-to-high-level output	50% $\overline{\text{RESET}}$ to 50% $\overline{\text{CEOUT}}$		15		μs
t_{PHL}	Propagation (delay) time, high-to-low-level output	$V_{DD} = 1.8\text{ V}$		5	15	ns
		$V_{DD} = 3.3\text{ V}$		1.6	5	
		$V_{DD} = 5\text{ V}$		1	3	
		V_{DD} to $\overline{\text{RESET}}$	$V_{IL} = V_{IT} - 0.2\text{ V}$, $V_{IH} = V_{IT} + 0.2\text{ V}$		2	5
PFI to $\overline{\text{PFO}}$	$V_{IL} = V(\text{PFI}) - 0.2\text{ V}$, $V_{IH} = V(\text{PFI}) + 0.2\text{ V}$		3	5		
t_t	Transition time	V_{DD} to $\overline{\text{BATTON}}$			3	μs

NOTE 7: Specified by design

TYPICAL CHARACTERISTICS

Table of Graphs

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$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	6
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TYPICAL CHARACTERISTICS

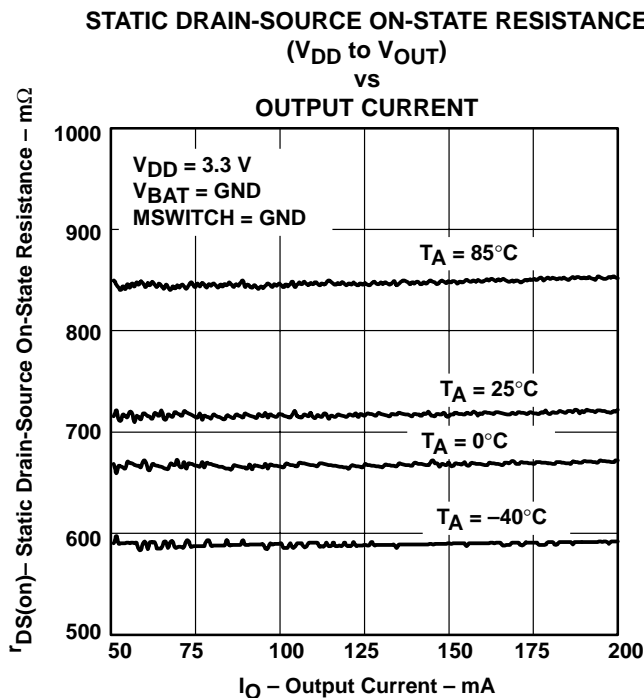


Figure 6

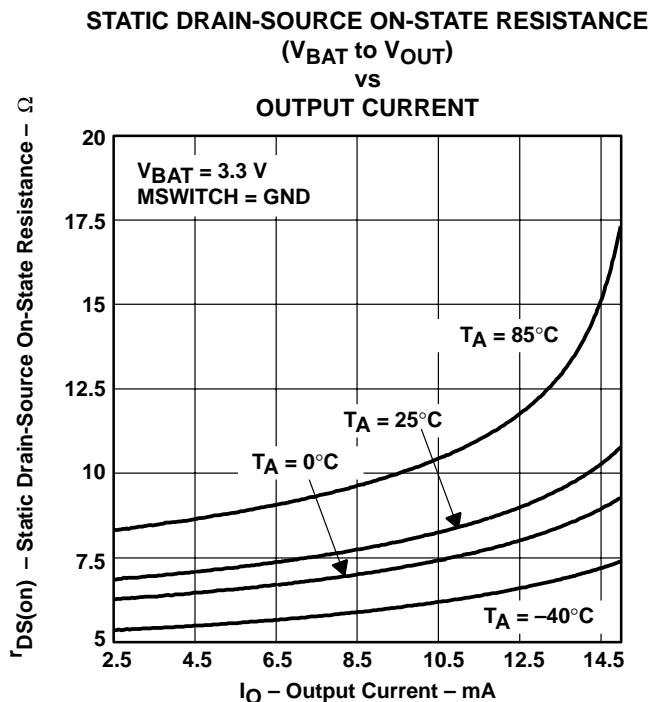


Figure 7

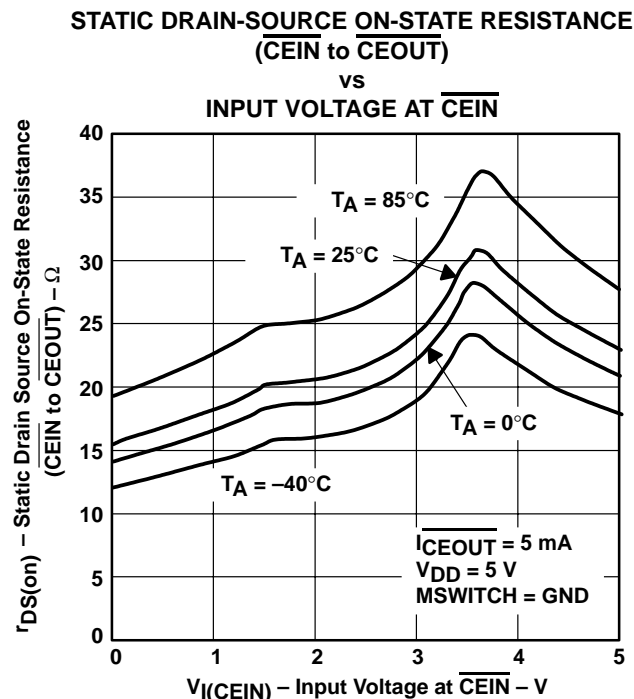


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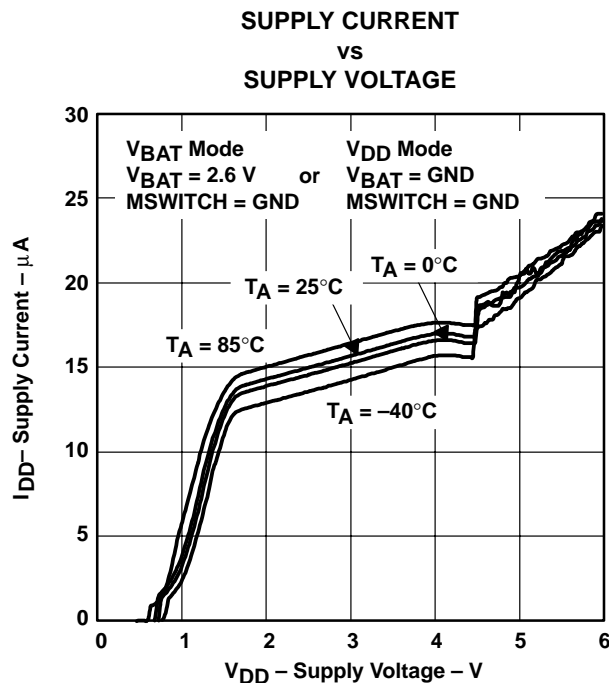


Figure 9

TPS3610U18, TPS3610T50 BATTERY-BACKUP SUPERVISORS FOR RAM RETENTION

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TYPICAL CHARACTERISTICS

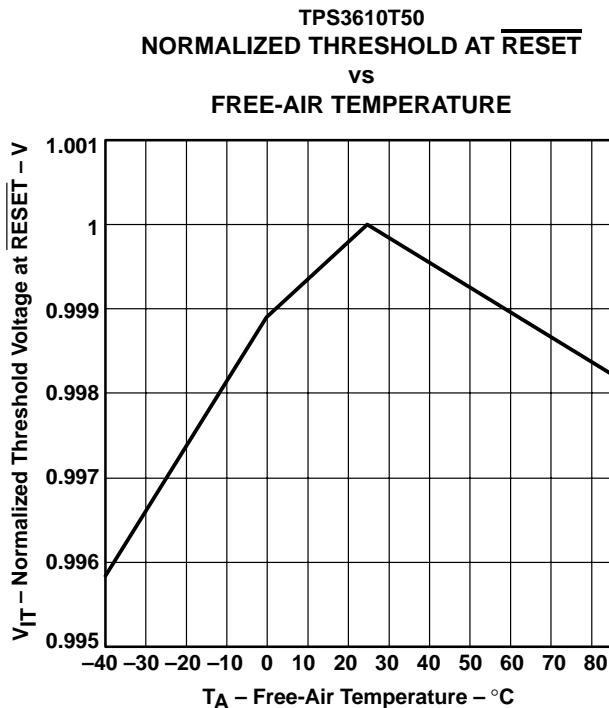


Figure 10

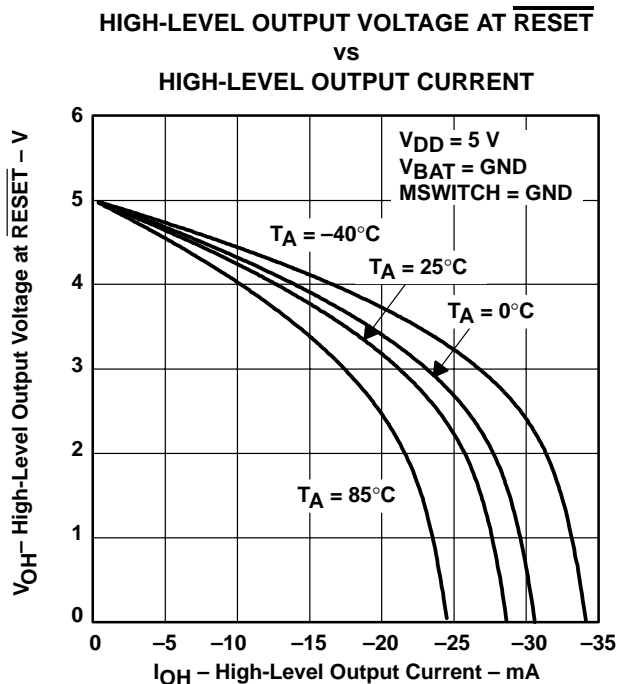


Figure 11

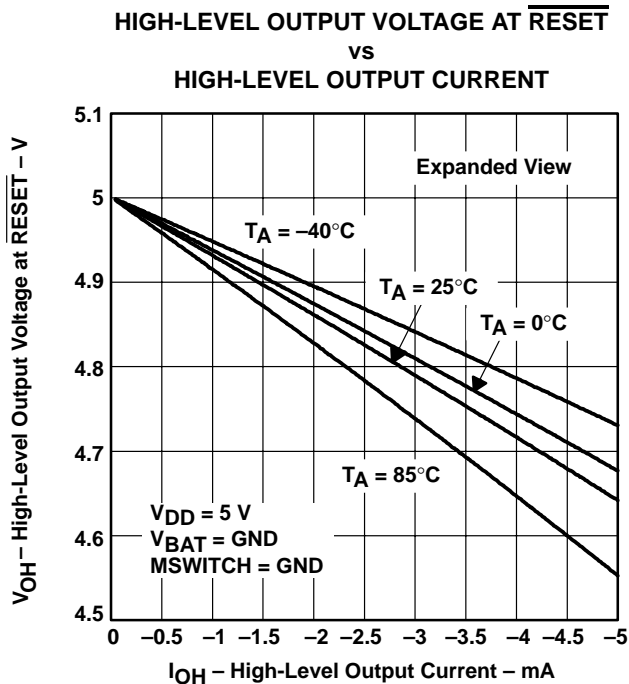


Figure 12



TYPICAL CHARACTERISTICS

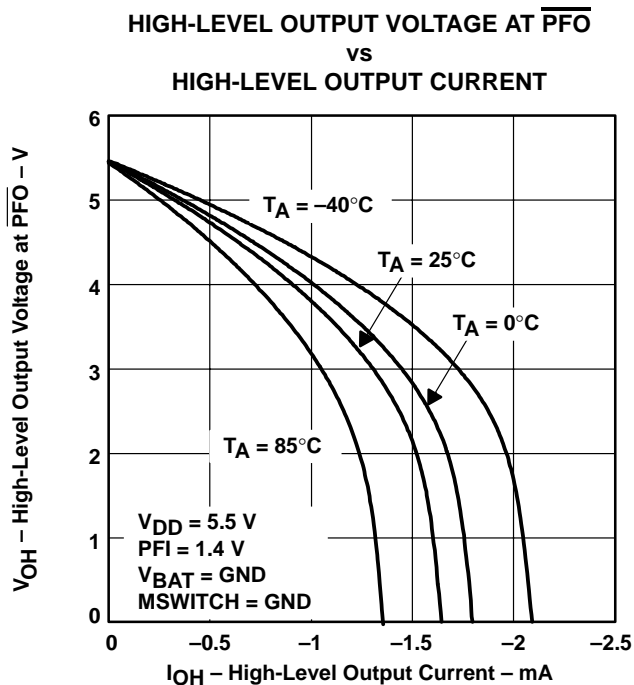


Figure 13

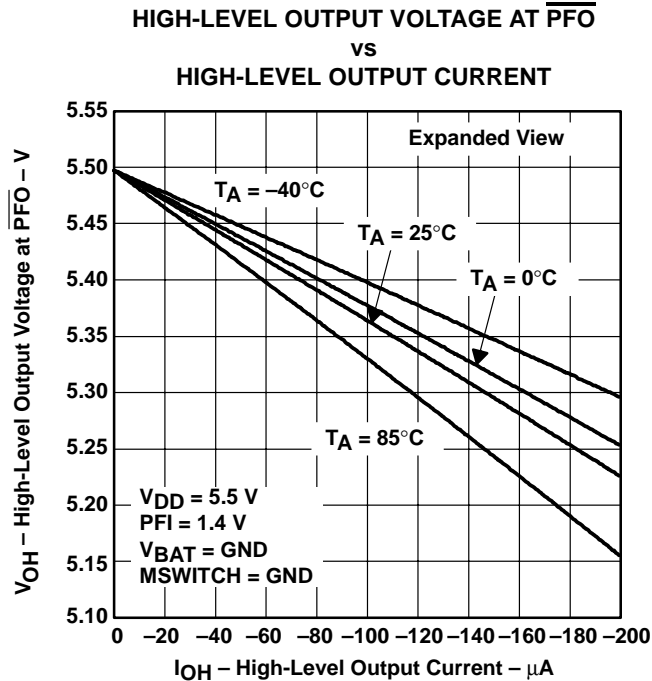


Figure 14

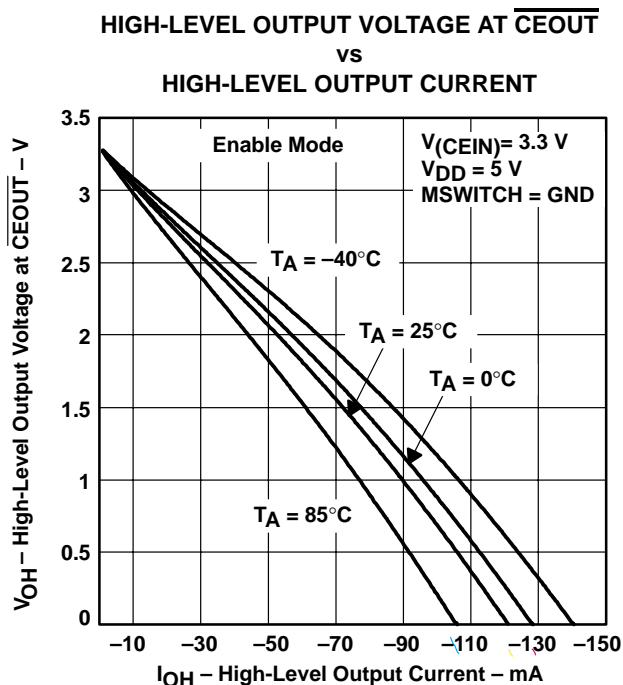


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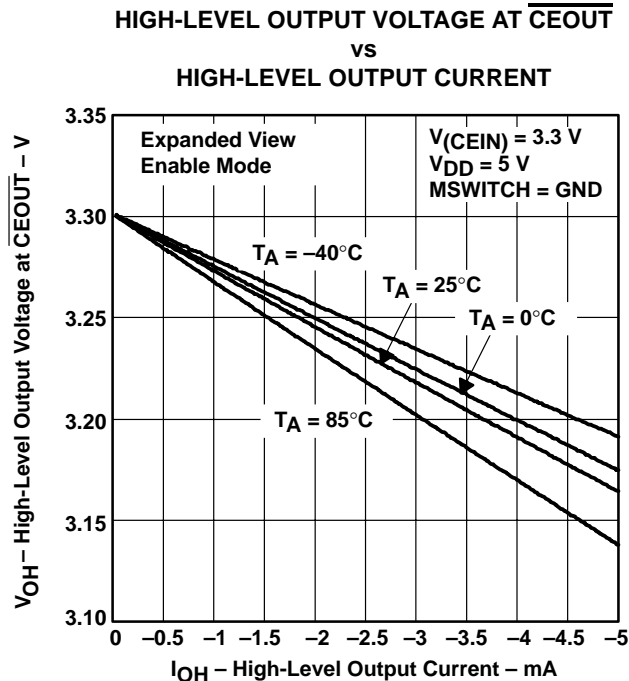
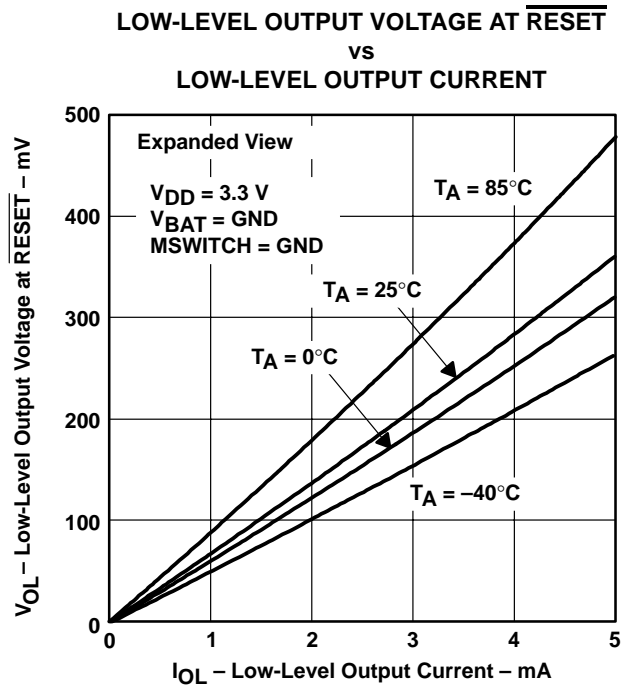
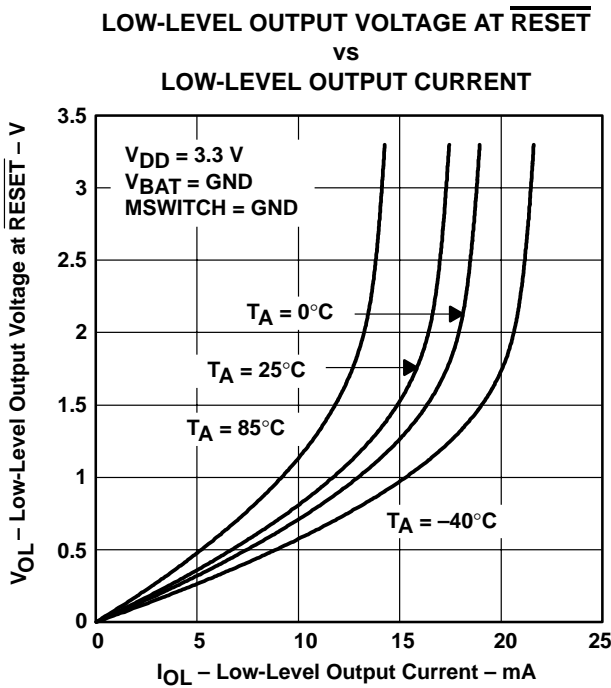
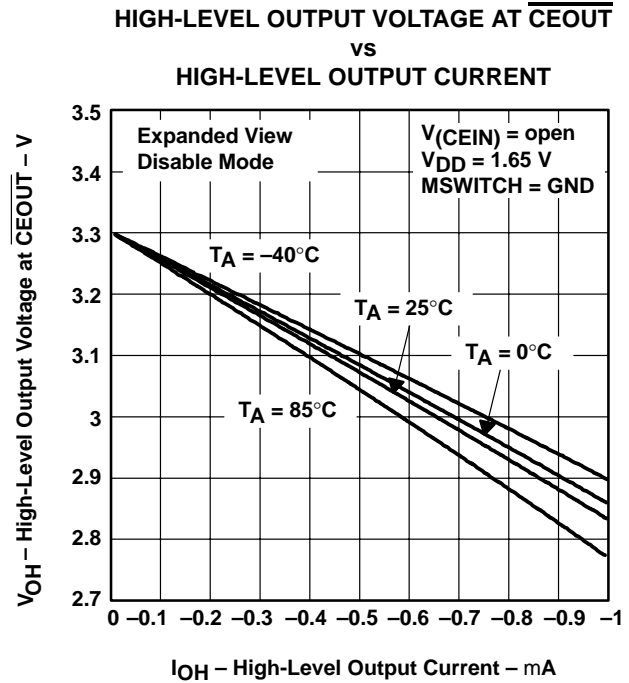
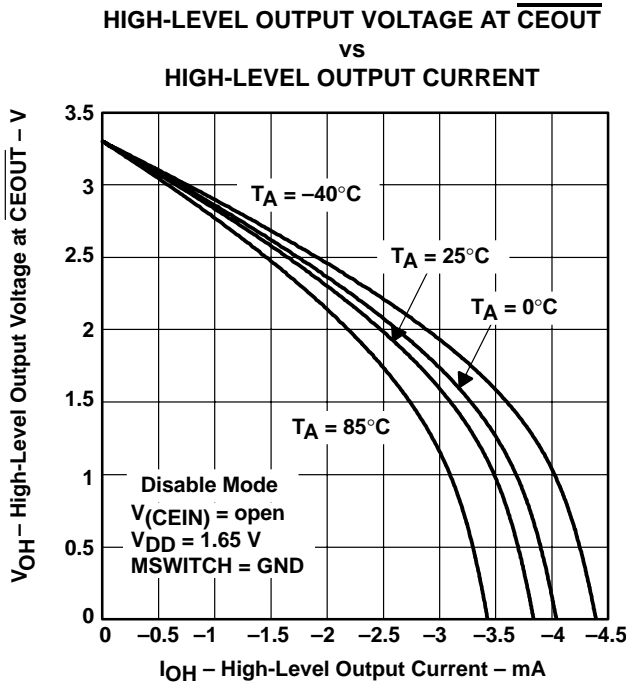


Figure 16

TPS3610U18, TPS3610T50 BATTERY-BACKUP SUPERVISORS FOR RAM RETENTION

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

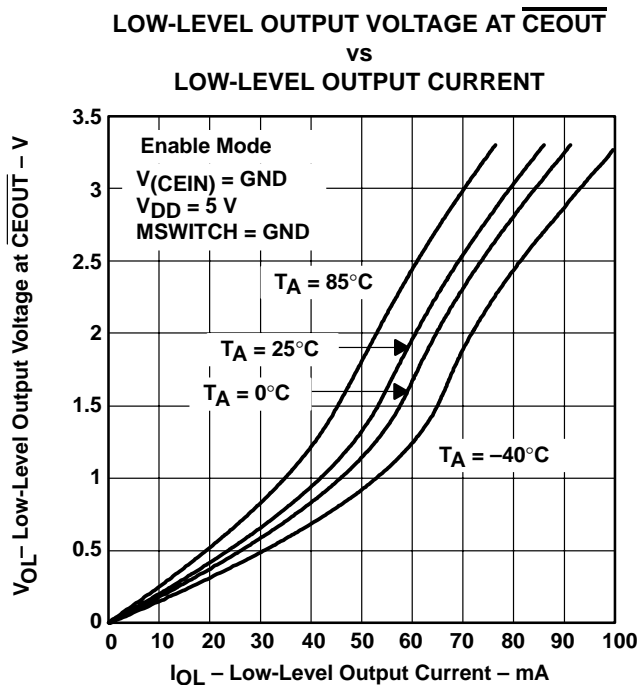


Figure 21

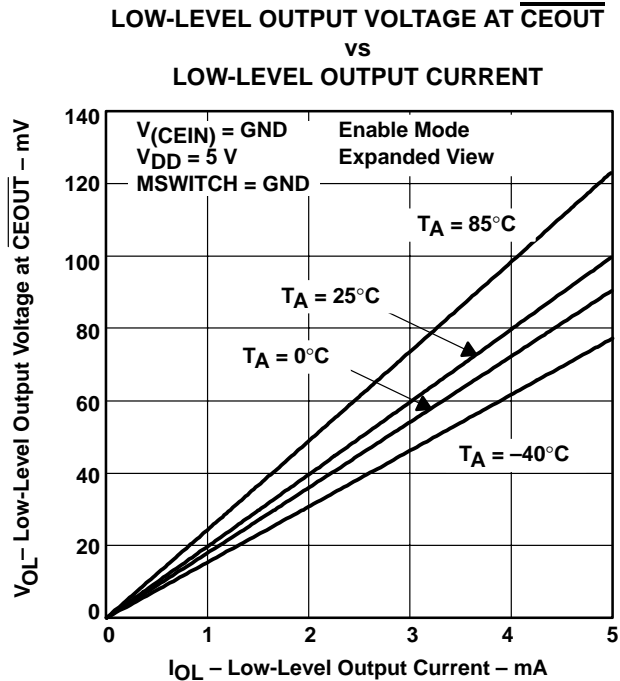


Figure 22

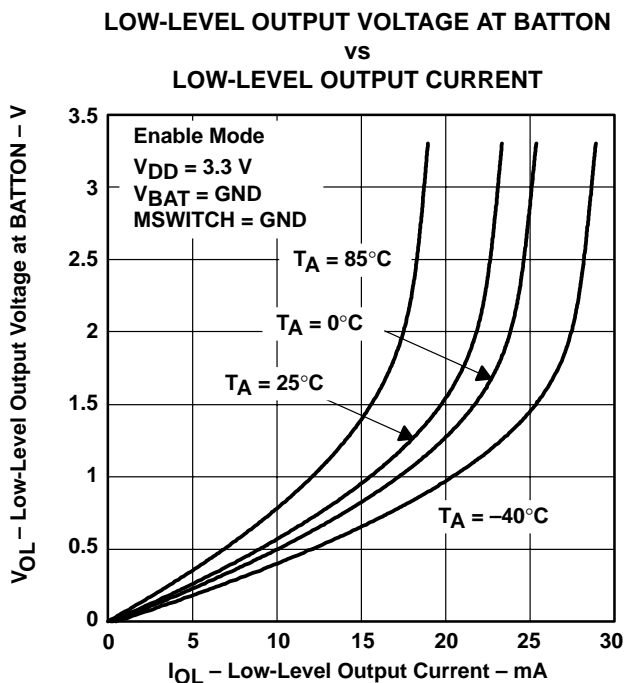


Figure 23

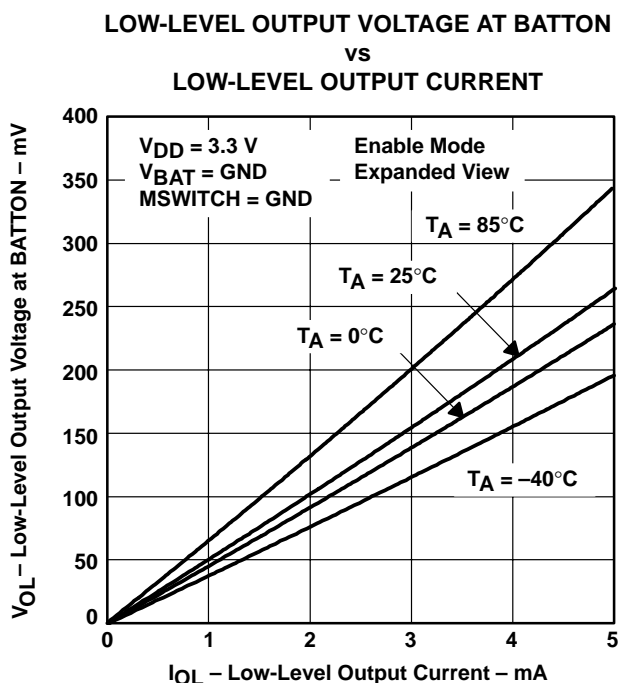


Figure 24

TPS3610U18, TPS3610T50 BATTERY-BACKUP SUPERVISORS FOR RAM RETENTION

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TYPICAL CHARACTERISTICS

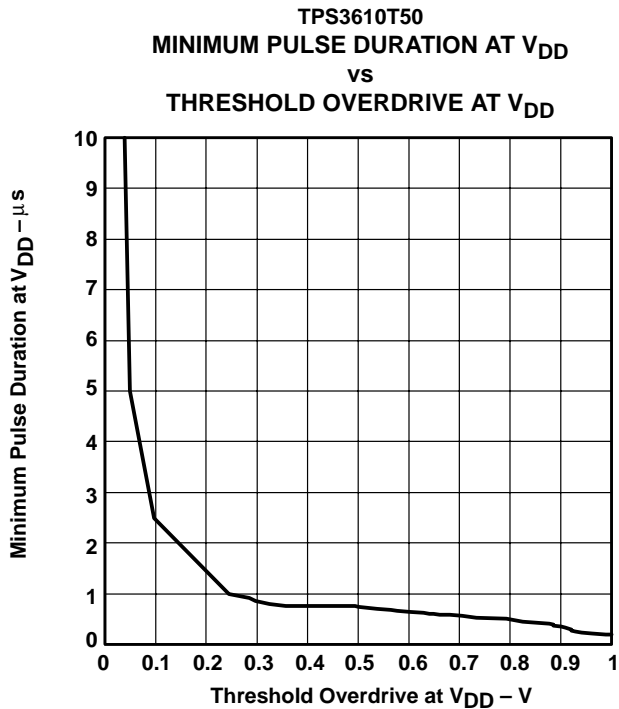


Figure 25

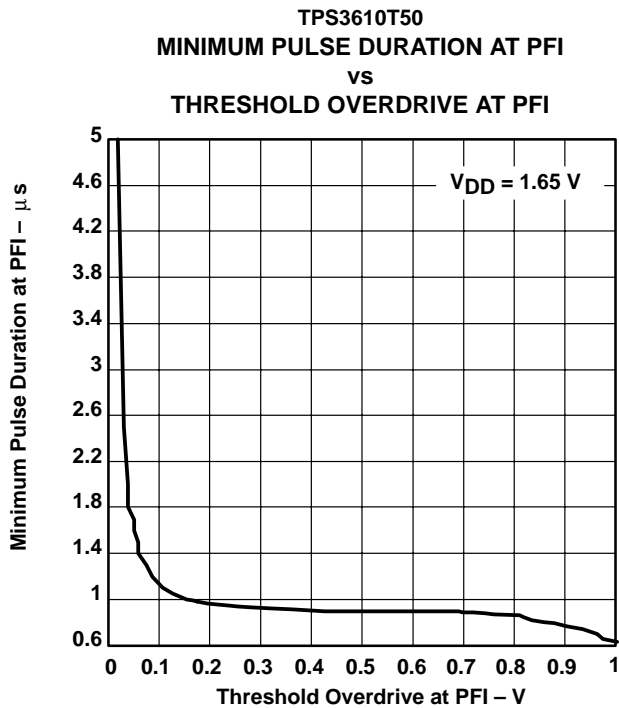


Figure 26



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3610T50PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3610T50	Samples
TPS3610T50PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3610T50	Samples
TPS3610T50PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3610T50	Samples
TPS3610T50PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3610T50	Samples
TPS3610U18PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3610U18	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

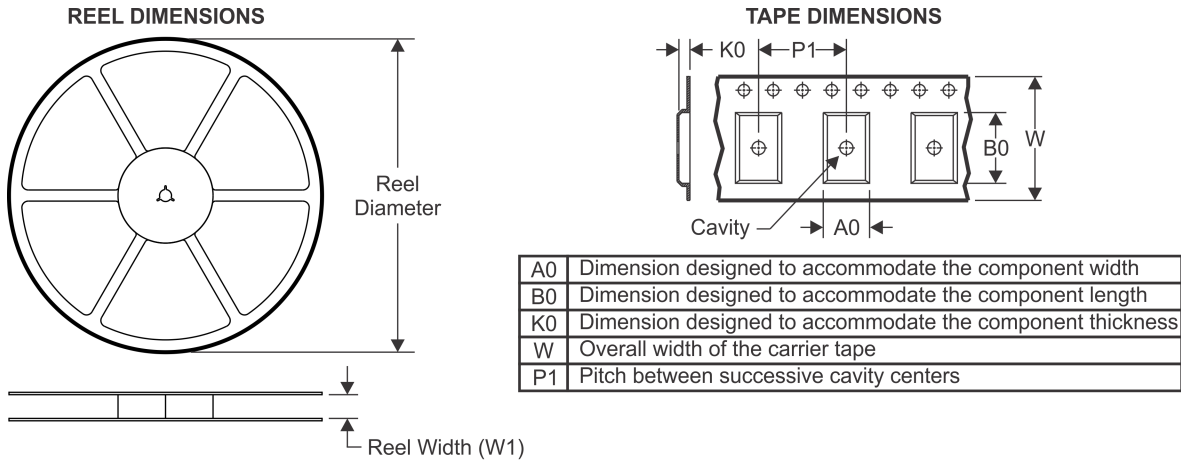
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3610T50PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

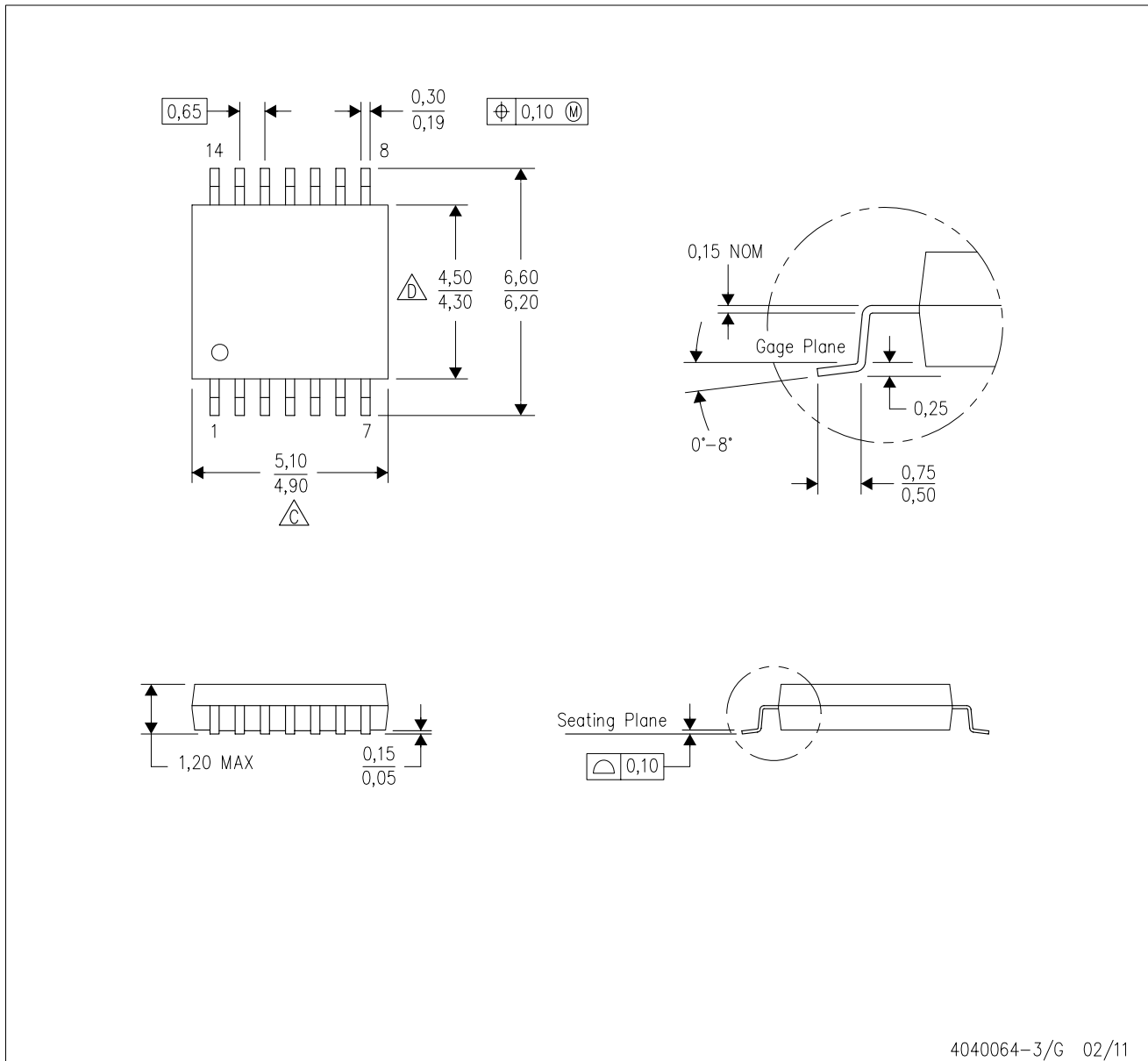


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3610T50PWR	TSSOP	PW	14	2000	340.5	338.1	20.6

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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