Document Number: MD7IC18120N
Rev. 0, 5/2010

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MD7IC18120NR1
MD7IC18120GNR1

1805–1880 MHz, 30 W AVG., 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

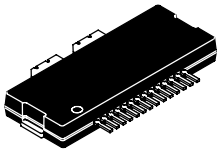
The MD7IC18120N/GN wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 1880 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats.

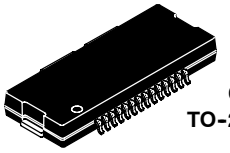
- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1A} = 70 mA, I_{DQ1B} = 160 mA, I_{DQ2B} = 500 mA, V_{GS2A} = 1.7 Vdc, P_{out} = 30 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)
1805 MHz	25.7	36.7	6.9
1840 MHz	25.7	36.3	6.9
1880 MHz	25.8	35.3	6.7

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1840 MHz, 140 Watts CW Output Power
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 100 Watts CW P_{out}
- Typical P_{out} @ 1 dB Compression Point ≃ 120 Watts CW

CASE 1866-02
TO-270 WBL-16
PLASTIC
MD7IC18120NR1





CASE 1867-02
TO-270 WBL-16 GULL
PLASTIC
MD7IC18120GNR1

Features

- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Large-Signal Load-Pull Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

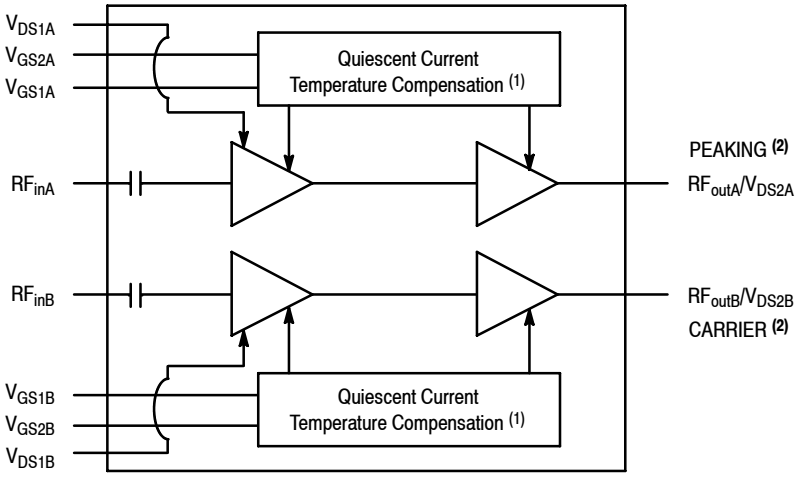
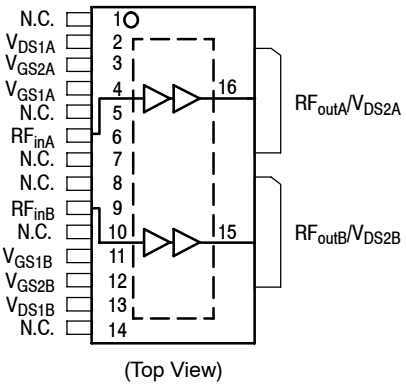


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.
2. Peaking and Carrier orientation is determined by the test fixture design.

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	175 1.5	W W/°C
Input Power	P_{in}	30	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Final Doherty Application			
Thermal Resistance, Junction to Case Case Temperature 78°C, P_{out} = 30 W CW, 1880 MHz Stage 1A, 28 Vdc, I_{DQ1A} = 70 mA Stage 1B, 28 Vdc, I_{DQ1B} = 160 mA Stage 2A, 28 Vdc, V_{G2A} = 1.7 Vdc Stage 2B, 28 Vdc, I_{DQ2B} = 500 mA	$R_{\theta JC}$	 4.5 4.5 0.88 0.88	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics (1)						
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	1	μAdc
Stage 1 — On Characteristics (1)						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 28 μAdc)		$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 70 mA, I_{DQ1B} = 160 mA)		$V_{GS(Q)}$	—	2.9	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, Measured in Functional Test)	I_{DQ1A} = 70 mA I_{DQ1B} = 160 mA	$V_{GG(Q)}$	4.0 7.1	5.0 8.1	6.0 9.1	Vdc
Stage 2 — Off Characteristics (1)						
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	1	μAdc
Stage 2 — On Characteristics (1)						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 185 μAdc)		$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2B} = 500 mA)		$V_{GS(Q)}$	—	2.6	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2B} = 500 mA, Measured in Functional Test)		$V_{GG(Q)}$	5.3	6.3	7.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.8 Adc)		$V_{DS(on)}$	—	0.35	—	Vdc

Functional Tests (2,3,4) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 70 mA, I_{DQ1B} = 160 mA, I_{DQ2B} = 500 mA, V_{GS2A} = 1.7 Vdc, P_{out} = 30 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	24.0	25.8	28.0	dB
Power Added Efficiency	PAE	33.0	35.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.0	6.7	—	dB

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in a Symmetrical Doherty configuration.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Typical Broadband Performance (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 70 mA, I_{DQ1B} = 160 mA, I_{DQ2B} = 500 mA, V_{GS2A} = 1.7 Vdc, P_{out} = 30 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)
1805 MHz	25.7	36.7	6.9
1840 MHz	25.7	36.3	6.9
1880 MHz	25.8	35.3	6.7

Typical Performances (1) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 70 mA, I_{DQ1B} = 160 mA, I_{DQ2B} = 500 mA, V_{GS2A} = 1.7 Vdc, 1805–1880 MHz Bandwidth

Characteristic		Symbol	Min	Typ	Max	Unit
P_{out} @ 1 dB Compression Point, CW		P1dB	—	120	—	W
IMD Symmetry @ 30 W PEP, P_{out} where IMD Third Order Intermodulation ≧ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)		IMD_{sym}	—	15	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)		VBW_{res}	—	35	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 30 W Avg.		G_F	—	0.3	—	dB
Quiescent Current Accuracy over Temperature with 2 kΩ Gate Feed Resistors (-30 to 85°C) (2)	Stage 1 Stage 2	ΔI_{QT}	—	4.26 5.04	—	%
Gain Variation over Temperature (-30°C to +85°C)		ΔG	—	0.04	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)		ΔP1dB	—	0.04	—	dBm/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

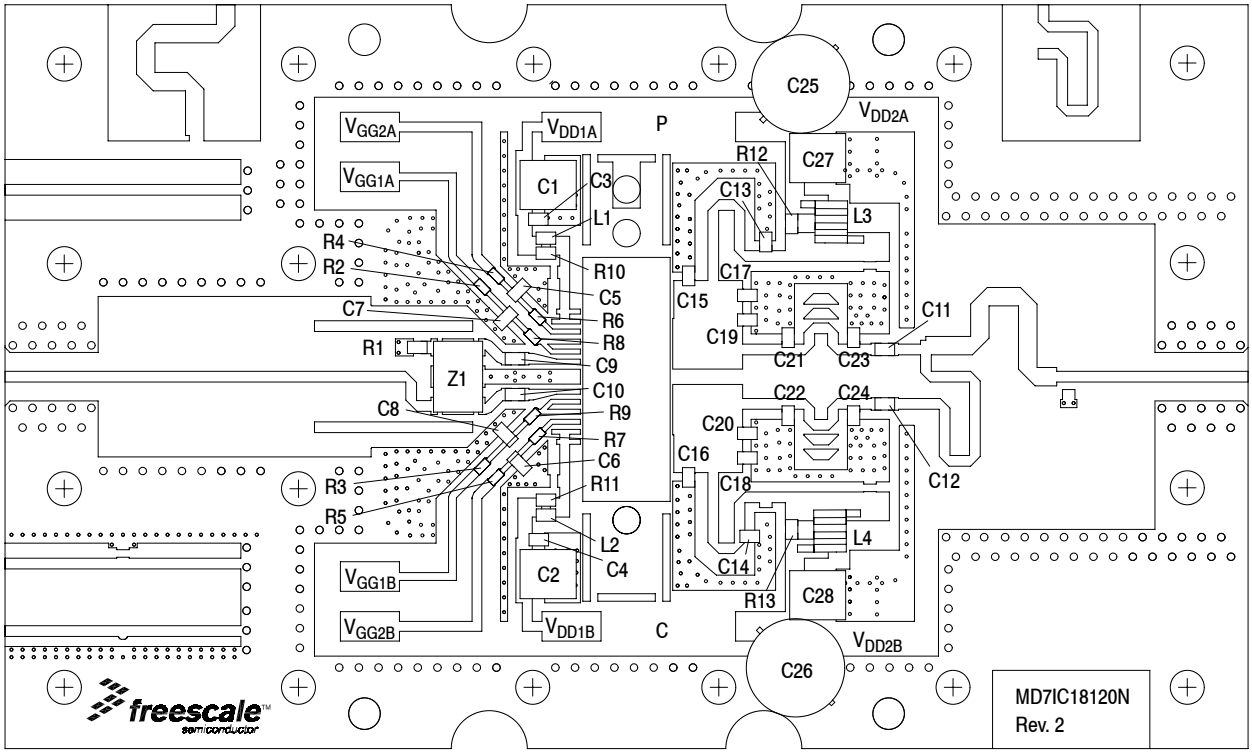


Figure 3. MD7IC18120NR1(GNR1) Test Circuit Component Layout

Table 6. MD7IC18120NR1(GNR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C27, C28	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C3, C4, C5, C6, C7, C8	0.1 μF Chip Capacitors	GRM21BR71H104KA01B	Murata
C9, C10, C11, C13, C14	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C12	100 pF Chip Capacitor	ATC600F101JT250XT	ATC
C15, C16, C17, C18	2.2 pF Chip Capacitors	ATC600F2R2BT250XT	ATC
C19, C20	1.5 pF Chip Capacitors	ATC600F1R5BT250XT	ATC
C21, C22, C23	1.0 pF Chip Capacitors	ATC600F1R0BT250XT	ATC
C24	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C25, C26	330 μF, 35 V Electrolytic Capacitors	MCGPR35V337M10X16-RH	Panasonic
L1, L2	6.8 nH Chip Inductors	0805CS-060XJLB	CoilCraft
L3, L4	2.5 nH, 1 Turn Inductors	A01TKLC	CoilCraft
R1	50 Ω, 1/8 W Chip Resistor	SG732ATTDD51R0F	KOA Speer
R2, R3, R4, R5, R6, R7, R8, R9	1000 Ω, 1/10 W Chip Resistors	SG731JTTDD1001F	KOA Speer
R10, R11, R12, R13	10 Ω, 1/10 W Chip Resistors	CRCW060310R0FKEA	Vishay
Z1	1900 MHz Band 90°, 3 dB Chip Hybrid Coupler	GSC351-HYB1900	SOSHIN
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

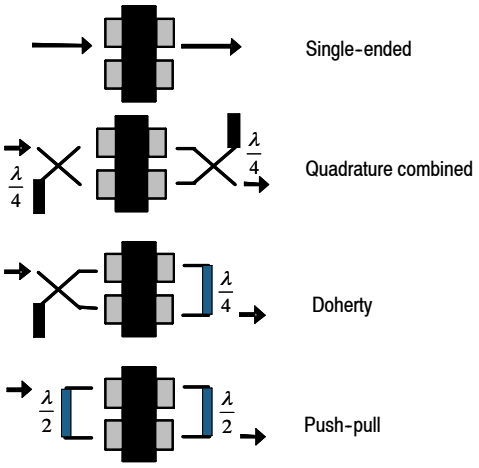


Figure 4. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

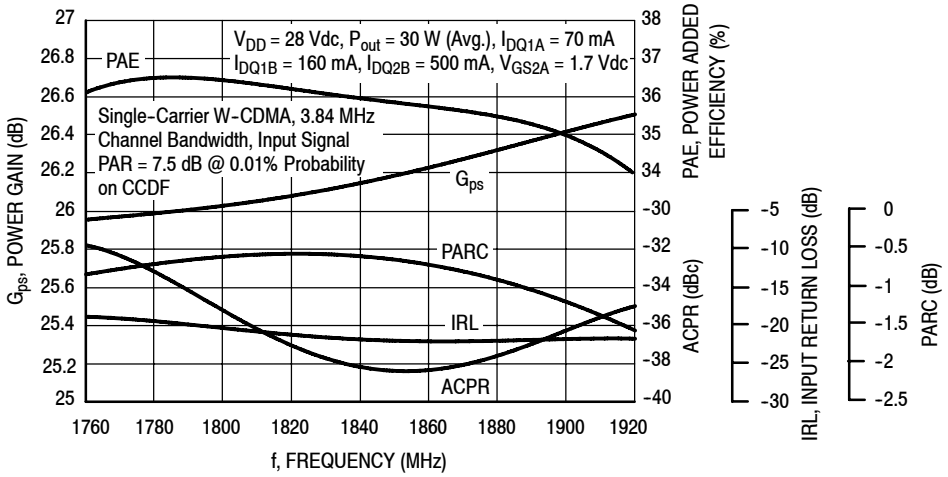


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 30 Watts Avg.

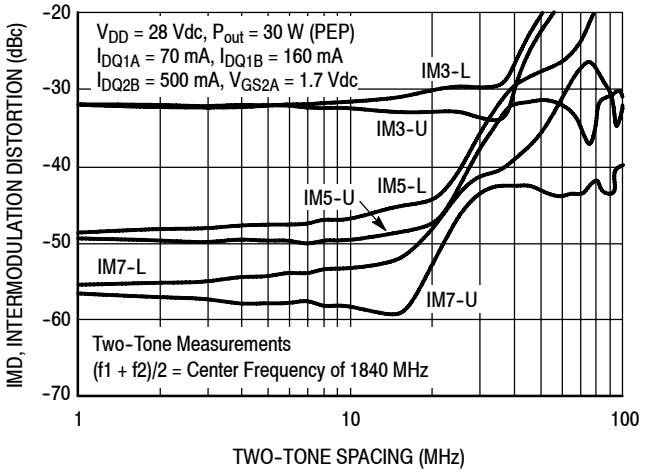


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

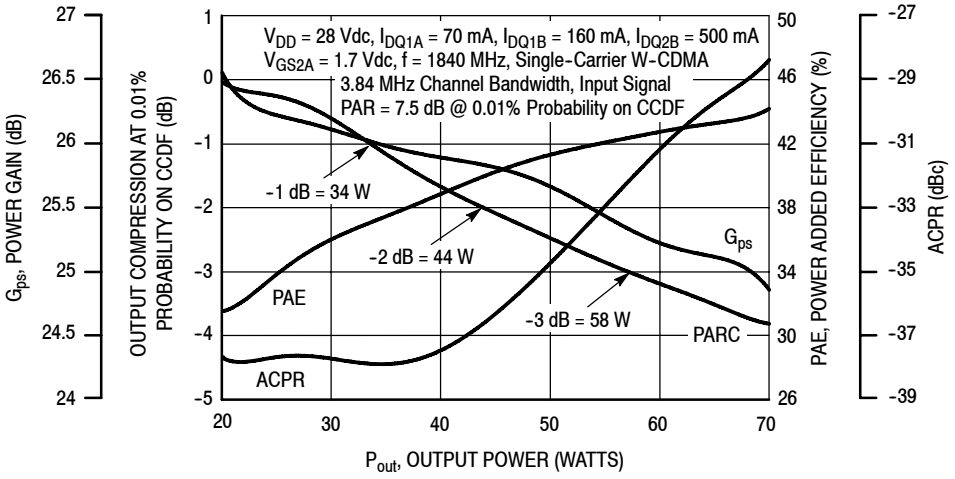


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

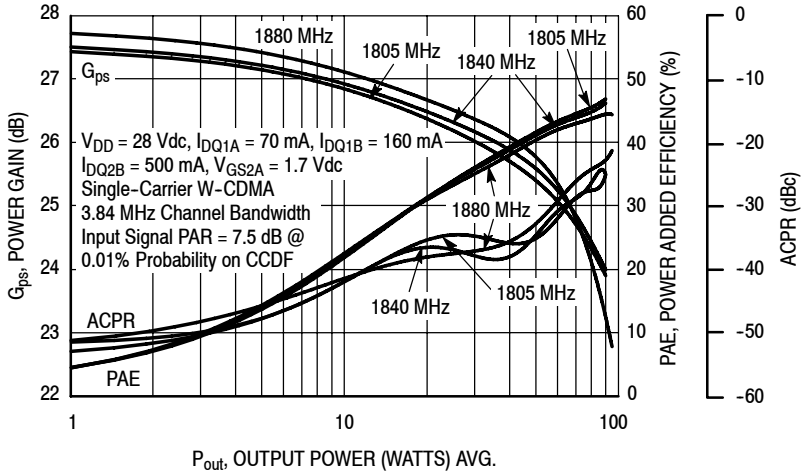


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

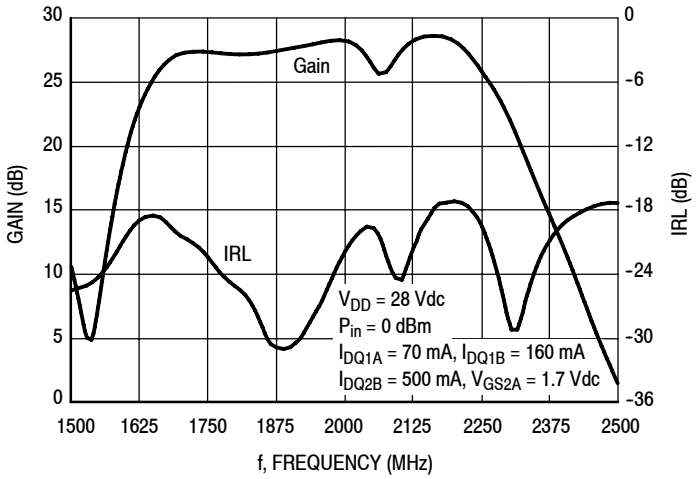


Figure 9. Broadband Frequency Response

W-CDMA TEST SIGNAL

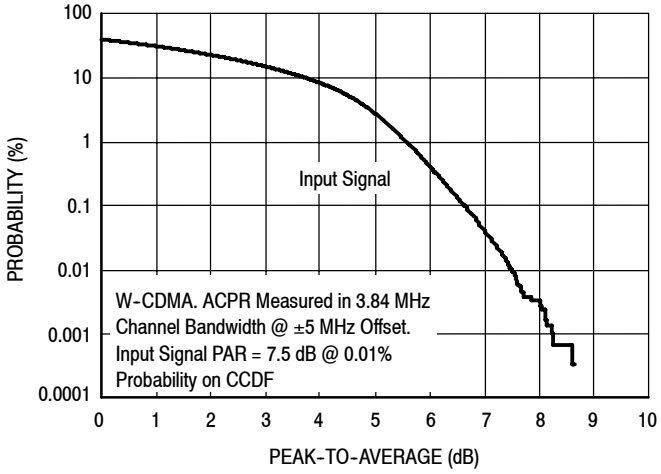


Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

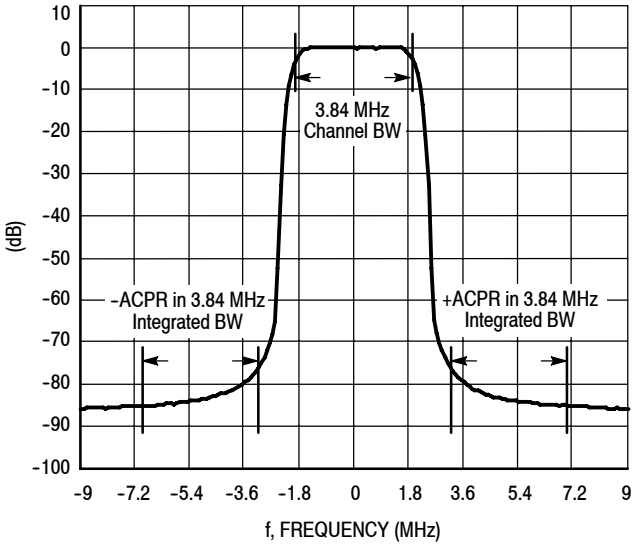


Figure 11. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ1B} = 120 mA, I_{DQ2B} = 450 mA

f MHz	Max P_{out} (1) Watts	Max P_{out} (1) dBm	Z_{in} Ω	Z_{load} Ω
1805	68	48.3	56.20 + j3.50	2.79 – j5.39
1840	69	48.4	60.80 – j6.10	2.81 – j5.45
1880	74	48.7	57.90 – j12.00	2.41 – j5.63

(1) Maximum output power measurement reflects pulsed 1 dB gain compression.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

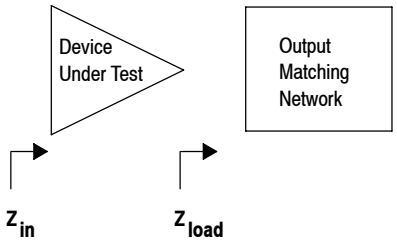


Figure 12. Maximum Output Power — Doherty Load Pull Optimization for Carrier Side

V_{DD} = 28 Vdc, I_{DQ1B} = 120 mA, I_{DQ2B} = 450 mA

f MHz	Max Eff. (1) %	Z_{in} Ω	Z_{load} Ω
1805	53.3	56.20 + j3.50	4.10 – j4.49
1840	53.4	60.80 – j6.10	3.74 – j4.54
1880	54.0	57.90 – j12.00	3.65 – j4.55

(1) Maximum efficiency measurement reflects pulsed 1 dB gain compression.

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

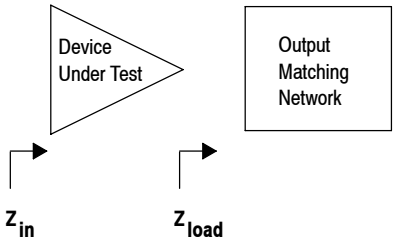
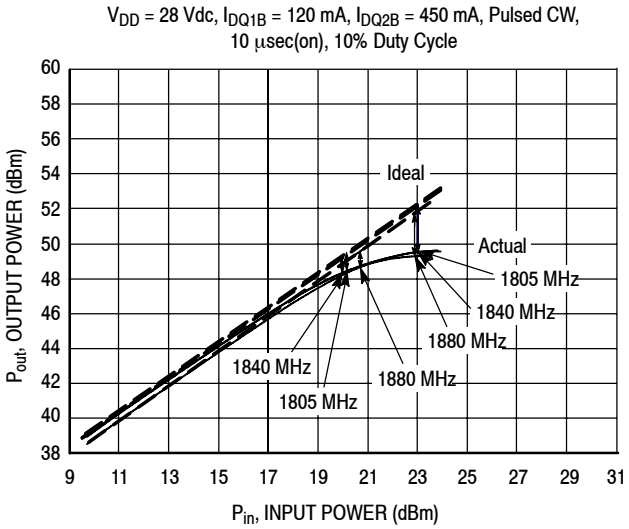


Figure 13. Maximum Efficiency — Doherty Load Pull Optimization for Carrier Side

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
1805	70	48.5	89	49.5
1840	69	48.4	89	49.5
1880	74	48.7	85	49.3

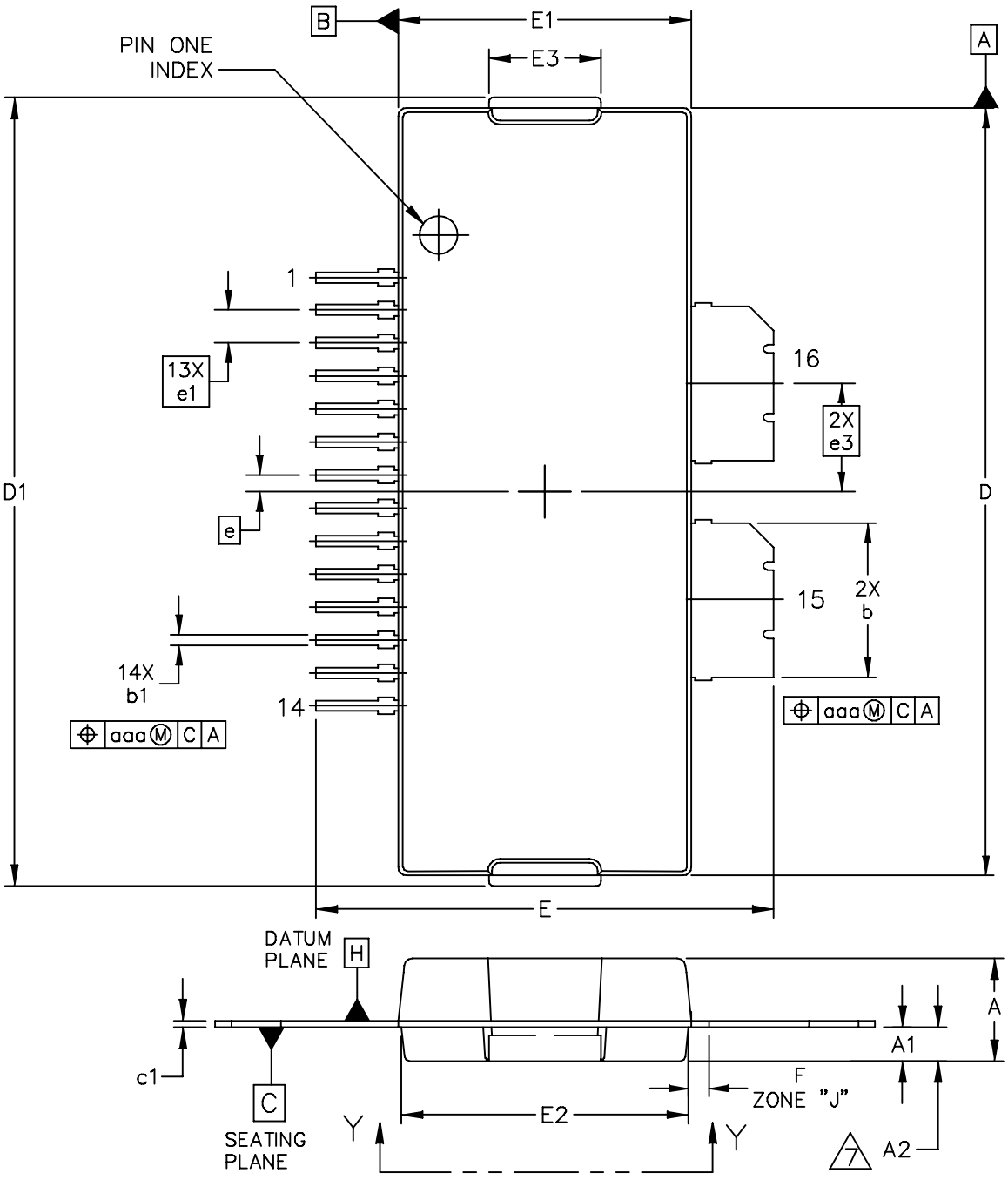
Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
1805	P1dB	56.20 – j3.50	2.80 – j5.40
1840	P1dB	60.80 + j6.10	2.80 – j5.40
1880	P1dB	57.90 + j12.00	2.40 – j5.60

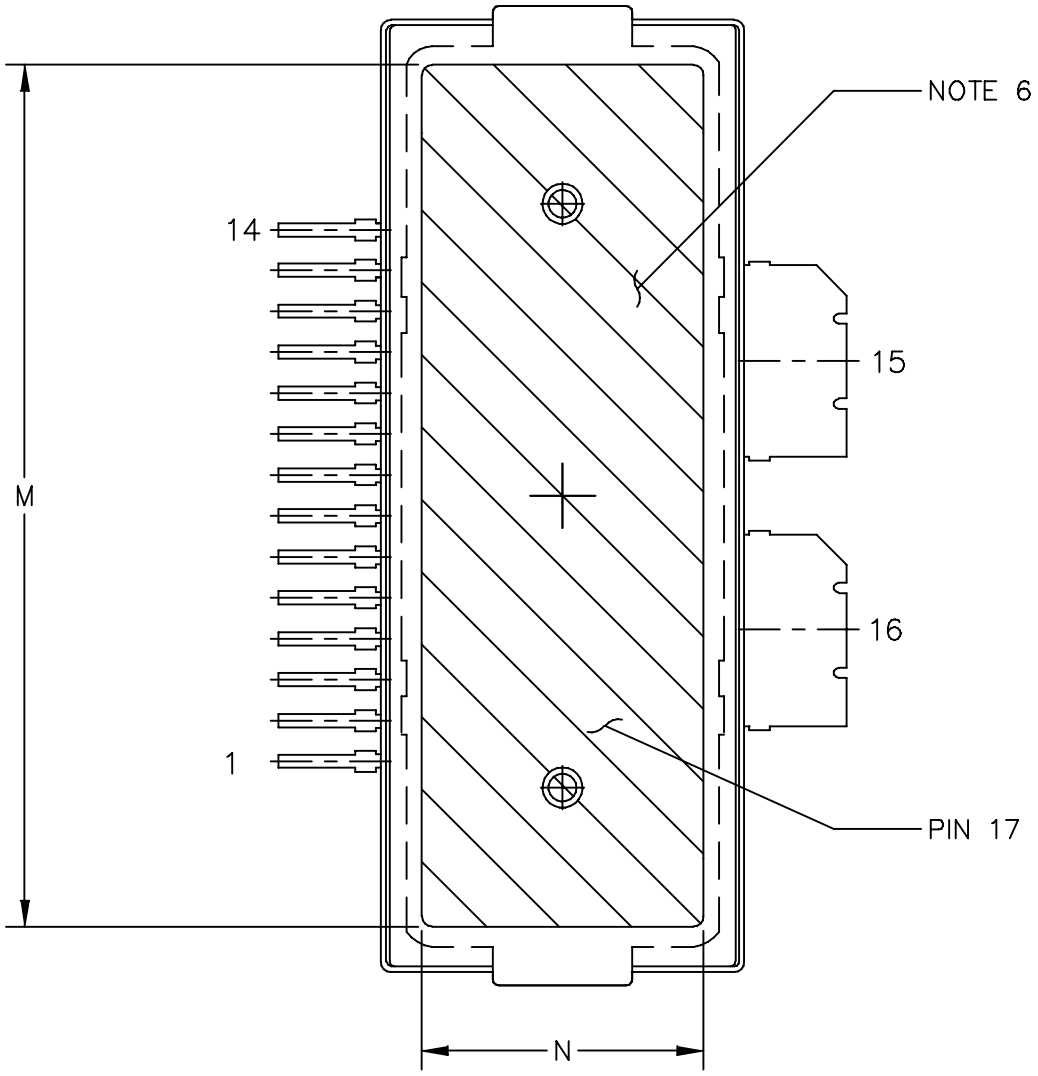
Figure 14. Pulsed CW Output Power versus Input Power @ 28 V

NOTE: Measurement made on the Class AB, carrier side of the device.

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC	DOCUMENT NO: 98ASA10739D	REV: A
	CASE NUMBER: 1866-02	02 AUG 2007
	STANDARD: NON-JEDEC	



VIEW Y–Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 WIDE BODY LONG, 16 LEAD, PLASTIC	DOCUMENT NO: 98ASA10739D	REV: A
	CASE NUMBER: 1866–02	02 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

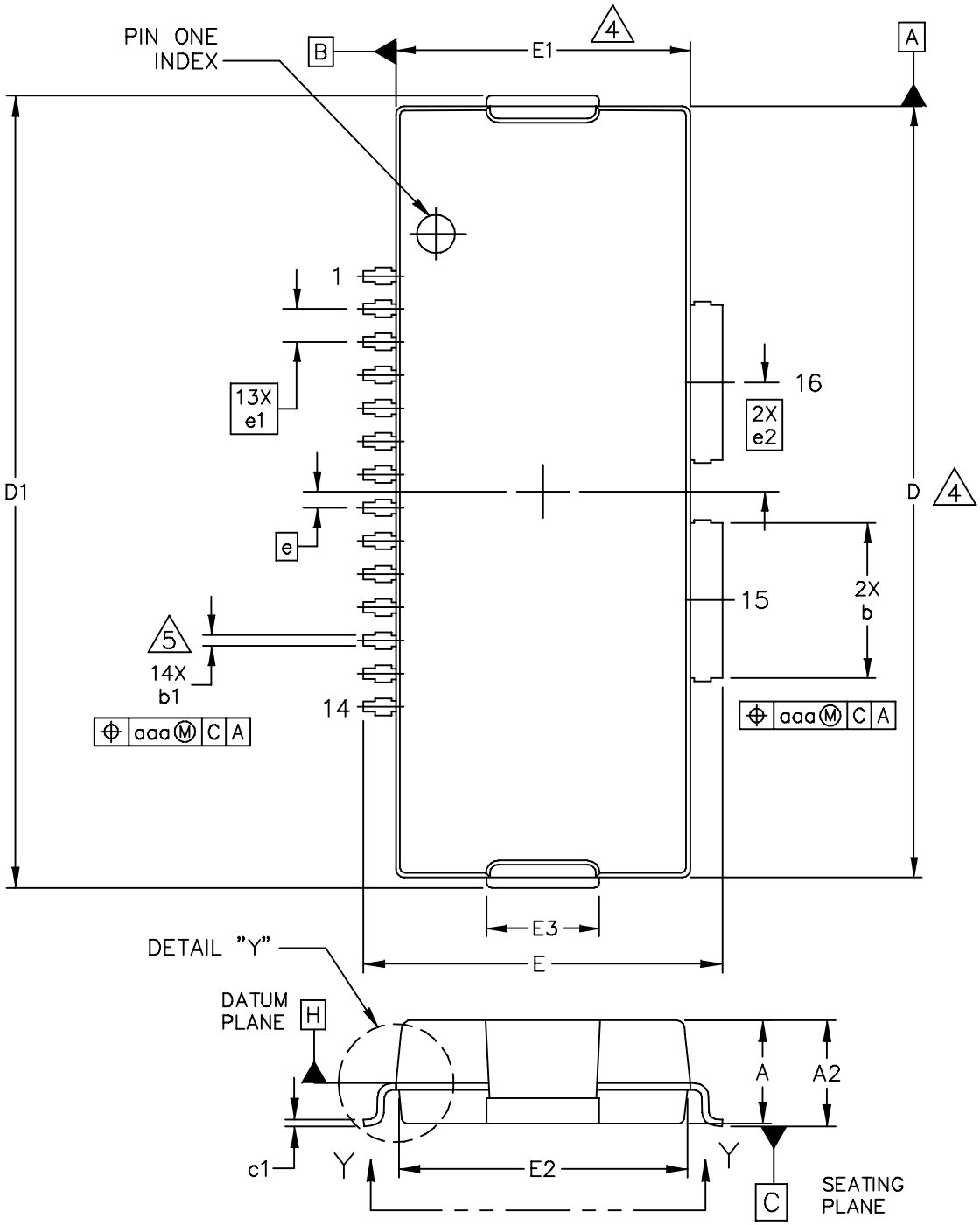
6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

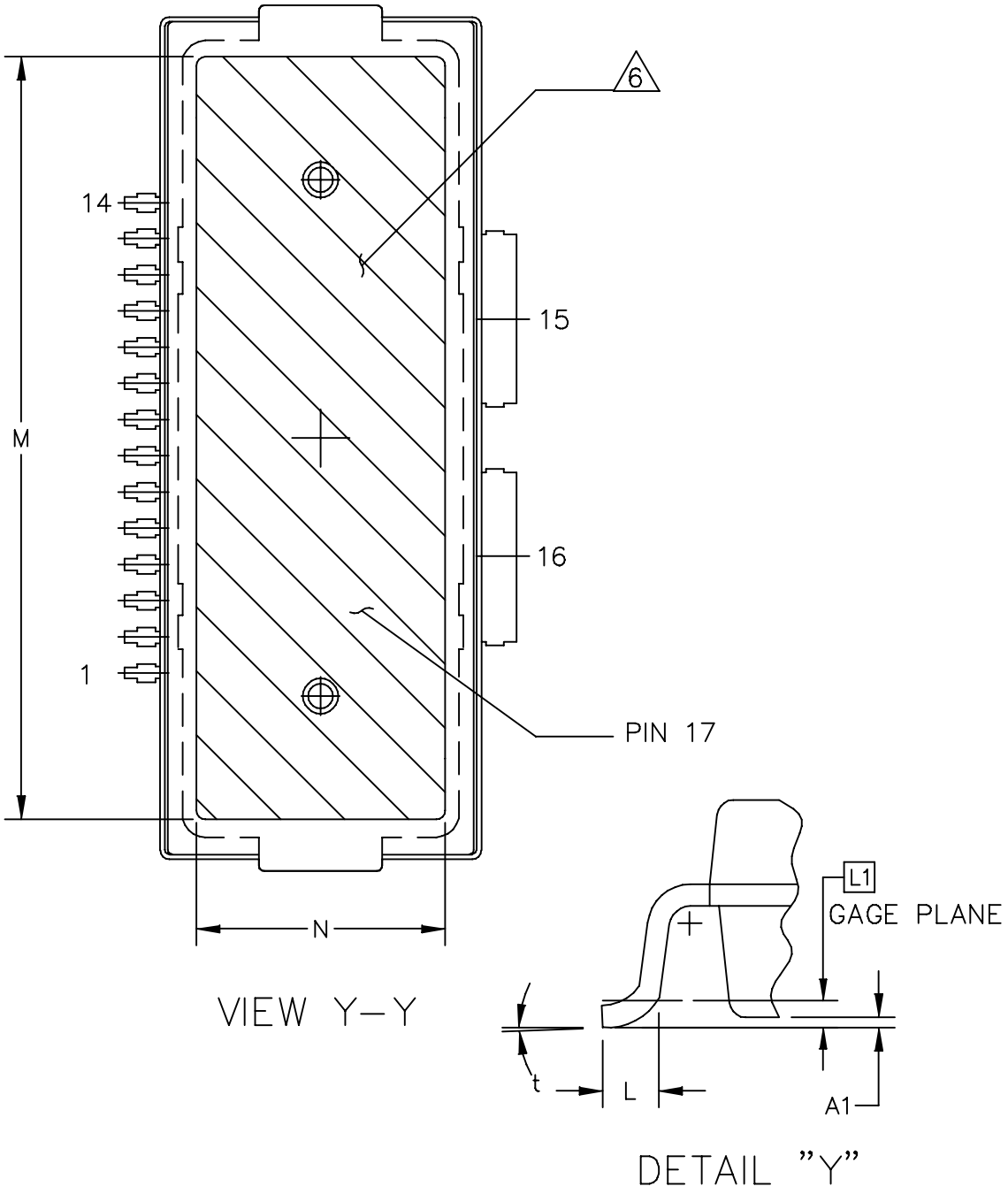
DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.122	.128	3.10	3.25	M	.800	----	20.32	----
A1	.039	.043	0.96	1.12	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	b	.184	.190	4.67	4.83
D	.928	.932	23.57	23.67	b1	.010	.016	0.25	0.41
D1	.954	.958	24.23	24.33	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e3	.131 BSC		3.33 BSC	
E3	.132	.140	3.35	3.56					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10739D	REV: A
TO–270 WIDE BODY LONG, 16 LEAD, PLASTIC	CASE NUMBER: 1866–02	02 AUG 2007
	STANDARD: NON–JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC	DOCUMENT NO: 98ASA10740D	REV: A
	CASE NUMBER: 1867-02	02 AUG 2007
	STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC	DOCUMENT NO: 98ASA10740D	REV: A
	CASE NUMBER: 1867–02	02 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.122	.128	3.10	3.25	b	.184	.190	4.67	4.83
A1	.001	.004	0.02	0.10	b1	.010	.016	0.25	0.41
A2	.125	.131	3.18	3.33	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.954	.958	24.23	24.33	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.131 BSC		3.33 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.346	.350	8.79	8.89	aaa	.004		0.10	
E3	.132	.140	3.35	3.56					
L	.018	.024	0.46	0.61					
L1	.01 BSC		0.25 BSC						
M	.800	----	20.32	----					
N	.270	----	6.86	----					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10740D	REV: A
TO–270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC	CASE NUMBER: 1867–02	02 AUG 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2010	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MD7IC18120N
Rev. 0, 5/2010