Revision History

Revision 0.1 (Oct. 2011) -First release.

Revision 0.2 (Apr. 2012)

- Update package dimension to 8 x 10.5 mm2.

Revision 0.3 (Sep. 2013)

- Add package dimension 7.5 x 10.6 mm2.

Revision 0.4 (Mar. 2014)

- Add DDR3 speed 1866.

Revision 0.5 (Jul. 2014)

- Add Package dimension 9 x 10.5 mm2.

2Gb (32M×8Bank×8) Double DATA RATE 3 low voltage SDRAM

Features

- JEDEC Standard VDD/VDDQ = 1.5V±0.075V
- All inputs and outputs are compatible with SSTL_15 interface.
- Fully differential clock inputs (CK, /CK) operation.
- Eight Banks
- Posted CAS by programmable additive latency
- Bust length: 4 with Burst Chop (BC) and 8.
- CAS Write Latency (CWL): 5, 6, 7, 8, 9, 10
- CAS Latency (CL): 6, 7, 8, 9, 10, 11, 12, 13
- Write Latency (WL) =Read Latency (RL) -1.
- Bi-directional Differential Data Strobe (DQS).
- Data inputs on DQS centers when write.
- Data outputs on DQS, /DQS edges when read.
- On chip DLL align DQ, DQS and /DQS transition with CK transition.
- DM mask write data-in at the both rising and falling edges of the data strobe.
- Sequential & Interleaved Burst type available both for 8 & 4 with BC.
- Multi Purpose Register (MPR) for pre-defined pattern read out
- On Die Termination (ODT) options: Synchronous ODT, Dynamic ODT, and Asynchronous ODT
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms
- Refresh Interval: 7.8us T_{case} between 0˚C ~ 85˚C
- Refresh Interval: 3.9us Tcase between 85°C ~ 95°C
- RoHS Compliance
- Driver Strength: RZQ/7, RZQ/6(RZQ=240Ω)
- High Temperature Self-Refresh rate enable
- ZQ calibration for DQ drive and ODT
- RESET pin for initialization and reset function

Description

The EM47EM0888SBA is a high speed Double Date Rate 3 (DDR3) low voltage Synchronous DRAM fabricated with ultra high performance CMOS process containing 2,147,483,648 bits which organized as 32Mbits x 8 banks by 8 bits. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin (DDR3-1866) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) On Die Termination, (4) programmable driver strength data,(5) seamless BL4 access with bank-grouping. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style. The 2Gb DDR3 devices operates with a single power supply: 1.5V±0.075V VDD and VDDQ. Available package: FBGA-78Ball (with 0.8mm x 0.8mm ball pitch)

Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Package size
EM47EM0888SBA-150	256M x 8	DDR3-1333 (9-9-9)	FBGA-78B	Commercial	8x10.5mm
EM47EM0888SBA-125	256M x 8	DDR3-1600 (11-11-11)	FBGA-78B	Commercial	8x10.5mm
EM47EM0888SBA-107	256M x 8	DDR3-1866 (13-13-13)	FBGA-78B	Commercial	8x10.5mm
EM47EM0888SBA-150A	256M x 8	DDR3-1333 (9-9-9)	FBGA-78B	Commercial	7.5x10.6mm
EM47EM0888SBA-125A	256M x 8	DDR3-1600 (11-11-11)	FBGA-78B	Commercial	7.5x10.6mm
EM47EM0888SBA-107A	256M x 8	DDR3-1866 (13-13-13)	FBGA-78B	Commercial	7.5x10.6mm
EM47EM0888SBA-150B	256M x 8	DDR3-1333 (9-9-9)	FBGA-78B	Commercial	9x10.5mm
EM47EM0888SBA-125B	256M x 8	DDR3-1600 (11-11-11)	FBGA-78B	Commercial	9x10.5mm
EM47EM0888SBA-107B	256M x 8	DDR3-1866 (13-13-13)	FBGA-78B	Commercial	9x10.5mm
EM47EM0888SBA-150E	256M x 8	DDR3-1333 (9-9-9)	FBGA-78B	Commercial	8x10.5mm
EM47EM0888SBA-125E	256M x 8	DDR3-1600 (11-11-11)	FBGA-78B	Commercial	8x10.5mm
EM47EM0888SBA-107E	256M x 8	DDR3-1866 (13-13-13)	FBGA-78B	Commercial	8x10.5mm

Note: Speed (t_{CK} *) is in order of CL-t_{RCD}-t_{RP}

Pin Assignment: Top View

1	2	3		7	8	9
VSS	VDD	NC	A	NC, /TDQS	VSS	VDD
VSS	VSSQ	DQ0	B	DM, TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS	C	DQ1	DQ3	VSSQ
VSSQ	DQ6	/DQS	D	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	E	DQ7	DQ5	VDDQ
NC	VSS	/RAS	F	CK	VSS	NC
ODT	VDD	/CAS	G	/CK	VDD	CKE
NC	/CS	/WE	H	A10, AP	ZQ	NC
VSS	BA0	BA2	J	NC	VREFCA	VSS
VDD	A3	A0	K	A12, /BC	BA1	VDD
VSS	A5	A2	L	A1	A4	VSS
VDD	A7	A9	M	A11	A6	VDD
VSS	/RESET	A13	N	A14	A8	VSS

78 Ball FBGA

Pin Description (Simplified)

Pin	Name	Function
F7,G7	CK, /CK	**(System Clock)** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK . Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
H2	/CS	**(Chip Select)** All commands are masked when /CS is registered HIGH. /CS provides for external Rank selection on systems with multiple Ranks. /CS is considered part of the command code.
G9	CKE	**(Clock Enable)** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self- refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including self-refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self -refresh.
K3,L7,L3,K2, L8,L2,M8,M2, N8,M3,H7,M7, K7,N3,N7,J7	A0~A9,A10(AP), A11,A12(/BC), A13,A14,A15	**(Address)** Provided the row address (RA0 – RA15) for active commands and the column address (CA0-CA9) and auto precharge bit for read/write commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during Mode Register Set commands. A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop, LOW: burst chopped). See command truth table for details.
J2,K8,J3	BA0, BA1,BA2	**(Bank Address)** BA0 – BA2 define to which bank an active, read, write or precharge command is being applied. Bank address also determines if the mode register is to be accessed during a MRS cycle.
G1	ODT	**(On Die Termination)** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS , DM/TDQS, and TDQS signal. The ODT pin will be ignored if the Mode Register ***MR1*** is programmed to disable ODT.

Pin Description (Continued)

C3,D3	DQS, /DQS	**(Data Strobe)** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signal /DQS to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
B7,A7	TDQS, /TDQS	**(Termination Data Strobe)** When enabled via Mode Register A11=1 in ***MR1***, DRAM will enable the same termination resistance function on TDQS /TDQS that is applied to DQS/DQS. When disabled via mode register A11=0 in ***MR1***, DM/TDQS will provide the data mask function and /TDQS is not used.
F3, G3, H3	/RAS , /CAS , /WE	**(Command Inputs)** /RAS , /CAS and /WE (along with /CS) define the command being entered.
B3,C7,C2,C8,E3, E8,D2,E7	DQ0~7	**(Data Input/Output)** Data inputs and outputs are on the same pin.
A2,A9,D7,G2,G8, K1,K9,M1,M9/A1, A8,B1,D8,F2,F8,J1 ,J9,L1,L9,N1,N9	VDD,VSS	**(Power Supply/Ground)** VDD and VSS are power supply for internal circuits.
B9,C1,E2,E9 /B2,B8,C9,D1,D9	VDDQ ,VSSQ	**(DQ Power Supply/DQ Ground)** VDDQ and VSSQ are power supply for the output buffers.
H8	ZQ	**(ZQ Calibration)** Reference pin for ZQ calibration
N2	/RESET	**(Active Low Asynchronous Reset)** Reset is active when /RESET is LOW, and inactive when /RESET is HIGH. /RESET must be HIGH during normal operation. /RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
E1	VREFDQ	**(Reference Voltage)** Reference voltage for DQ
J8	VREFCA	**(Reference Voltage)** Reference voltage for CA
A3,F1,H1,F9, H9	NC	**(No Connection)** No internal electrical connection is present.

Note: Input pins only BA0-BA2, A0-A15, /RAS , /CAS , /WE , /CS , CKE, ODT and /RESET do not supply termination.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.4 ~ +1.975		V
V_{DD}	Power Supply Voltage	-0.4 ~ +1.975		V
V_{DDQ}	Power Supply Voltage	-0.4 ~ +1.975		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +95	°C
		Extended	-25 ~ +95	
T_{STG}	Storage Temperature Range	-55 ~ +100		°C

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Power Supply for I/O Voltage	1.425	1.5	1.575	V

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	Min.	Max.	Units
V_{IHCA} (DC100)	DC input logic high	VREF+0.100	VDD	V
V_{ILCA} (DC100)	DC input logic low	VSS	VREF-0.100	V
V_{IHCA} (AC175)	AC input logic high	VREF+0.175	-	V
V_{ILCA} (AC175)	AC input logic low	-	VREF-0.175	V
V_{IHCA} (AC150)	AC input logic high	VREF+0.150	-	V
V_{ILCA} (AC150)	AC input logic low	-	VREF-0.150	V
V_{REFCA} (DC)	Reference voltage for ADD, CMD	0.49*VDD	0.51*VDD	V

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min.	Max.	Units
V_{IHDQ} (DC100)	DC input logic high	VREF+0.100	VDD	V
V_{ILDQ} (DC100)	DC input logic low	VSS	VREF-0.100	V
V_{IHDQ} (AC175)	AC input logic high	-	-	V
V_{ILDQ} (AC175)	AC input logic low	-	-	V
V_{IHDQ} (AC150)	AC input logic high	VREF+0.150	-	V
V_{ILDQ} (AC150)	AC input logic low	-	VREF-0.150	V
V_{REFDQ} (DC)	Reference voltage for DQ, DM	0.49*VDD	0.51*VDD	V

Note1. For input pins except /RESET: VREF= V_{REFCA} (DC) or VREF= V_{REFDQ} (DC).

Note2. The AC peak noise on VREF may not allow VREF to deviate from V_{REFCA} (DC) or VREF= V_{REFDQ} (DC) by more than ±1% VDD (for reference: approx. ±15mV.

Note3. For reference voltage = VDD/2 ±15mV.

Pin Capacitance

Symbol	Parameters	Pins	Min.	Max.	Unit	Notes
CCK	Input pin capacitance, CK, /CK	CK, /CK	0.8	1.4	pF	1,3
CDCK	Delta input pin capacitance, CK, /CK		0	0.15	pF	1,2
CIN_CTRL	Input pin capacitance, control pins	/CS,CKE,ODT	0.75	1.3	pF	1
CDIN_CTRL	Delta input pin capacitance, control pins		-0.4	0.2	pF	1,4
CIN_ADD_CMD	Input pin capacitance, address and command pins	/RAS,/CAS,/WE, Address	0.75	1.3	pF	1
CDIN_ADD_CMD	Delta input pin capacitance, address and command pins		-0.4	0.4	pF	1,5
CIO	Input/output pins capacitance	DQ,DQS,/DQS TDQS,/TDQS, DM	1.5	2.5	pF	1,6
CDIO	Delta input/output pins capacitance		-0.5	0.3	pF	1,7,8
CDDQS	Delta input/output pins capacitance	DQS, /DQS	0	0.15	pF	1,10
CZQ	Input/output pin capacitance, ZQ	ZQ	-	3	pF	1,9

Notes1. VDD, VDDQ, VSS, VSSQ applied and all other pins (except the pin under test) floating. VDD = VDDQ =1.5V, VBIAS=VDD/2.

Notes2. Absolute value of CCK(CK-pin) - CCK(/CK-pin).

Notes3. CCK (min.) will be equal to CIN (min.)

Notes4. CDIN_CTRL = CIN_CTRL - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes5. CDIN_ADD_CMD = CIN_ADD_CMD - 0.5*(CCK(CK-pin) + CCK(/CK-pin))

Notes6. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

Notes7. DQ should be in high impedance state.

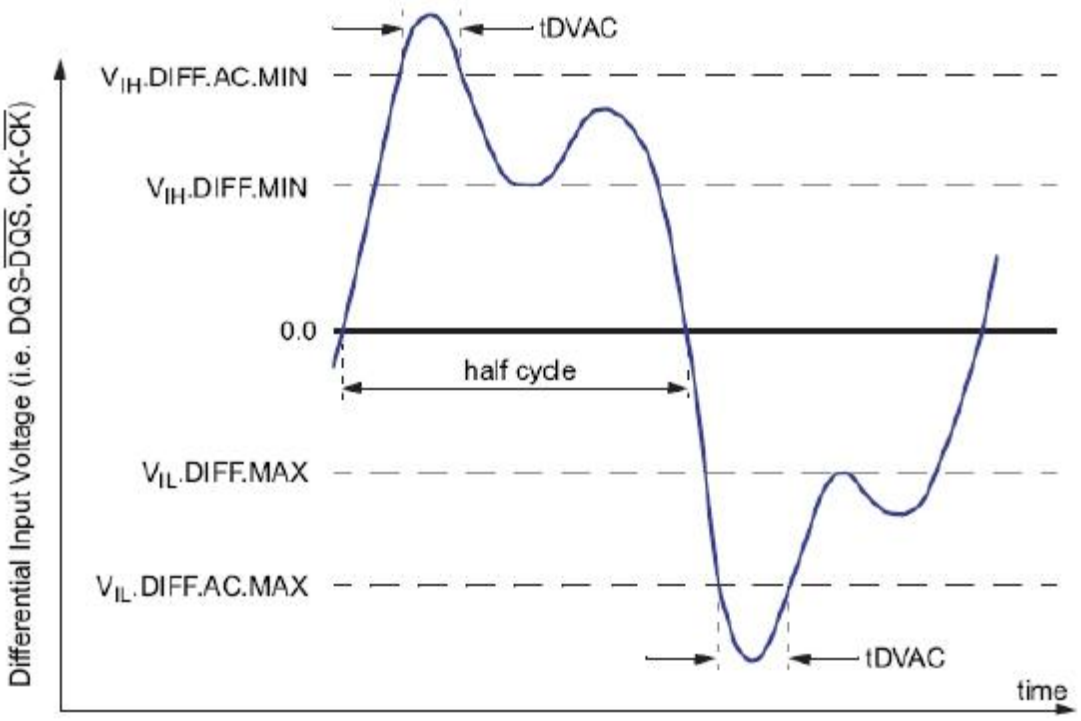
Notes8. CDIO = CIO (DQ, DM) - 0.5*(CIO(DQS-pin) + CIO(/DQS-pin)).

Notes9. Maximum external load capacitance on ZQ pin is 5pF.

Notes10. Absolute value of CIO(DQS) - CIO(/DQS).

AC and DC Logic Input Levels for Differential Signals

Differential signals definition



Definition of differential ac-swing and "time above ac level" tDVAC

Differential AC and DC Input Levels

Symbol	Parameter	Min.	Max.	Units	Note
V_{IHdiff}	Differential input high	+0.2	See ***Note3***	V	1
V_{ILdiff}	Differential input low	See ***Note3***	-0.2	V	1
V_{IHdiff} (AC)	AC Differential input high	2x(VIH(AC)-VREF)	See ***Note3***	V	2
V_{ILdiff} (AC)	AC Differential input low	See ***Note3***	2x(VREF-VIL(AC))	V	2

Note1. It is used to define a differential signal slew-rate.

Note2. For CK - /CK use VIH/VIL(AC) of address/command and VREFCA; for strobes (DQS, DQS) use VIH/VIL(AC) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

Note3. These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals.

Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

- Allowed time before ringback (tDVAC) for CK - /CK and DQS - /DQS

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV	
-	Min	Max	Min	Max
>4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
<1.0	0	-	150	-

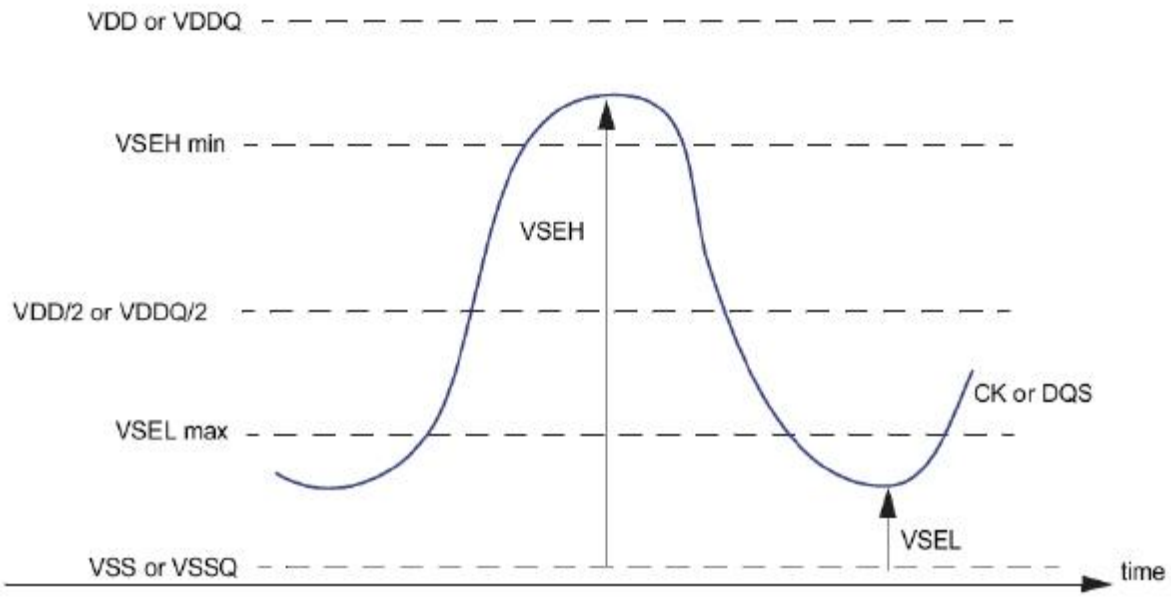
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, /CK, /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(AC) / VIL(AC)) for Address/Command signals) in every half-cycle.

DQS, /DQS have to reach VSEHmin / VSELmax [approximately the ac-levels (VIH(AC) / VIL(AC)) for DQ signals] in every half-cycle preceding and following a valid transition.

Note that the applicable AC-levels for Address/Command and DQ's might be different per speed-bin etc. E.g., if V_{IHCA}(AC150)/V_{ILCA}(AC150) is used for Address/Command signals, then these AC-levels apply also for the single-ended components of differential CK and /CK.



Single-ended requirement for differential signals

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same.

The transition of single-ended signals through the AC-levels is used to measure setup time. For singleended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, /CK, /DQS

Symbol	Parameter	Min.	Max.	Units	Note
VSEH	Single-ended high-level for strobes	(VDD/2)+0.175	See ***Note3***	V	1,2
	Single-ended high-level for CK, /CK	(VDD/2)+0.175	See ***Note3***	V	1,2
VSEL	Single-ended low-level for strobes	See ***Note3***	(VDD/2)-0.175	V	1,2
	Single-ended low-level for CK, /CK	See ***Note3***	(VDD/2)-0.175	V	1,2

Note1. For CK, /CK use VIH/VIL(AC) of address/command; for strobes (DQS, DQS) use VIH/VIL(AC) of DQs.

Note2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.

Note3. These values are not defined, however the single-ended components of differential signals CK, /CK, DQS, /DQS need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot.

AC and DC Output Measurement Levels

Symbol	Parameter	Specification	Units	Note
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	0.8*V_{DDQ}	V	
V_{OM}(DC)	DC output middle measurement level (for IV curve linearity)	0.5*V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.2*V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output slew rate)	VTT+0.1*V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output slew rate)	VTT-0.1*V_{DDQ}	V	1
V_{OHdiff}(DC)	AC differential output high measurement level (for output slew rate)	0.2*V_{DDQ}	V	2
V_{OLdiff}(DC)	AC differential output low measurement level (for output slew rate)	-0.2*V_{DDQ}	V	2

Notes1. The swing of ±0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

Notes2. The swing of ±0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

DQS Output Crossing Voltage - VOX (DDR3-1600 or Higher Speed Bin)

Symbol	Parameters	DQS, /DQS differential slew rate								Unit
		5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	11V/ns	12V/ns	
V_{OX} (AC) max.	Deviation of DQS, /DQS output cross point voltage from 0.5*V_{DDQ}	+100	+120	+140	+160	+180	+200	+200	+200	mV
V_{OX} (AC) min.		-100	-120	-140	-160	-180	-200	-200	-200	mV

DQS Output Crossing Voltage - VOX (DDR3-1333 or Lower Speed Bin)

Symbol	Parameters	DQS, /DQS differential slew rate								Unit
		5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	11V/ns	12V/ns	
V_{OX} (AC) max.	Deviation of DQS, /DQS output cross point voltage from 0.5*V_{DDQ}	+125	+150	+175	+200	+225	+225	+225	+225	mV
V_{OX} (AC) min.		-125	-150	-175	-200	-225	-225	-225	-225	mV

Notes1. Measured using an effective test load of 25Ω to 0.5* V_{DDQ} at each of the differential outputs.
Notes2. For a differential slew rate in between the listed values, the V_{OX} value may be obtained by linear interpolation.
Notes3. The DQS, /DQS pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one V_{OX} value when tested with specified test condition. The DQS and /DQS differential slew rate when measuring V_{OX} determines which V_{OX} limits to use.

Recommended DC Operating Conditions

VDD/VDDQ = 1.5V±0.075V

Symbol	Parameter & Test Conditions	-125	-150	Units
		Max		
I_{DD1}	**Operating One Bank Active-Read-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	105	100	mA
I_{DD2P1}	**Precharge Power-Down Current Fast Exit:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	35	30	mA
I_{DD2N}	**Precharge Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	45	40	mA
I_{DD3P}	**Active Power-Down Current:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	40	35	mA
I_{DD4W}	**Operating Burst Write Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	185	165	mA
I_{DD4R}	**Operating Burst Read Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	180	160	mA
I_{DD5B}	**Burst Refresh Current:** CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	210	200	mA

Symbol	Parameter & Test Conditions	-125	-150	Units
		Max		
I_{DD6}	**Self Refresh Current: Normal Temperature Range;** TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	12	12	mA
I_{DD7}	**Operating Bank Interleave Read Current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	370	330	mA

Note 1: Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

Note 2: Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

Note 3: Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit

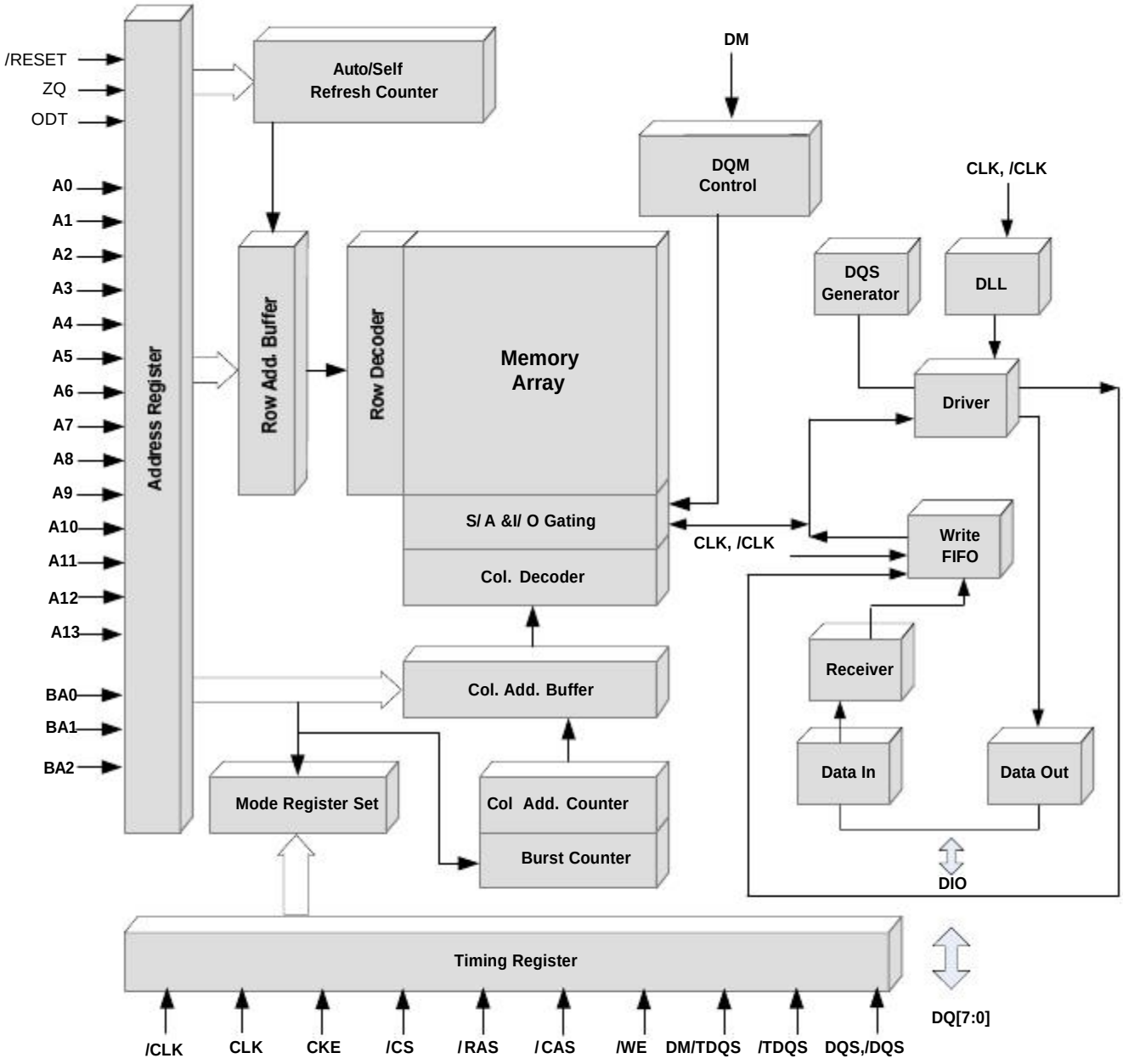
Note 4: Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

Note 5: Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

Note 6: Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM

Note 7: Read Burst type : Nibble Sequential, set MR0 A[3]=0B

Block Diagram



AC Operating Test Characteristics

DDR3-1333 & DDR3-1600 Speed Bins

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	-107 (DDR3-1866)		-125 (DDR3-1600)		-150 (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	Internal read command to first data			13.750	20	13.125	20	ns	8
t_{RCD}	Active to read or write delay			13.750	-	13.125	-	ns	8
t_{RP}	Precharge command period			13.750	-	13.125	-	ns	8
t_{RC}	Active to active/auto refresh command			48.750	-	49.125	-	ns	8
t_{RAS}	Active to precharge command period			35	9*t_{REFI}	36	9*t_{REFI}	ns	7
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=6, CWL=5	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,5,6
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=7, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3,4,5,6
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=8, CWL=6	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1,2,3,5,6
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=9, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,4,6
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=10, CWL=7	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,6
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=11, CWL=8	1.25	<1.5	1.25	<1.5	-	-	ns	1,2,3
$t_{CK\ (AVG)}$	Average Clock Cycle, CL=13, CWL=9	1.07	<1.25	-	-	-	-	ns	1,2,3
-	Support CL Settings	6,7,8,9,10,11,13		6,7,8,9,10,11		6,7,8,9,10		nCK	
-	Support CWL Settings	5,6,7,8,9,10		5,6,7,8		5,6,7		nCK	

Notes1. The CL setting and CWL setting result in tCK (avg) (min.) and tCK (avg) (max.) requirements. When making a selection of tCK (avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

Notes2. tCK (avg) (min.) limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (avg) value (2.5, 1.875, 1.5, 1.25, or 1.07ns) when calculating CL (nCK) = tAA (ns) / tCK (avg)(ns), rounding up to the next 'Supported CL'.

Notes3. tCK (avg) (max.) limits: Calculate tCK (avg) + tAA (max.)/CL selected and round the resulting tCK (avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns or 1.07ns). This result is tCK (avg) (max.) corresponding to CL selected.

Notes4. 'Reserved' settings are not allowed. User must program a different value.

Notes5. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes6. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.

Notes7. tREFI depends on operating case temperature (TC).

Notes8. For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min.) must be 13.125 ns or lower. SPD settings must be programmed to match.

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	-107 (DDR3-1866)		-125 (DDR3-1600)		-150 (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK}	Minimum clock cycle, DLL-off mode	8	-	8	-	8	-	ns	6
t_{CH}, $t_{CL\ (AVG)}$	Average CK high/low level width	0.47	0.53	0.47	0.53	0.47	0.53	ns	
t_{RRD}	Active bank A to active bank B command period	6	-	6	-	6	-	ns	
		4	-	4	-	4	-	nCK	
t_{FAW}	Four Activate Window	30	-	30	-	30	-	ns	
t_{IH}(base) DC100	Address and Control input hold time (VIH/VIL(DC100) levels)	100	-	120	-	140	-	ps	16
t_{IS}(base) AC175	Address and Control input setup time (VIH/VIL(AC175) levels)	25	-	45	-	65	-	ps	16
t_{IS}(base) AC150	Address and Control input setup time (VIH/VIL(AC150) levels)	25+105	-	45+125	-	65+150	-	ps	16,24
t_{DH}(base)	DQ and DM input hold time (VIH/VIL(DC) levels)	25	-	45	-	65	-	ps	17
t_{DS}(base)	DQ and DM input setup time (VIH/VIL(AC) levels)	10	-	10	-	10	-	ps	17
t_{IPW}	Address and control input pulse width for each input	535	-	560	-	620	-	ps	25
t_{DIPW}	DQ and DM input pulse width for each input	320	-	360	-	400	-	ps	25
t_{HZ}(DQ)	DQ high impedance time	-	195	-	225	-	250	ps	13,14
t_{LZ}(DQ)	DQ low impedance time	-390	195	-450	225	-500	250	ps	13,14
t_{HZ}(DQS)	DQS,/DQS high impedance time RL+BL/2 reference	-	195	-	225	-	250	ps	13,14
t_{LZ}(DQS)	DQS,/DQS low impedance time RL-1 reference	-390	195	-450	225	-500	250	ps	13,14
t_{DQSQ}	DQS,/DQS to DQ skew per group, per access	-	85	-	100	-	125	ps	12,13
t_{CCD}	/CAS to /CAS command delay	4	-	4	-	4	-	nCK	
t_{QH}	DQ output hold time from DQS, /DQS	0.38	-	0.38	-	0.38	-	t_{CK} (avg)	12,13
t_{DQSCK}	DQS,/DQS rising edge output access time from rising CK,/CK	-225	255	-225	225	-255	255	ps	12,13
t_{DQSS}	DQS latch rising transitions to associated clock edges	-0.27	0.27	-0.27	0.27	-0.25	0.25	t_{CK} (avg)	
t_{DQSH}	DQS input high pulse width	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK} (avg)	27,28

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	-107 (DDR3-1866)		-125 (DDR3-1600)		-150 (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{DSH}	DQS falling edge hold time from rising CK	0.18	-	0.18	-	0.18	-	t_{CK} (avg)	29
t_{DSS}	DQS falling edge setup time to rising CK	0.18	-	0.18	-	0.18	-	t_{CK} (avg)	29
t_{DQSL}	DQS input low pulse width	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK} (avg)	26,28
t_{QSH}	DQS output high time	0.40	-	0.40	-	0.40	-	t_{CK} (avg)	12,13
t_{QSL}	DQS output low time	0.40	-	0.40	-	0.40	-	t_{CK} (avg)	12,13
t_{MRD}	Mode register set command cycle	4	-	4	-	4	-	nCK	
t_{MOD}	Mode register set command update Delay	15	-	15	-	15	-	ns	
		12	-	12	-	12	-	nCK	
t_{RPRE}	Read preamble time	0.9	-	0.9	-	0.9	-	t_{CK} (avg)	13,19
t_{RPST}	Read postamble time	0.3	-	0.3	-	0.3	-	t_{CK} (avg)	11,13
t_{WPRE}	Write preamble time	0.9	-	0.9	-	0.9	-	t_{CK} (avg)	1
t_{WPST}	Write postamble time	0.3	-	0.3	-	0.3	-	t_{CK} (avg)	1
t_{WR}	Write recovery time	15	-	15	-	15	-	ns	
t_{DAL}(min)	Auto precharge write recovery + precharge time	WR + roundup[t_{RP} / t_{CK}(avg)						nCK	
t_{MPRR}	Multi purpose register recovery time	1	-	1	-	1	-	nCK	22
t_{WTR}	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns	18
		4	-	4	-	4	-	nCK	
t_{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns	
		4	-	4	-	4	-	nCK	
t_{CKESR}	Minimum CKE low width for self-refresh entry to exit	$t_{CKE\ (min)}$ +1	-	$t_{CKE\ (min)}$ +1	-	$t_{CKE\ (min)}$ +1	-	nCK	
t_{CKSRE}	Valid clock requirement after self-refresh entry or power-down entry	10	-	10	-	10	-	ns	
		5	-	5	-	5	-	nCK	
t_{CKSRX}	Valid clock requirement before self-refresh exit or power-down exit	10	-	10	-	10	-	ns	
		5	-	5	-	5	-	nCK	

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	-107 (DDR3-1066)		-125 (DDR3-1600)		-150 (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		9-9-9			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XS}	Exit self-refresh to commands not requiring a locked DLL	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	ns	
		5	-	5	-	5	-	nCK	
t_{XSDLL}	Exit self-refresh to commands requiring a locked DLL	t_{DLL}(min)	-	t_{DLL}(min)	-	t_{DLL}(min)	-	nCK	
t_{RFC}	Auto-refresh to active/auto-refresh command	260	-	260	-	260	-	ns	
t_{REFI}	Average periodic refresh interval 0℃ ≦ T_C ≦ +85℃	-	7.8	-	7.8	-	7.8	µs	
t_{CKE}	CKE minimum high and low pulse width	5	-	5	-	5	-	ns	
		3	-	3	-	3	-	nCK	
t_{XPR}	Exit reset from CKE high to a valid command	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	ns	
		5	-	5	-	5	-	nCK	
t_{DLLK}	DLL locking time	512	-	512	-	512	-	nCK	
t_{PD}	Power-down entry to exit time	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		15
t_{XPDLL}	Exit precharge power-down with DLL frozen to commands requiring a locked DLL	24	-	24	-	24	-	ns	2
		10	-	10	-	10	-	nCK	
t_{XP}	Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	6	-	6	-	6	-	ns	
		3	-	3	-	3	-	nCK	
t_{WRPDEN} (min)	Timing of WR command to power-down entry (BL8OTF, BL8MRS, BL4OTF)	WL + 4 + [t_{WR} / t_{CK}(avg)]						nCK	9
t_{WRPDEN} (min)	Timing of WR command to power-down entry (BC4MRS)	WL + 2 + [t_{WR} / t_{CK}(avg)]						nCK	
$t_{WRAPDEN}$	Timing of WRA command to power-down entry (BL8OTF, BL8MRS, BL4OTF)	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
$t_{WRAPDEN}$	Timing of WRA command to power-down entry (BC4MRS)	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	-107 (DDR3-1866)		-125 (DDR3-1600)		-150 (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	13-13-13		11-11-11		7-7-7			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{REFPDEN}$	Timing of REF command to power-down entry	1	-	1	-	1	-	nCK	20,21
$t_{MRSPDEN}$	Timing of MRS command to power-down entry	t_{MOD} (min)	-	t_{MOD} (min)	-	t_{MOD} (min)	-		
t_{CPDED}	Command pass disable delay	1	-	1	-	1	-	nCK	
$t_{ACTPDEN}$	Timing of ACT command to power-down entry	1	-	1	-	1	-	nCK	20
t_{PRPDEN}	Timing of PRE command to power-down entry	1	-	1	-	1	-	nCK	20
t_{RDPDEN}	Timing of RD/RDA command to power-down entry	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	nCK	
t_{AON}	RTT turn-on	-195	195	-225	225	-250	250	ps	7
t_{AONPD}	Asynchronous RTT turn-on delay (Power-down with DLL frozen)	2	8.5	2	8.5	2	8.5	ns	
t_{AOF}	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	0.3	0.7	t_{CK} (avg)	8
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-down with DLL frozen)	2	8.5	2	8.5	2	8.5	ns	
ODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	4	-	nCK	
ODTH8	ODT high time with write command and BL8	6	-	6	-	6	-	nCK	
t_{ADC}	RTT dynamic change skew	0.3	0.7	0.3	0.7	0.3	0.7	t_{CK} (avg)	
t_{ZQinit}	Power-up and reset calibration time	512	-	512	-	512	-	nCK	
t_{ZQoper}	Normal operation full calibration time	256	-	256	-	256	-	nCK	
t_{ZQCS}	Normal operation short calibration time	64	-	64	-	64	-	nCK	23
t_{WLMRD}	First DQS pulse rising edge after write leveling mode is programmed	40	-	40	-	40	-	nCK	3
$t_{WLDQSEN}$	DQS./DQS delay after write leveling mode is programmed	25	-	25	-	25	-	nCK	3
t_{RTW}	Read to write command delay (BC4MRS, BC4OTF)	RL + t_{CCD}/2 + 2nCK-WL	-	RL + t_{CCD}/2 + 2nCK-WL	-	RL + t_{CCD}/2 + 2nCK-WL	-		
t_{RTW}	Read to write command delay (BL8MRS, BL8OTF)	RL + t_{CCD}/2 + 2nCK-WL	-	RL + t_{CCD}/2 + 2nCK-WL	-	RL + t_{CCD}/2 + 2nCK-WL	-		
t_{RAP}	Active to read with auto precharge command delay	t_{RCD} min	-	t_{RCD} min	-	t_{RCD} min	-		

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	**-107 (DDR3-1866)**		**-125** (DDR3-1600)		**-150** (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	**13-13-13**		**11-11-11**		**9-9-9**			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WLS}	Write leveling setup time from rising CK,/CK crossing to rising DQS,/DQS crossing	140	-	165	-	195	-	ps	
t_{WLH}	Write leveling hold time from rising DQS,/DQS crossing to rising CK,/CK crossing	140	-	165	-	195	-	ps	
t_{WLO}	Write leveling output delay	0	7.5	0	7.5	0	7.5	ns	
t_{WLOE}	Write leveling output error	0	2	0	2	0	2	ns	
t_{CK} (abs)	Absolute clock period	t_{CK} (avg)min+ t_{JIT}(per)min	t_{CK} (avg)max+ t_{JIT} (per)max	t_{CK} (avg)min+ t_{JIT}(per)min	t_{CK} (avg)max+ t_{JIT} (per)max	t_{CK} (avg)min+ t_{JIT} (per)min	t_{CK} (avg)max+ t_{JIT} (per)max	ps	
t_{CH} (abs)	Absolute clock high pulse width	0.43	-	0.43	-	0.43	-	t_{CK} (avg)	30
t_{CL} (abs)	Absolute clock low pulse width	0.43	-	0.43	-	0.43	-	t_{CK} (avg)	31
t_{JIT} (per)	Clock period jitter	-60	60	-70	70	-80	80	ps	
t_{JIT} (per,lck)	Clock period jitter during DLL locking period	-50	50	-60	60	-70	70	ps	
t_{JIT} (cc)	Cycle to cycle period jitter	120		-	140	-	140	ps	
t_{JIT} (cc,lck)	Cycle to cycle period jitter during DLL locking period	100		-	120	-	120	ps	
t_{ERR} (nper)	Cumulative error across n= 13,14,… 49,50 cycles	t_{ERR} (nper)min=(1+0.68ln(n))*t_{JIT} (per)min t_{ERR} (nper)max=(1+0.68ln(n))*t_{JIT} (per)max						ps	32

AC Operating Test Characteristics

VDD/VDDQ = 1.5V±0.075V

Symbol	Speed Bin	**-107** (DDR3-1866)		**-125** (DDR3-1600)		**-150** (DDR3-1333)		Units	Notes
	CL-nRCD-nRP	**13-13-13**		**11-11-11**		**9-9-9**			
	Parameter	Min.	Max.	Min.	Max.	Min.	Max.		
t_{ANPD}	ODT to power-down entry/ exit latency	WL–1	-	WL–1	-	WL–1	-	nCK	
$ODTL_{on}$	ODT turn on latency	WL–2	WL–2	WL–2	WL–2	WL–2	WL–2	nCK	
$ODTL_{off}$	ODT turn off latency	WL–2	WL–2	WL–2	WL–2	WL–2	WL–2	nCK	
$ODTL_{cnw}$	ODT latency for changing from RTT_Nom to RTT_WR	WL–2	WL–2	WL–2	WL–2	WL–2	WL–2	nCK	
$ODTL_{cwn4}$	ODT latency for changing from RTT_WR to RTT_Nom (BC4)	-	4+$ODTL_{off}$	-	4+$ODTL_{off}$	-	4+$ODTL_{off}$	nCK	
$ODTL_{cwn8}$	ODT latency for changing from RTT_WR to RTT_Nom (BL8)	-	6+$ODTL_{off}$	-	6+$ODTL_{off}$	-	6+$ODTL_{off}$	nCK	

Note 1: Actual value dependant upon measurement level definitions which are TBD.

Note 2: Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.

Note 3: The max values are system dependent.

Note 4: WR as programmed in mode register.

Note 5: Value must be rounded-up to next higher integer value.

Note 6: There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

Note 7: ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.

Note 8: ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.

Note 9: tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

Note 10: WR in clock cycles as programmed in MR0.

Note 11: The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.

Note 12: Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.

Note 13: Value is only valid for RON34.

Note 14: Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.

Note 15: tREFI depends on operating case temperature (Tc).

Note 16: tIS(base) and tIH(base) values are for 1V/ns command/ addresss single-ended slew rate and 2V/ns CK, /CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.

Note 17: tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals, VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and and Slew Rate Derating section.

Note 18: Start of internal write transaction is defined as follows ;

For BL8 (fixed by MRS and on-the-fly, OTF) : Rising clock edge 4 clock cycles after WL.

For BC4 (on-the-fly, OTF) : Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

Note 19: The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Note 20: CKE is allowed to be registered low while operations such as row activation, precharge, auto precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.

Note 21: Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.

Note 22: Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

Note 23: One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

Note 24: The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

Note 25: Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).

Note 26: tDQSL describes the instantaneous differential input low pulse width on DQS - /DQS, as measured from one falling edge to the next consecutive rising edge.

Note 27: tDQSH describes the instantaneous differential input high pulse width on DQS - /DQS, as measured from one rising edge to the next consecutive falling edge.

Note 28: tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

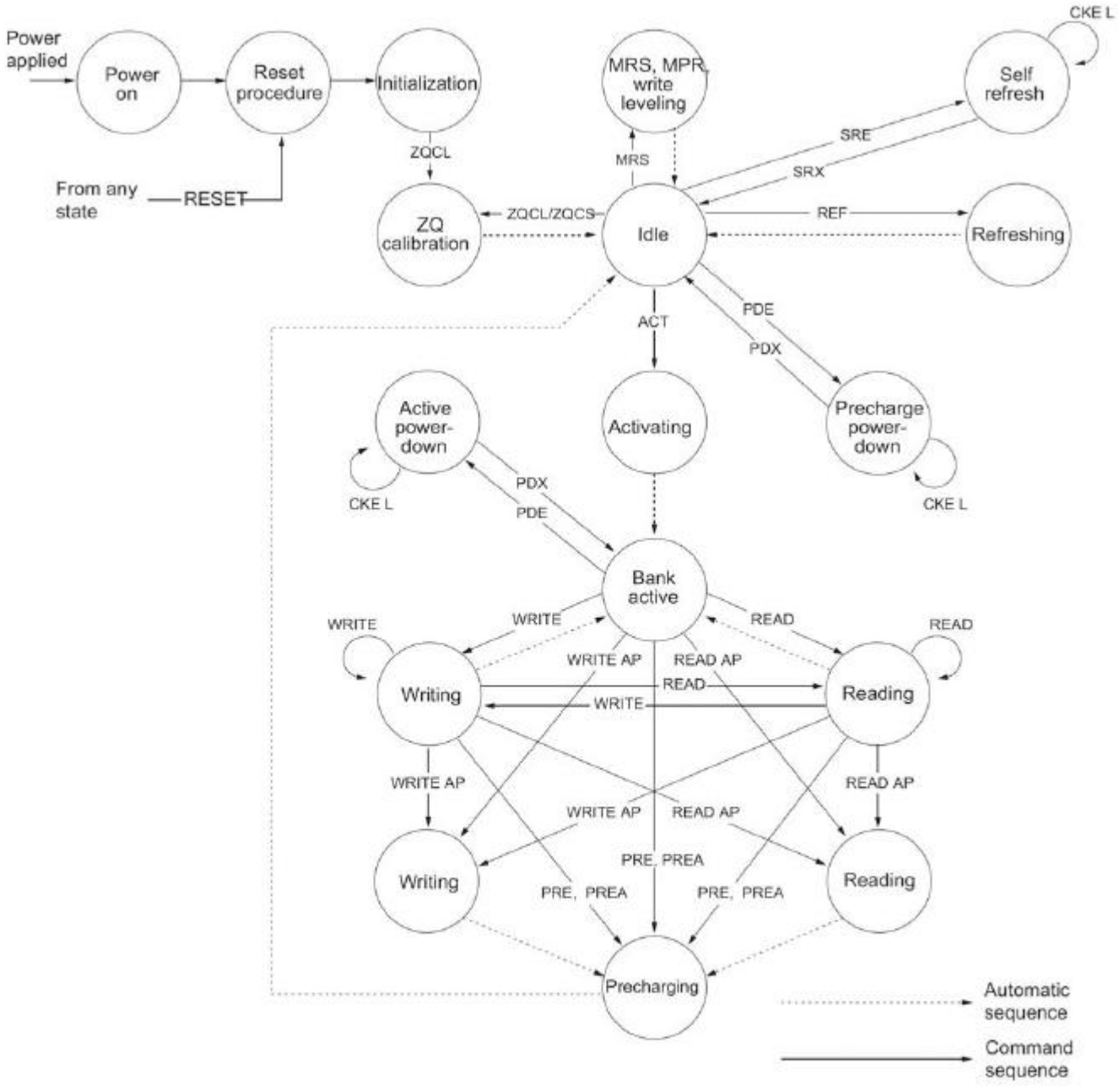
Note 29: tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

Note 30: tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

Note 31: tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Note 32: n = from 13 cycles to 50 cycles. This row defines 38 parameters.

Simplified State Diagram



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA = PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0~BA2	A10	A12, A10~A0
		n-1	N							
Device Deselect	DES	H	H	H	X	X	X	X	X	X,X
No Operation	NOP	H	H	L	H	H	H	V	V	V,V
Read (fixed BL8/BC4)	RD	H	H	L	H	L	H	BA	L	V,CA
Read (BC4, OTF)	RDS4	H	H	L	H	L	H	BA	L	L,CA
Read (BL8, OTF)	RDS8	H	H	L	H	L	H	BA	L	H,CA
Read with Auto Pre-charge (fixed BL8/BC4)	RDA	H	H	L	H	L	H	BA	H	V,CA
Read with Auto Pre-charge (BC4, OTF)	RDAS4	H	H	L	H	L	H	BA	H	L,CA
Read with Auto Pre-charge (BL8, OTF)	RDAS8	H	H	L	H	L	H	BA	H	H,CA
Write (fixed BL8/BC4)	WR	H	H	L	H	L	L	BA	L	V,CA
Write (BC4, OTF)	WRS4	H	H	L	H	L	L	BA	L	L,CA
Write (BL8,OTF)	WRS8	H	H	L	H	L	L	BA	L	H,CA
Write with Auto Pre-charge (fixed BL8/BC4)	WRA	H	H	L	H	L	L	BA	H	V,CA
Write with Auto Pre-charge (BC4, OTF)	WRAS4	H	H	L	H	L	L	BA	H	L,CA
Write with Auto Pre-charge (BL8, OTF)	WRAS8	H	H	L	H	L	L	BA	H	H,CA
Bank Activate	ACT	H	H	L	L	H	H	BA	RA	
Pre-charge Single Bank	PRE	H	H	L	L	H	L	BA	L	V,V
Pre-charge All Banks	PREA	H	H	L	L	H	L	V	H	V,V
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code	
Refresh	REF	H	H	L	L	L	H	V	V	V,V
Self Refresh entry	SRE	H	L	L	L	L	H	V	V	V,V
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X,X
				L	H	H	H	V	V	V,V
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X,X
		H	L	L	H	H	H	V	V	V,V
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X,X
		L	H	L	H	H	H	V	V	V,V
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	H	X,X
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	L	X,X

H = High level, L = Low level, X = Don't care, V = Valid, BA=Bank Address, CA=Column Address, RA=Row Address

Note1. All DDR3 SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

Note2. /RESET is low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

Note3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Note4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

Note5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly (OTF) BL will be defined by MRS.

Note6. The Power Down Mode does not perform any refresh operation.

Note7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

Note8. Self Refresh Exit is asynchronous.

Note9. VREF(Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

Note11. The Deselect command performs the same function as No Operation command.

Note12. Refer to the CKE Truth Table for more detail with CKE transition.

2. CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n)	Notes
	n-1	n			
Power Down	L	L	X	Maintain power down	14,15
	L	H	DESELECT or NOP	Power down exit	11,14
Self Refresh	L	L	X	Maintain self refresh	15,16
	L	H	DESELECT or NOP	Self refresh exit	8,12,16
Bank Active	H	L	DESELECT or NOP	Active power down entry	11,13,14
Reading	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power down entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge power down entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge power down entry	11,13,14,18
	H	L	REFRESH	Self refresh	9,13,18
For more details with all signals, see “Command Truth Table”					10

Note1. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

Note2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge n.

Note3. Command (n) is the command registered at clock edge n, and ACTION (n) is a result of Command (n), ODT is not included here.

Note4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Note5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

Note6. During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

Note7. DESELECT and NOP are defined in the “Command Truth Table”.

Note8. On self-refresh exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

Note9. Self-Refresh mode can only be entered from the All Banks Idle state.

Note10. Must be a legal command as defined in the “Command Truth Table”.

Note11. Valid commands for power-down entry and exit are NOP and DESELECT only.

Note12. Valid commands for self-refresh exit are NOP and DESELECT only.

Note13. Self-Refresh can not be entered during Read or Write operations.

Note14. The Power-Down does not perform any refresh operations.

Note15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

Note16. VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh

operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write Leveling activity may not occur earlier than 512 nCK after exit from Self Refresh.

Note17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

Note18. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Initialization

The following sequence is required for power-up and initialization and is shown in below Figure:

1. Apply power (/RESET is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). /RESET needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before /RESET being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.

- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
- Vref tracks VDDQ/2. OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After /RESET is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clocks (CK, /CK) need to be started and stabilized for at least 10 ns or 5 t_{CK} (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as /RESET is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after /RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, t_{XPR}, before issuing the first MRS command to load mode register. *(t_{XPR}=max (t_{XS} ; 5 x t_{CK})*

6. Issue MRS Command to load ***MR2*** with all application settings. (To issue MRS command for ***MR2***, provide “Low” to BA0 and BA2, “High” to BA1.)

7. Issue MRS Command to load ***MR3*** with all application settings. (To issue MRS command for ***MR3***, provide “Low” to BA2, “High” to BA0 and BA1.)

8. Issue MRS Command to load ***MR1*** with all application settings and DLL enabled. (To issue "DLL Enable"

command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).

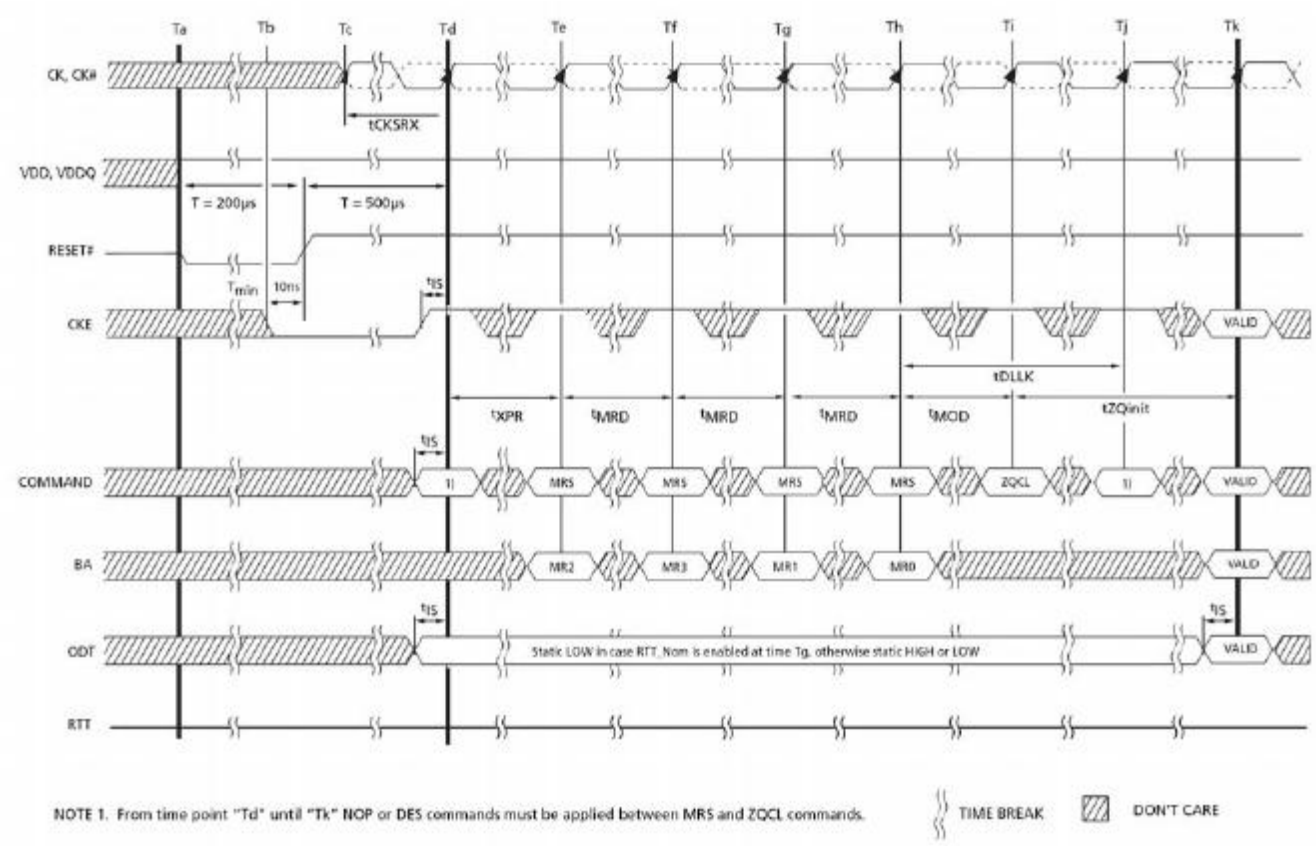
9. Issue MRS Command to load ***MR0*** with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both tDLLK and tZQinit completed.

12. The DDR3 SDRAM is now ready for normal operation.

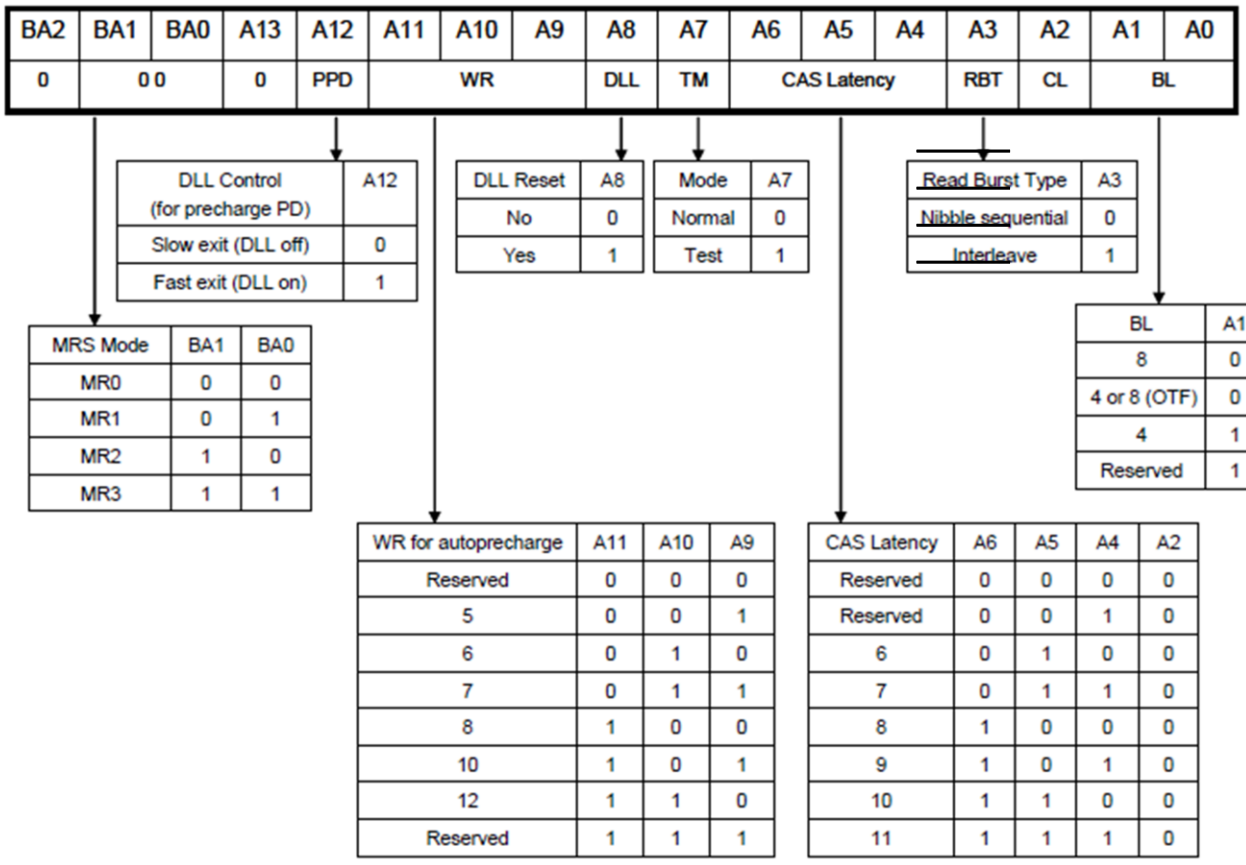
Reset and Power up initialization sequence



Mode Register Definition

Mode Register MR0

The Mode Register ***MR0*** stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0 0		0	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL	

DLL Control (for precharge PD)	A12
Slow exit (DLL off)	0
Fast exit (DLL on)	1

DLL Reset	A8
No	0
Yes	1

Mode	A7
Normal	0
Test	1

Read Burst Type	A3
Nibble sequential	0
Interleave	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

BL	A1	A0
8	0	0
4 or 8 (OTF)	0	1
4	1	0
Reserved	1	1

WR for autoprecharge	A11	A10	A9
Reserved	0	0	0
5	0	0	1
6	0	1	0
7	0	1	1
8	1	0	0
10	1	0	1
12	1	1	0
Reserved	1	1	1

CAS Latency	A6	A5	A4	A2
Reserved	0	0	0	0
Reserved	0	0	1	0
6	0	1	0	0
7	0	1	1	0
8	1	0	0	0
9	1	0	1	0
10	1	1	0	0
11	1	1	1	0

Note1. BA2 and A13 are reserved for future use and must be programmed to 0 during MRS.

Note2. WR (write recovery for autoprecharge) min in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/t_{CK}[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.

Burst Type (A3)

Burst Length	R/W	A2	A1	A0	Sequential Addressing, A3=0	Interleave Addressing, A3=1
4 (chop)	R	0	0	0	0123TTTT	0123TTTT
	R	0	0	1	1230TTTT	1032TTTT
	R	0	1	0	2301TTTT	2301TTTT
	R	0	1	1	3012TTTT	3210TTTT
	R	1	0	0	4567TTTT	4567TTTT
	R	1	0	1	5674TTTT	5476TTTT
	R	1	1	0	6745TTTT	6745TTTT
	R	1	1	1	7456TTTT	7654TTTT
	W	0	V	V	0123XXXX	0123XXXX
	W	1	V	V	4567XXXX	4567XXXX
8	R	0	0	0	01234567	01234567
	R	0	0	1	12305674	10325476
	R	0	1	0	23016745	23016745
	R	0	1	1	30127456	32107654
	R	1	0	0	45670123	45670123
	R	1	0	1	56741230	54761032
	R	1	1	0	67452301	67452301
	R	1	1	1	74563012	76543210
	W	V	V	V	01234567	01234567

Note1. In case of burst length being fixed to 4 by ***MR0*** setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12 (/BC), the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

Note2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

Note3. T: Output driver for data and strobes are in high impedance.

Note4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

Note5. X: Don't Care.

CAS Latency

The CAS Latency is defined by ***MR0*** (bits A9-A11). CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by ***MR0*** (bit A7 = 0) and rest bits set to the desired values. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM factory and should NOT be used. No operations or functionality is specified if A7 = 1.

DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

Write Recovery

The programmed WR value ***MR0*** (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/ tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When ***MR0*** (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When ***MR0*** (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

Mode Register MR1

The Mode Register ***MR1*** stores the data for enabling or disabling the DLL, output driver strength, RTT_Nom impedance, additive latency, write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0, low on BA1 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	Qoff	TDQS	0	Rtt	0	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL

TDQS enable	A11
Disabled	0
Enabled	1

Output Driver Impedance Control	A5	A1
RZQ/6	0	0
RZQ/7	0	1
Reserved	1	0
Reserved	1	1

DLL Enable	A0
Enable	0
Disable	1

Qoff	A12
Output buffer enabled	0
Output buffer disabled	1

Write leveling enable	A8
Disabled	0
Enabled	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

Rtt_Nom	A9	A6	A2
ODT disabled	0	0	0
RZQ/4	0	0	1
RZQ/2	0	1	0
RZQ/6	0	1	1
RZQ/12	1	0	0
RZQ/8	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Additive Latency	A4	A3
0	0	0
CL - 1	0	1
CL - 2	1	0
Reserved	1	1

Note1. BA2, A8, A10 and A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.

Note2. Qoff: Outputs disabled - DQs, DQSs, /DQSs.

Note3. In Write leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 1, all RTT_Nom settings are allowed; in Write Leveling Mode (***MR1***[bit7] = 1) with ***MR1***[bit12] = 0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

Note4. New RON value is defined as RON48=RZQ/5.

DLL Enable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with ***MR1*** (A0 = 0), the DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refers to “DLL-off Mode”.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits ***MR1***{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, ***MR2*** {A10, A9} = {0,0}, to disable Dynamic ODT externally.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in ***MR1***. A separate value (Rtt_WR) may be programmed in ***MR2*** to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, It allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

Output Disable

The outputs may be enabled/disabled by ***MR1*** (bit A12). When this feature is enabled (A12 = 1), all output pins (DQs, DQS, /DQS, etc.) are disconnected from the device, thus removing any loading of the output drivers. For normal operation, A12 should be set to '0'.

TQS, /TDQS

TDQS (Termination Data Strobe) provides additional termination resistance outputs that may be useful in some system configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS & /TDQS pins that is applied to the DQS & /DQS pins. In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS. The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the /TDQS pin is not used.

Mode Register MR2

The Mode Register ***MR2*** stores the data for controlling refresh related features, including RTT_WR impedance and CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1, low on BA0 and BA2, while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	Rtt_WR		0	SRT	0	CWL			0		

Self refresh temp. range	A7
Normal operating temp. range	0
Extended temp. self refresh	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

Rtt_WR	A10	A9
Dynamic ODT off	0	0
RZQ/4	0	1
RZQ/2	1	0
Reserved	1	1

CAS write latency (CWL)	A6	A4	A3
5(t_{CK} ≧ 2.5ns)	0	0	0
6 (2.5ns > t_{CK} ≧ 1.875ns)	0	0	1
7 (1.875ns > t_{CK} ≧ 1.5ns)	0	1	0
8 (1.5ns > t_{CK} ≧ 1.25ns)	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

Note1. BA2, A8, A11 ~ A13 are RFU and must be programmed to 0 during MRS.

Note2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

CAS Write Latency (CWL)

The CAS Write Latency is defined by ***MR2*** (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. ***MR2*** Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only RTT_Nom is available.

Mode Register MR3

The Mode Register ***MR3*** controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	MPR	MPR Location	

MPR Operation	A2
Normal operation	0
Dataflow from MPR	1

MRS Mode	BA1	BA0
MR0	0	0
MR1	0	1
MR2	1	0
MR3	1	1

MPR Location	A1	A0
Predefined pattern	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

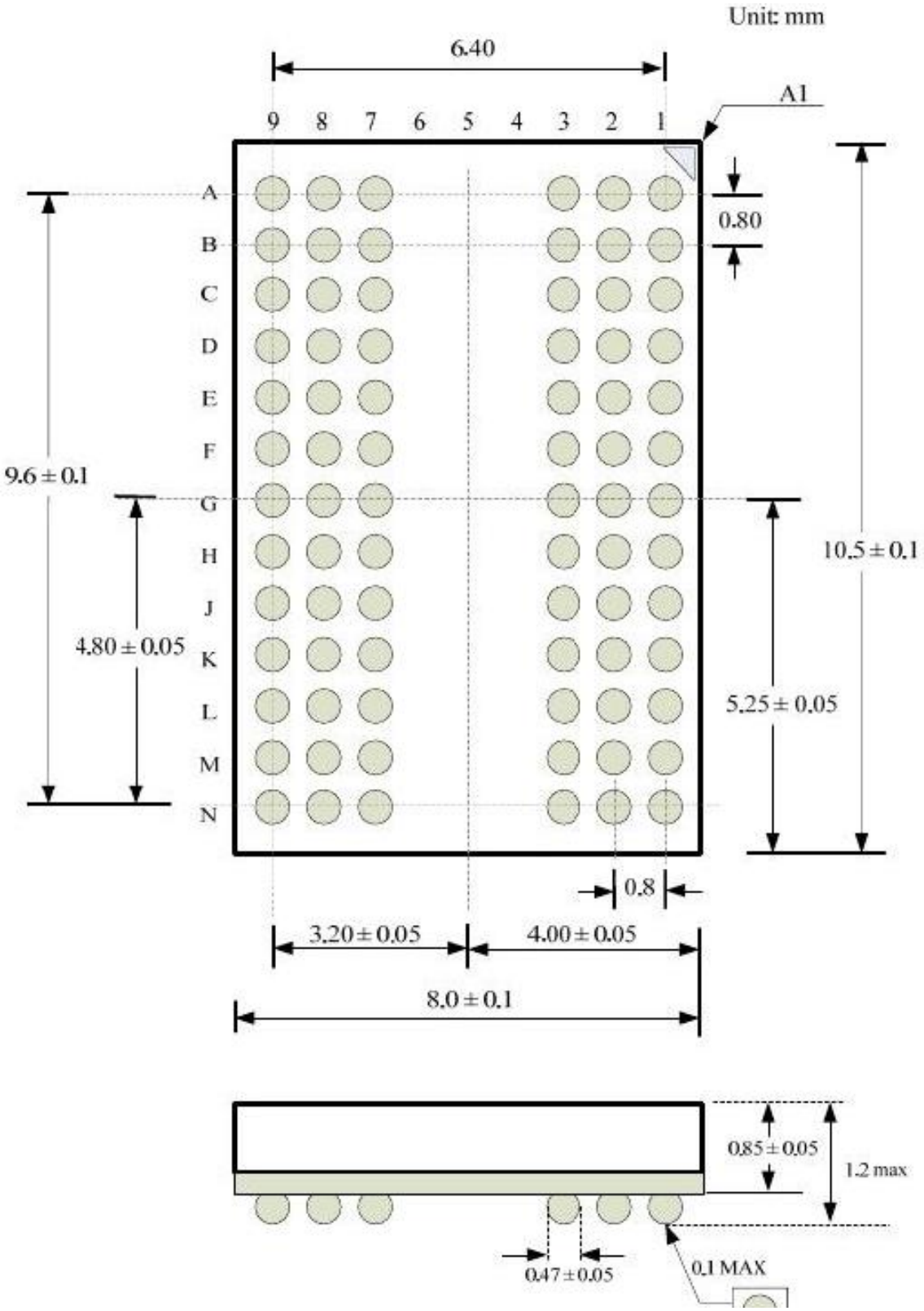
Note1. BA2, A3 - A13 are reserved for future use (RFU) and must be programmed to 0 during MRS.
Note2. The predefined pattern will be used for read synchronization.
Note3. When MPR control is set for normal operation, ***MR3*** A[2] = 0, ***MR3*** A[1:0] will be ignored

Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to ***MR3*** Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (***MR3*** bit A2 = 0). Power-down mode, self-refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

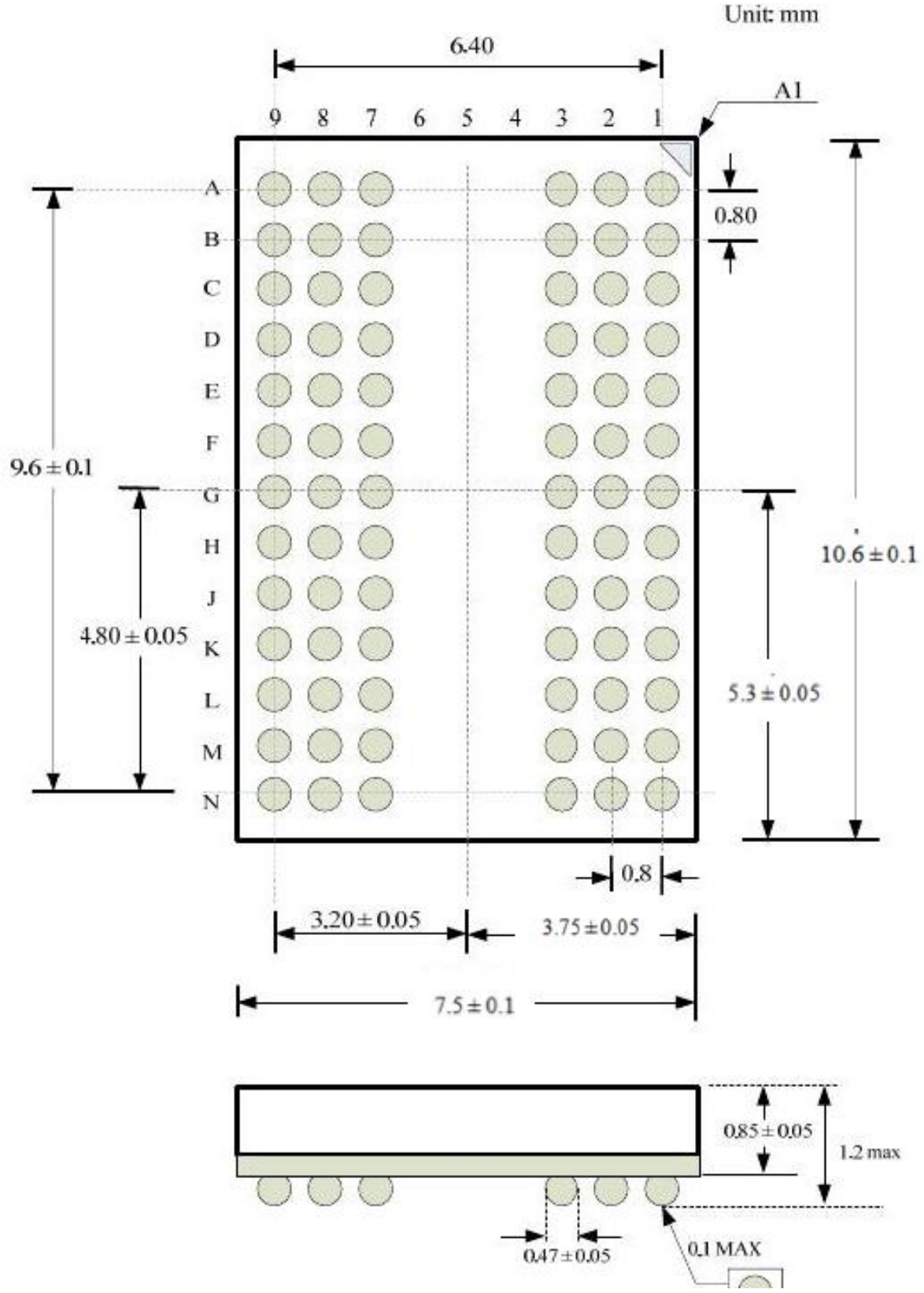
Package Description: 78Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



Package Description: 78Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)



Package Description: 78Ball-FBGA

Solder ball: Lead free (Sn-Ag-Cu)

