

MC14001B Series

B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B,
MC14025B, MC14071B, MC14073B,
MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in} , V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in} , I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C
V_{ESD}	ESD Withstand Voltage Human Body Model Machine Model Charged Device Model	> 3000 > 300 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



ON Semiconductor®

<http://onsemi.com>

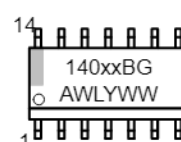


SOIC-14
D SUFFIX
CASE 751A

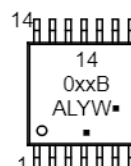


TSSOP-14
DT SUFFIX
CASE 948G

MARKING DIAGRAMS



SOIC-14



TSSOP-14

xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

DEVICE INFORMATION

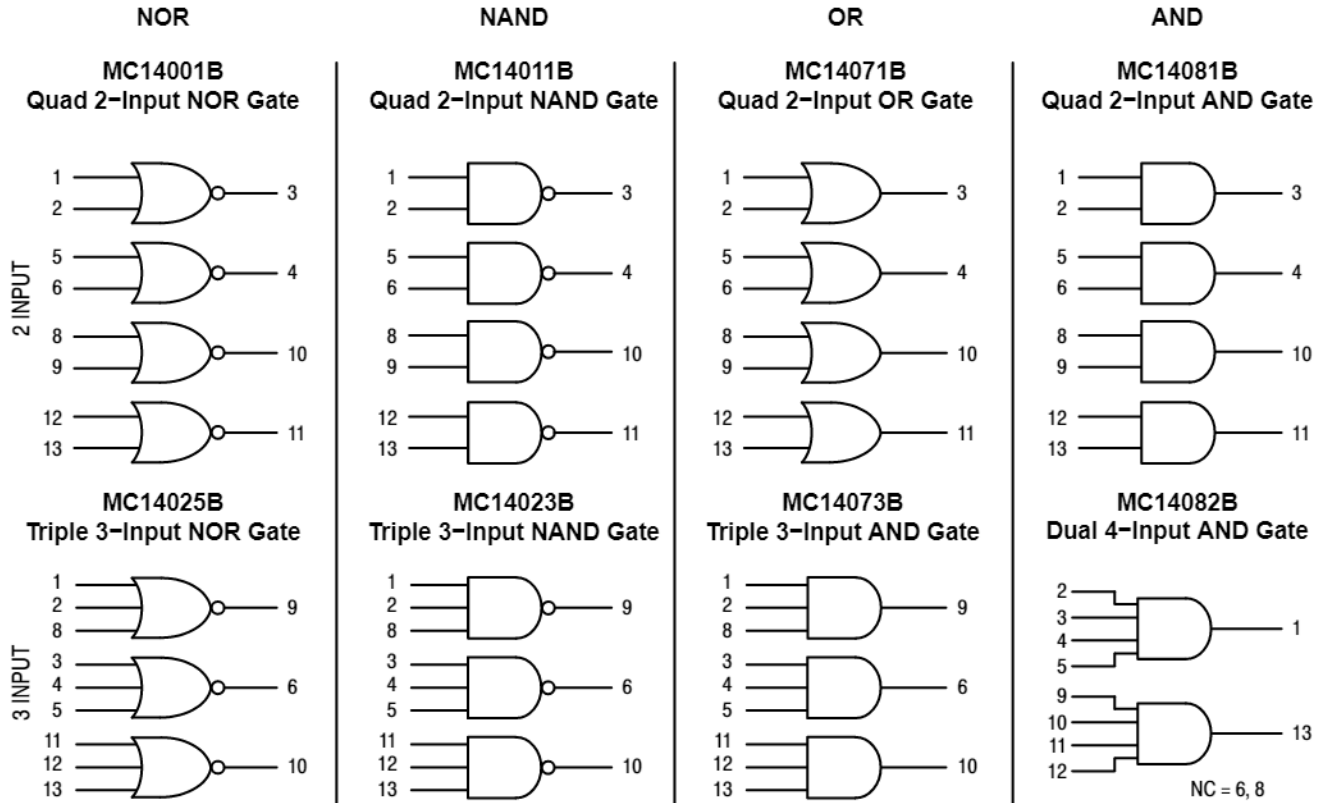
Device	Description
MC14001B	Quad 2-Input NOR Gate
MC14011B	Quad 2-Input NAND Gate
MC14023B	Triple 3-Input NAND Gate
MC14025B	Triple 3-Input NOR Gate
MC14071B	Quad 2-Input OR Gate
MC14073B	Triple 3-Input AND Gate
MC14081B	Quad 2-Input AND Gate
MC14082B	Dual 4-Input AND Gate

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

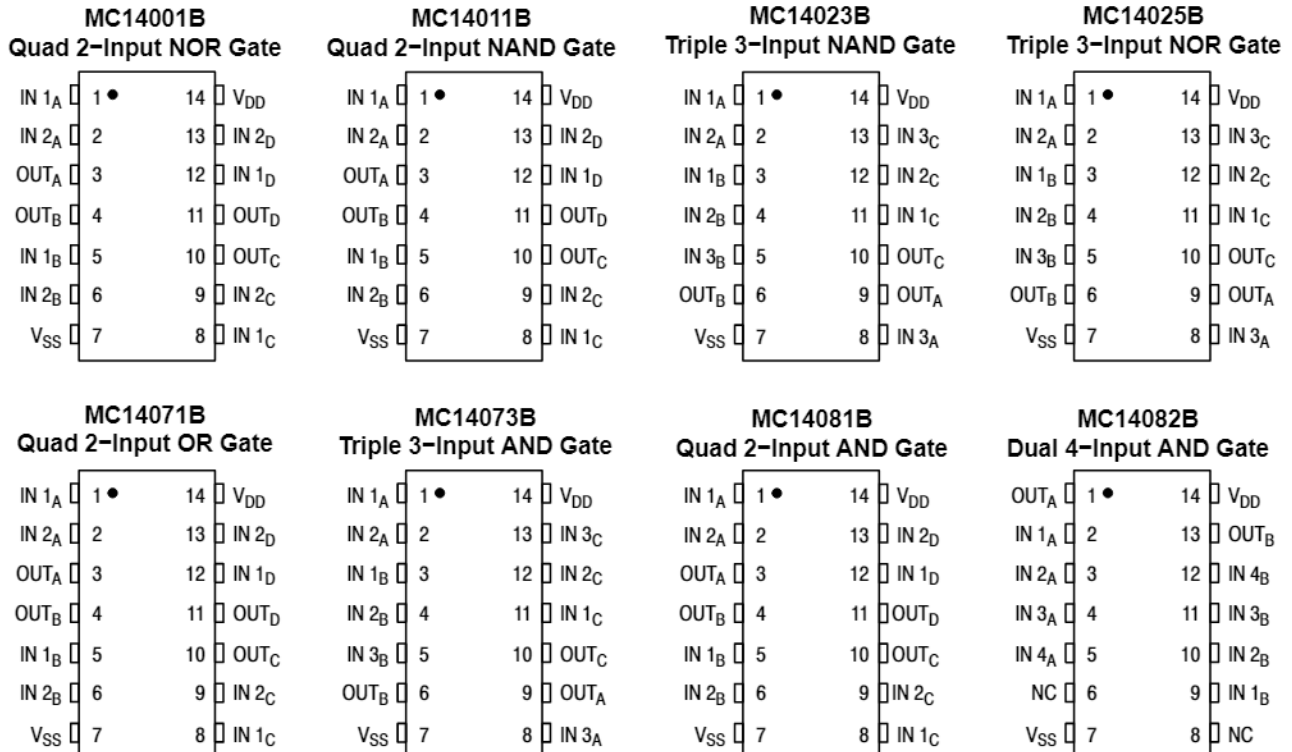
MC14001B Series

LOGIC DIAGRAMS



V_{DD} = PIN 14
 V_{SS} = PIN 7
 FOR ALL DEVICES

PIN ASSIGNMENTS



NC = NO CONNECTION

MC14001B Series

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	“0” Level V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	“1” Level V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	“0” Level V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	“1” Level V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I _{IN}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.5	–	0.0010	0.5	–	15	
		15	–	1.0	–	0.0015	1.0	–	30	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate, C _L = 50 pF)	I _T	5.0 10 15	I _T = (0.3 μA/kHz) f + I _{DD} /N I _T = (0.6 μA/kHz) f + I _{DD} /N I _T = (0.9 μA/kHz) f + I _{DD} /N							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

MC14001B Series

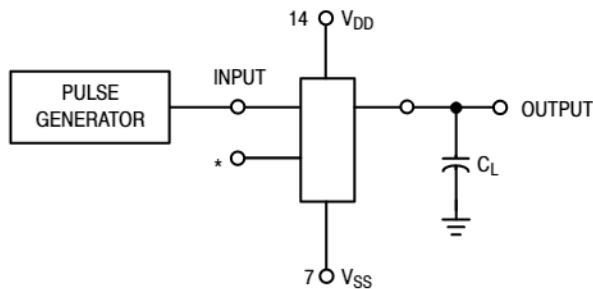
B-SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time, All B-Series Gates $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time, All B-Series Gates $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time MC14001B, MC14011B only $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 27 \text{ ns}$ All Other 2, 3, and 4 Input Gates $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$ 8-Input Gates (MC14068B, MC14078B) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	— — — — — — — — —	125 50 40 160 65 50 200 80 60	250 100 80 300 130 100 350 150 110	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



*All unused inputs of AND, NAND gates must be connected to V_{DD} .
 All unused inputs of OR, NOR gates must be connected to V_{SS} .

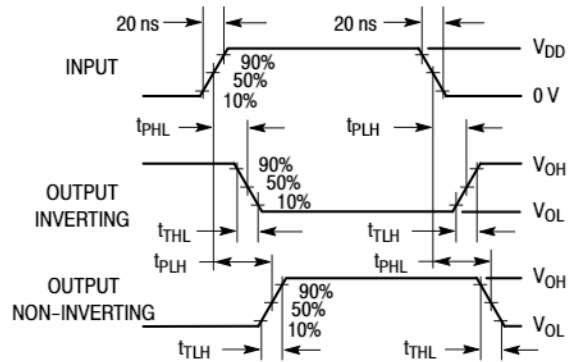
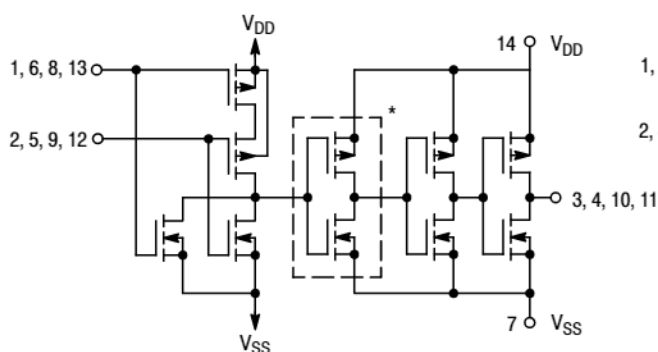


Figure 1. Switching Time Test Circuit and Waveforms

MC14001B Series

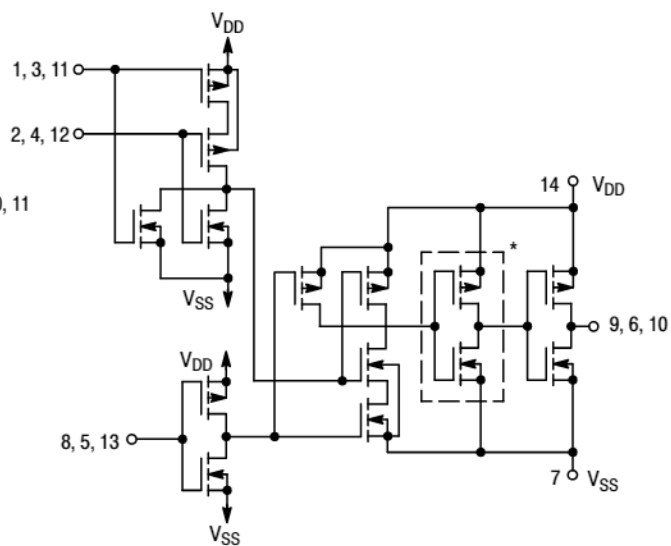
CIRCUIT SCHEMATIC NOR, OR GATES

MC14001B, MC14071B
One of Four Gates Shown



*Inverter omitted in MC14001B

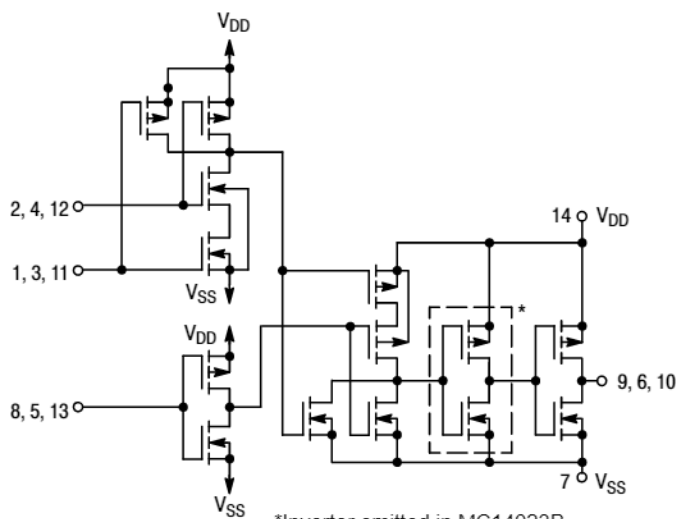
MC14025B
One of Three Gates Shown



*Inverter omitted in MC14025B

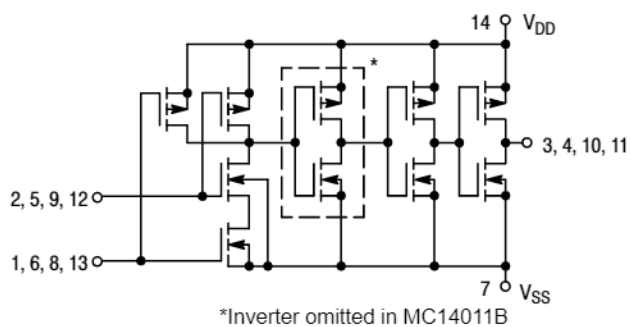
CIRCUIT SCHEMATIC NAND, AND GATES

MC14023B, MC14073B
One of Three Gates Shown



*Inverter omitted in MC14023B

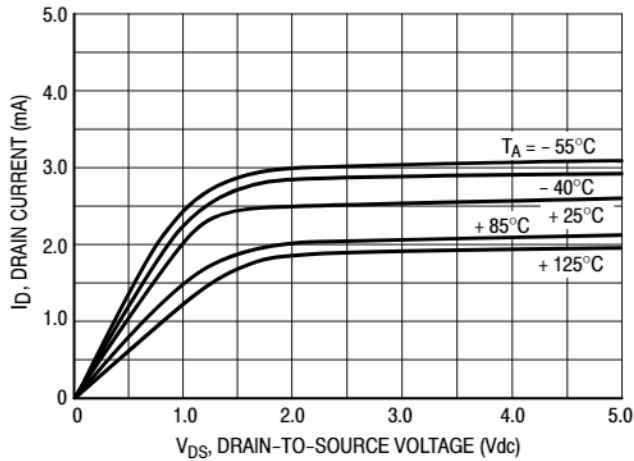
MC14011B, MC14081B
One of Four Gates Shown



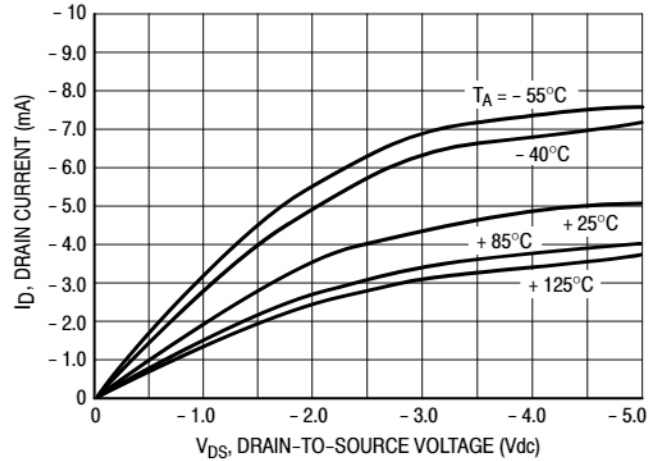
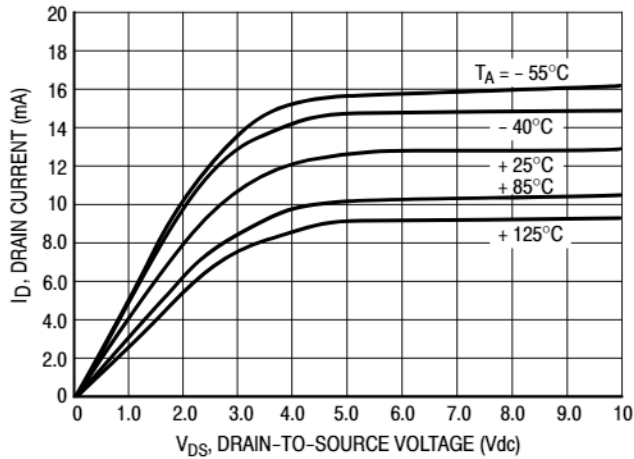
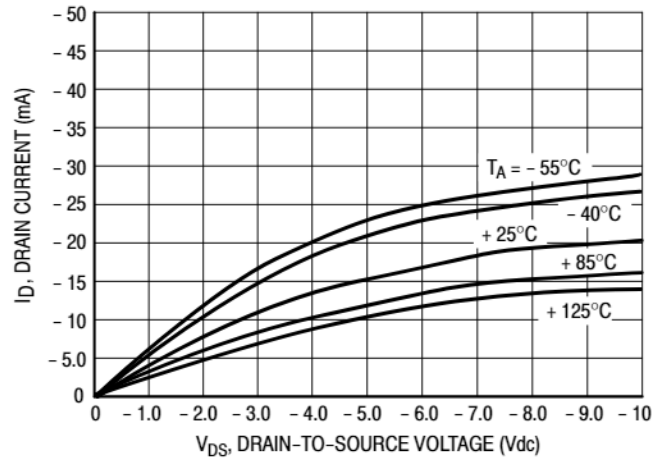
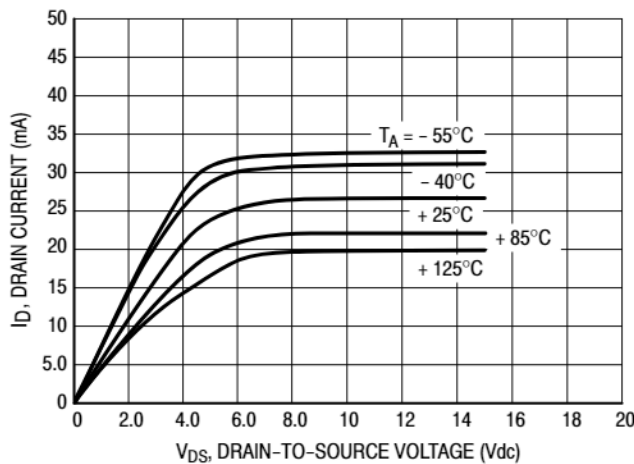
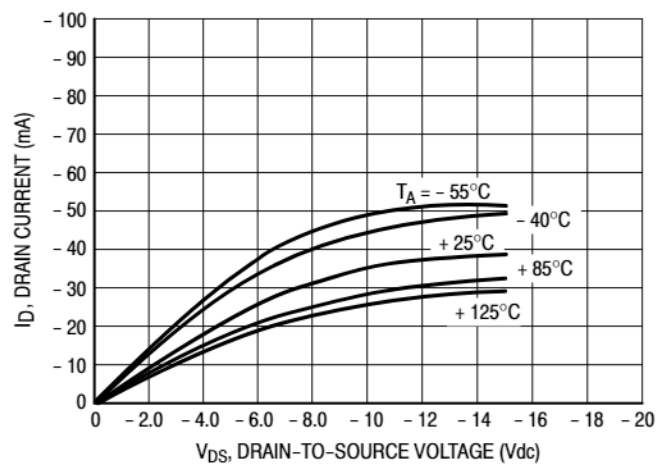
*Inverter omitted in MC14011B

TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

Figure 2. $V_{GS} = 5.0$ Vdc

P-CHANNEL DRAIN CURRENT (SOURCE)

Figure 3. $V_{GS} = -5.0$ VdcFigure 4. $V_{GS} = 10$ VdcFigure 5. $V_{GS} = -10$ VdcFigure 6. $V_{GS} = 15$ VdcFigure 7. $V_{GS} = -15$ Vdc

These typical curves are not guarantees, but are design aids.
 Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

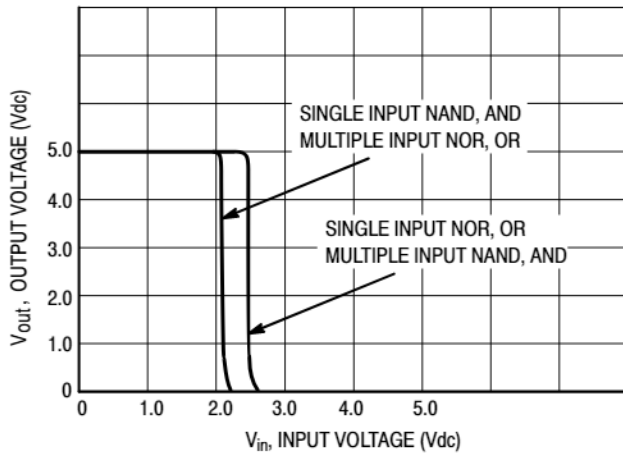


Figure 8. $V_{DD} = 5.0 \text{ Vdc}$

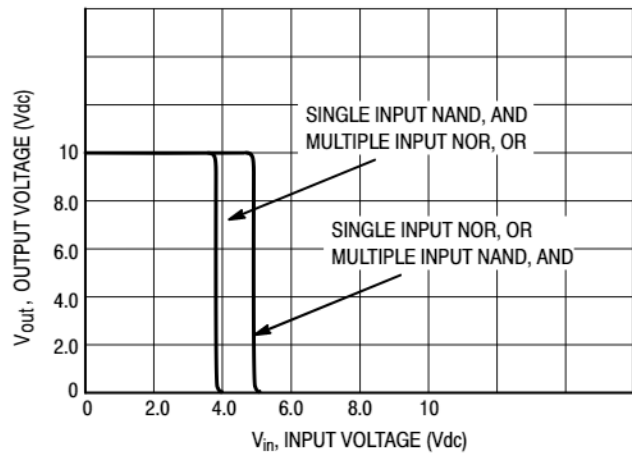


Figure 9. $V_{DD} = 10 \text{ Vdc}$

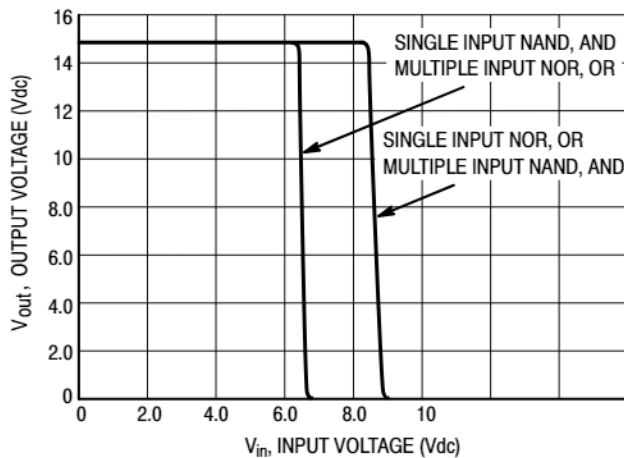


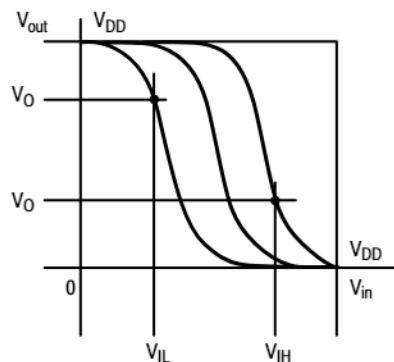
Figure 10. $V_{DD} = 15 \text{ Vdc}$

DC NOISE MARGIN

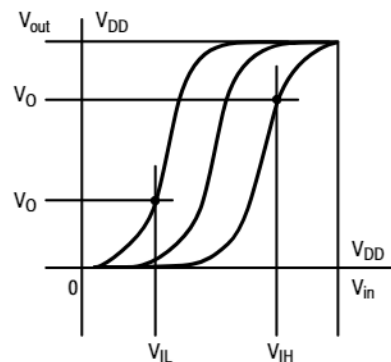
The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply



(a) Inverting Function



(b) Non-Inverting Function

$V_{SS} = 0 \text{ VOLTS DC}$

Figure 11. DC Noise Immunity

MC14001B Series

ORDERING INFORMATION

Device	Package	Shipping†
MC14001BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14001BDG*		
MC14001BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14001BDR2G*		
MC14001BDTR2G	TSSOP-14 (Pb-Free)	
NLV14001BDTR2G*		
MC14001BFELG	SOEIAJ-14 (Pb-Free)	2000 Units / Tape & Reel

MC14011BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14011BDG*		
MC14011BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14011BDR2G*		
MC14011BDTR2G	TSSOP-14 (Pb-Free)	
NLV14011BDTR2G*		
MC14011BFG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC14011BFELG		2000 Units / Tape & Reel

MC14023BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14023BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14023BDR2G*		
MC14023BFELG	SOEIAJ-14 (Pb-Free)	2000 Units / Tape & Reel

MC14025BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14025BDG*		
MC14025BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14025BDR2G*		

MC14071BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14071BDG*		
MC14071BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14071BDR2G*		
MC14071BDTG	TSSOP-14 (Pb-Free)	96 Units per Rail
MC14071BDTR2G		2500 Units / Tape & Reel
NLV14071BDTR2G*		

MC14073BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14073BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel

MC14001B Series

ORDERING INFORMATION (continued)

Device	Package	Shipping†
MC14081BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14081BDG*		
MC14081BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
NLV14081BDR2G*		
MC14081BDTR2G	TSSOP-14 (Pb-Free)	
NLV14081BDTR2G*		

MC14082BDG	SOIC-14 (Pb-Free)	55 Units / Rail
NLV14082BDG*		
MC14082BDR2G		2500 Units / Tape & Reel

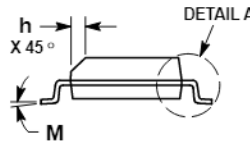
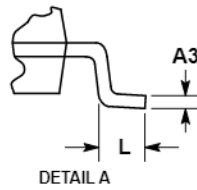
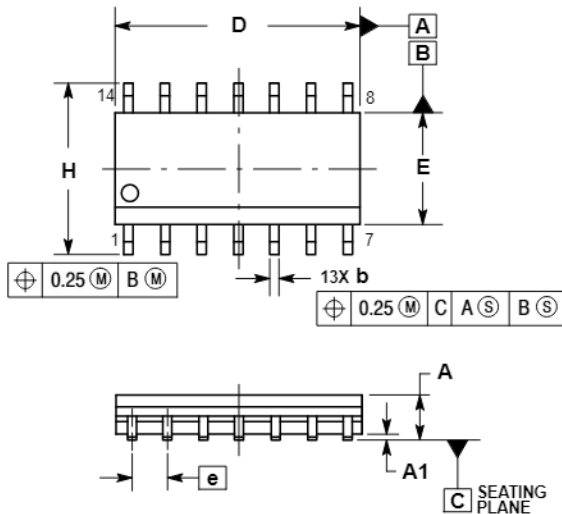
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14001B Series

PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K

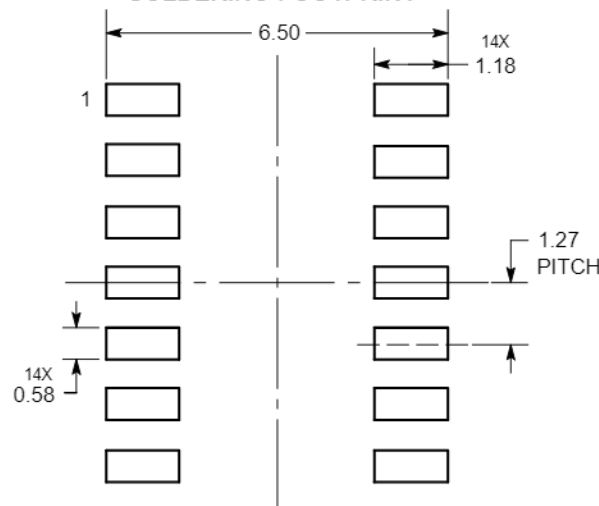


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative