D2900, JANUARY 1986 – REVISED MARCH 1988

- **Provides Control for 16K, 64K, and 256K Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **48-Pin Dual-In-Line Package**

description

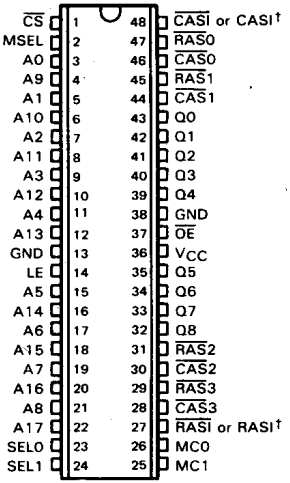
The 'ALS2967 and 'ALS2968 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS2967 offers active-low Row Address Strobe Input ($\overline{RASI}$) and Column Address Strobe Input ($\overline{CASI}$), while the 'ALS2968 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

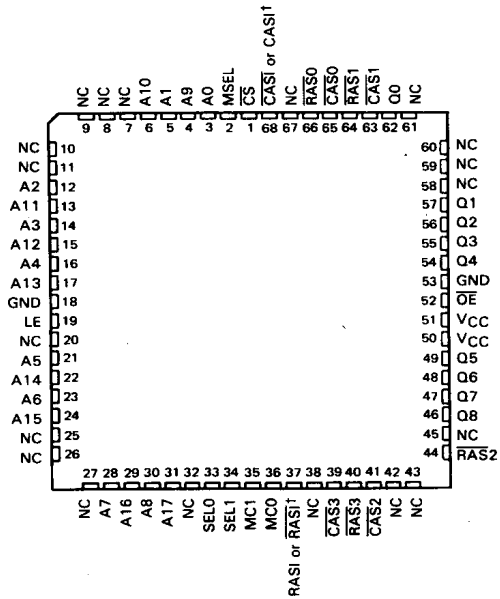
Using two 9-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 256K. These latches and the two row/column refresh address counters feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{RAS}$ and $\overline{CAS}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS2967 and 'ALS2968 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

SN74ALS2967, SN74ALS2968 . . . JD OR N PACKAGE
(TOP VIEW)



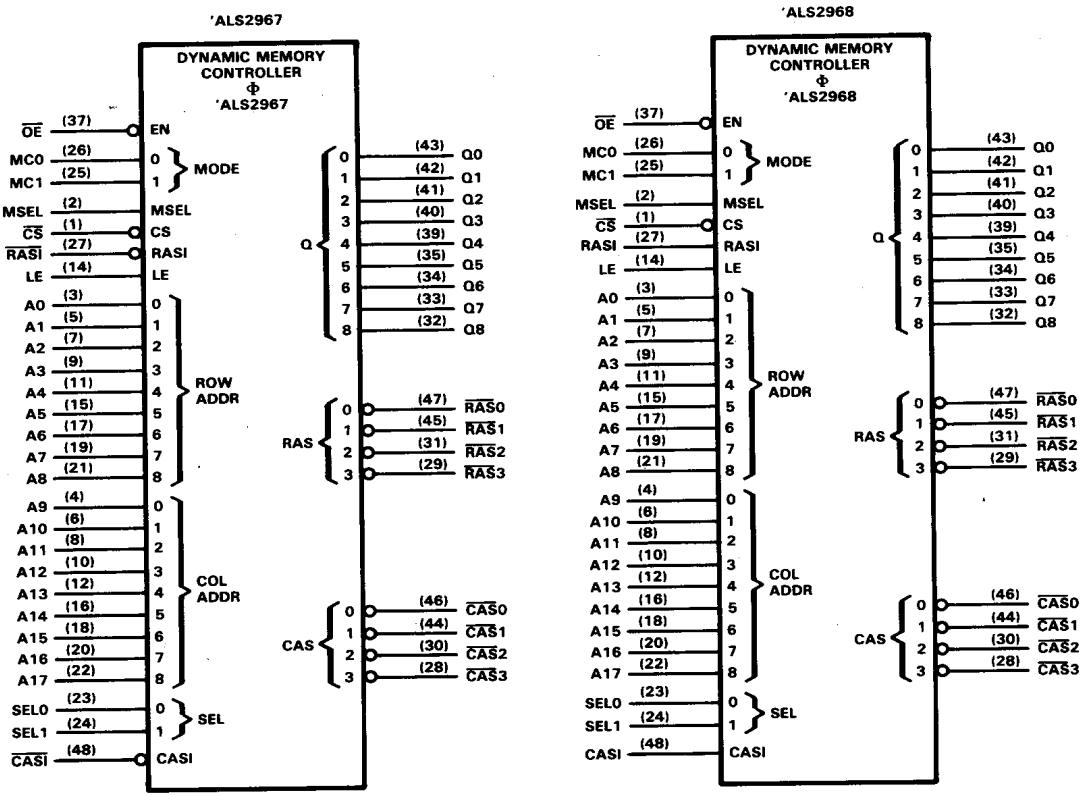
SN74ALS2967, SN74ALS2968 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
† 'ALS2967 has active-low inputs $\overline{CASI}$ and $\overline{RASI}$; 'ALS2968 has active-high inputs CASI and RASI.

The SN74ALS2967 and SN74ALS2968 are characterized for operation from 0°C to 70°C.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

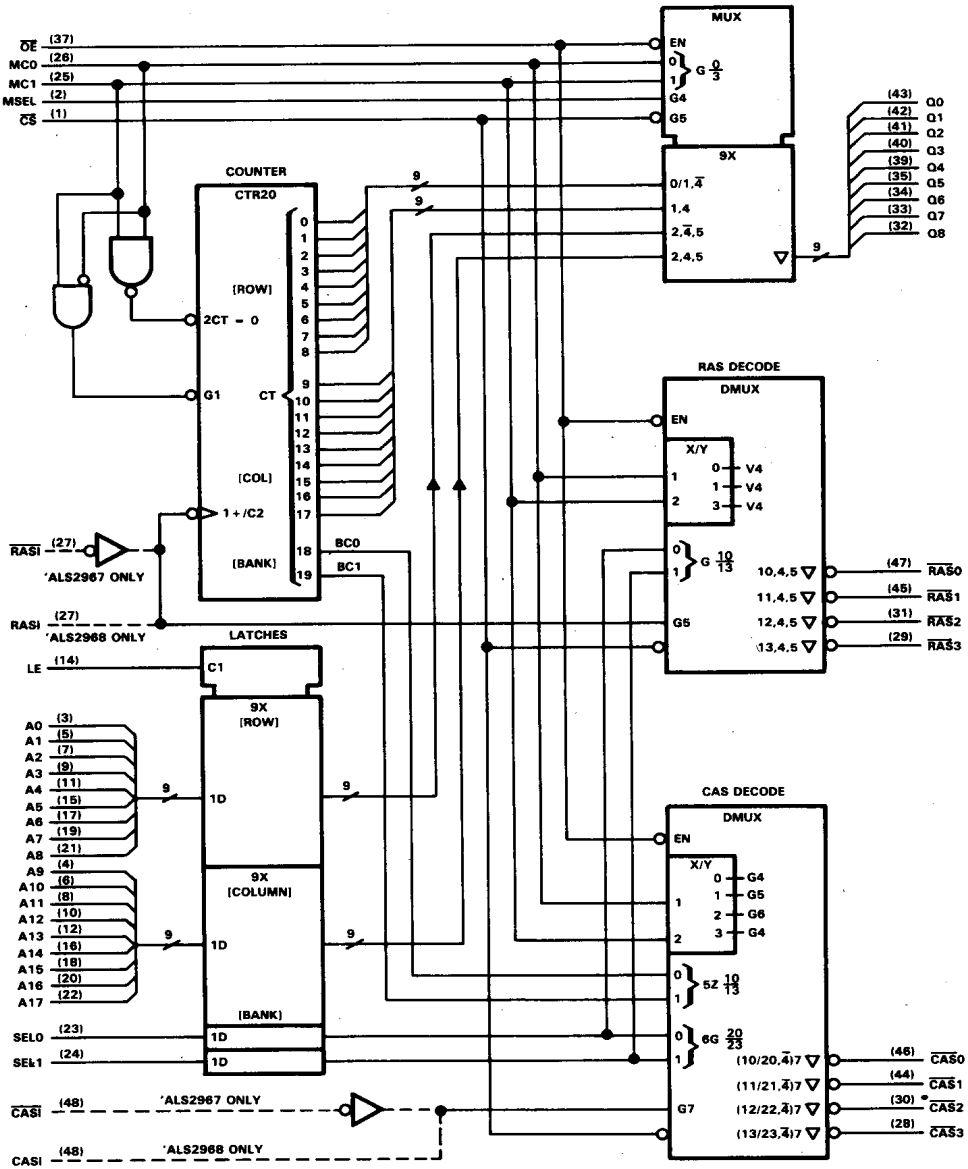


TABLE 1. PIN FUNCTION

PIN NAME	DESCRIPTION
A0-A17	Address Inputs. A0-A8 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q8 when the DMC is in the read/write mode and MSEL is low. A9-A17 are latched in as the column address, and will drive Q0-Q8 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
SEL0, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the $\overline{RAS}$ and $\overline{CAS}$ signals after $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) and $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968) go active.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MC0 and MC1 (see Mode Control Function Table).
$\overline{CS}$	Chip Select. This active-low input is used to enable the DMC. When $\overline{CS}$ is active, the DMC operates normally in all four modes. When $\overline{CS}$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
$\overline{OE}$	Output Enable. This active-low input enables/disables the output signals. When $\overline{OE}$ is high, the outputs of the DMC enter the high-impedance state.
MC0-MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
Q0-Q8	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
$\overline{RASI}$ or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded $\overline{RAS}$n output ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, or $\overline{RAS3}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four $\overline{RAS}$ outputs will be low while the Row Address Strobe Input signal is active. The $\overline{RASI}$ on the 'ALS2967 is an active-low input while on the 'ALS2968, RASI is an active-high input. (For more details see timing diagrams).
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a $\overline{RAS}$ signal to one of the four banks of dynamic memory. Each $\overline{RAS}$n output will go low when selected by SEL0 and SEL1 after $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) goes active. All four go low in response to $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) while in the refresh mode.
$\overline{CASI}$ or CASI	Column Address Strobe Input. This input going active causes the selected $\overline{CAS}$ output to be forced low. The $\overline{CASI}$ input on the 'ALS2967 is active low input while on the 'ALS2968, CASI is active high input. (For more details see timing diagrams.)
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SEL0, SEL1) determine which $\overline{CAS}$ output will go active following $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968) going active. When memory scrubbing is being performed, only the $\overline{CAS}$n signal selected will be active. For non-scrubbing cycles, all four $\overline{CAS}$ outputs will remain high.

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TABLE 2. MODE-CONTROL FUNCTION TABLE

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS2967) or CASI ('ALS2968). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active. The refresh counter is disabled while in this mode.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS2967) or RASI ('ALS2968) so that DRAM wake-up cycles may also be performed.

TABLE 3. ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q8
	MC1	MC0	MSEL	$\overline{CS}$	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address†
			H	L	Column address†
			X	H	All L
Clear refresh counter‡	H	H	X	X	All L

TABLE 4. RAS OUTPUT FUNCTIONS

INPUTS							OUTPUTS			
'ALS2967 $\overline{RASI}$	'ALS2968 RASI	MC1	MC0	SEL1†	SEL0†	$\overline{CS}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	H
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

TABLE 5. CAS OUTPUT FUNCTIONS

INPUTS									OUTPUTS			
'ALS2967 $\overline{CASI}$	'ALS2968 CASI	MC1	MC0	SEL1†	SEL0†	INTERNAL BC1	INTERNAL BC0	$\overline{CS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

† If LE is low, outputs will be the levels entered when LE was last high. If LE is high, outputs will follow address inputs as selected by MSEL.
‡ For 'ALS2967, clearing occurs on the low-to-high transition of $\overline{RASI}$; for 'ALS2968, clearing occurs on the high-to-low transition of RASI.

read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a one-megaword dynamic memory. The DMC is used to control the four banks of 256K memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches, (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

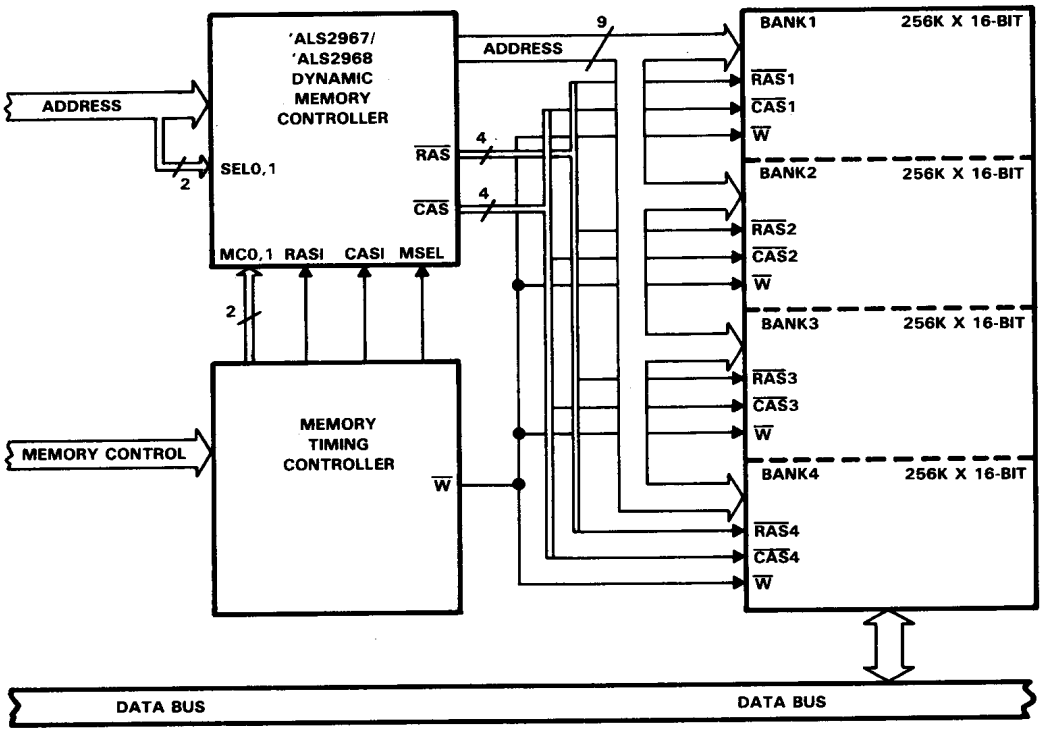

FIGURE 1. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level (V_{CC} – 1.5 V).

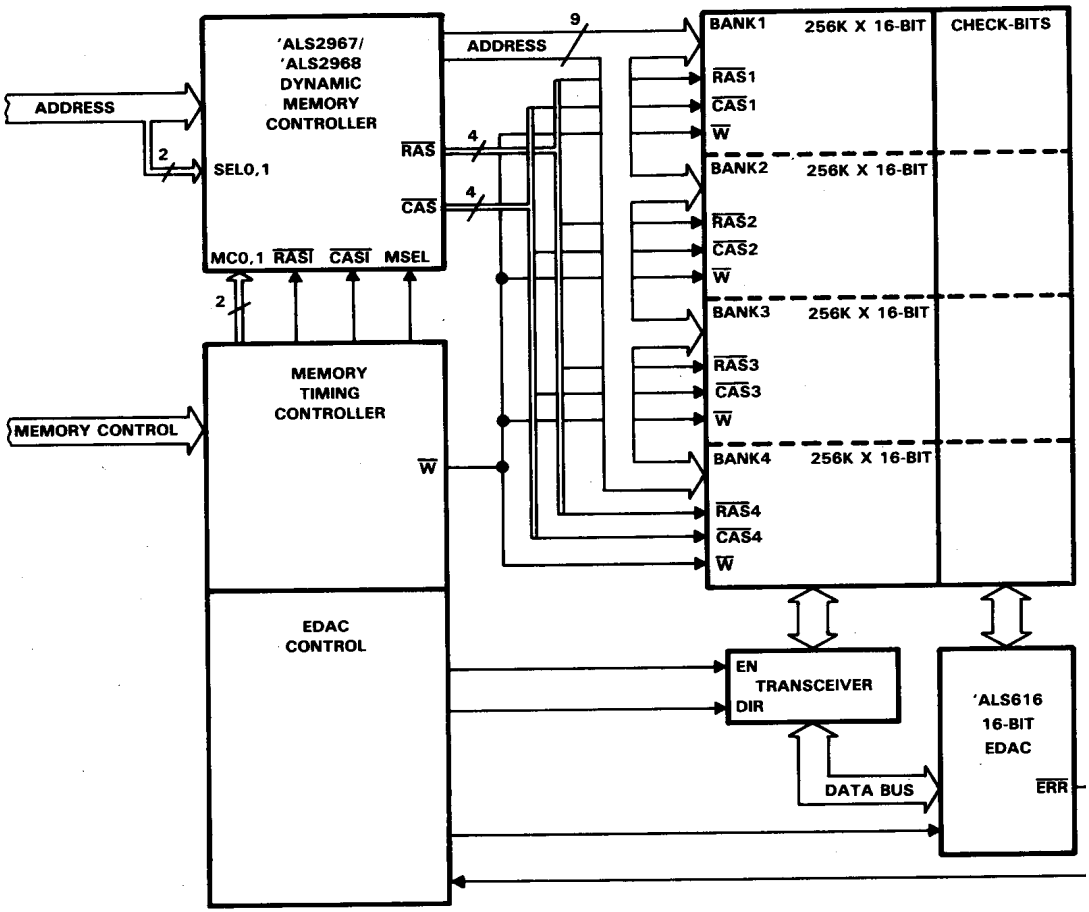

FIGURE 2. 1-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

memory expansion

With a 9-bit address path, the DMC can control up to one megaword when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to expand the memory size by using additional DMCs. A four-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

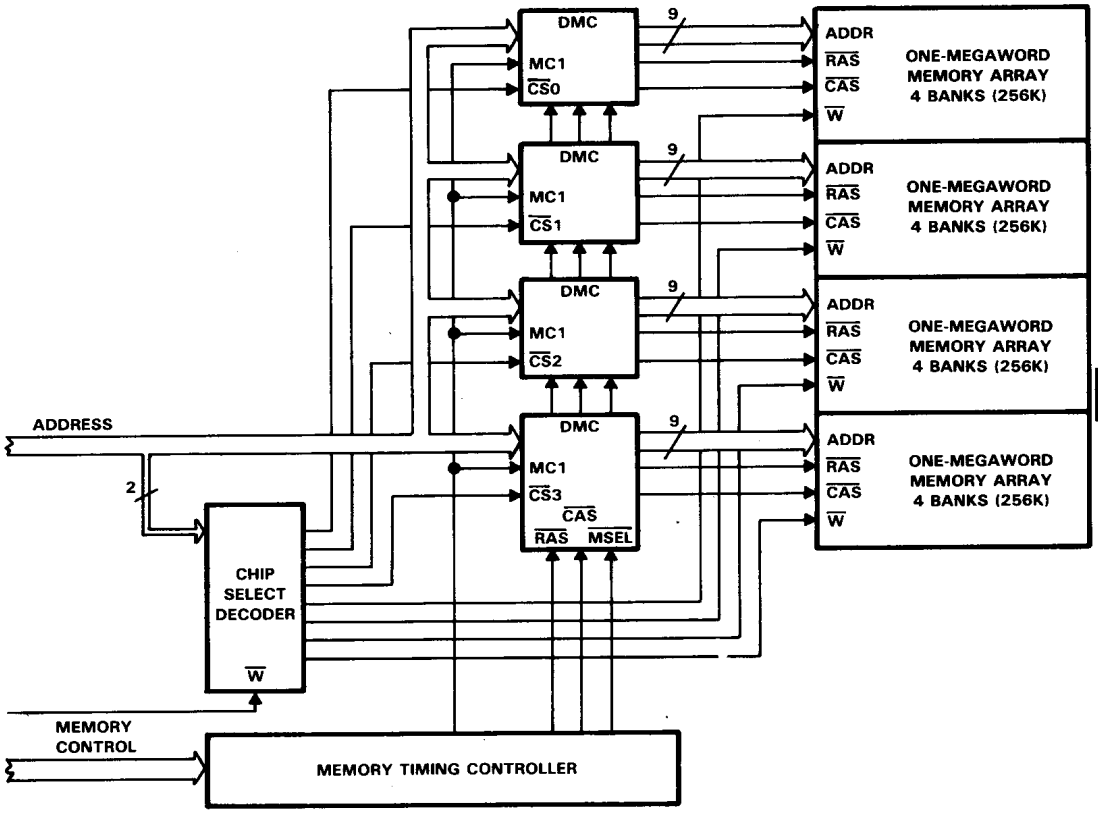

FIGURE 3. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

refresh operations

The two 9-bit counters in the 'ALS2967 and 'ALS2968 support 128-, 256-, and 512-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of RASI on the 'ALS2968. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS2967, and on the high-to-low transition of RASI on the 'ALS2968, if MC1 and MC0 are at a high logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MC0 both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

decoupling

Due to the high switching speed and high drive capability of the 'ALS2967 and 'ALS2968, it is necessary to decouple the device for proper operation. Multilayer ceramic 0.1 μF to 1 μF capacitors are recommended for decoupling. It is important to mount the capacitors as close as possible to the power pins (V_{CC} and GND) to minimize lead inductance and noise. A ground plane is recommended.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	(23) $\overline{RASI}$ low or RASI high	15			ns
		(24) $\overline{RASI}$ high or RASI low	15			
		(25) LE high	20			
t_{su}	Setup time	(26) An before LE↓	5			ns
		(27) SELn before LE↓	5			
		(28) MC0 or MC1 before $\overline{RASI}$↑ or RASI↓	25			
		(29) SELn before $\overline{RASI}$↓ or RASI↑	15			
t_h	Hold time	(30) An after LE↓	5			ns
		(31) SELn after LE↓	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OL}‡	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,			136	200	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and duration should not exceed 1 second.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RAS}$I or RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	9	18	25	ns
$t_{pd(2)}$	$\overline{RAS}$I or RASI	$\overline{RAS}$n		3	10	18	ns
$t_{pd(3)}$	$\overline{CAS}$I or CASI	$\overline{CAS}$n		3	9	17	ns
$t_{pd(4)}$	Any A	Any Q		3	9	18	ns
$t_{pd(5)}$	MSEL	Any Q		3	12	20	ns
$t_{pd(6)}$	LE↑	Any Q			13	25	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	25	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		7	13	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		3	10	21	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		3	9	19	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	23	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	20	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	19	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	20	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			11	18	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	19	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			11	19	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			11	19	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			10	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			10	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			9	20	ns

switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RAS}$I or RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	12	20	27	ns
$t_{pd(2)}$	$\overline{RAS}$I or RASI	$\overline{RAS}$n		5	12	23	ns
$t_{pd(3)}$	$\overline{CAS}$I or CASI	$\overline{CAS}$n		4	12	22	ns
$t_{pd(4)}$	Any A	Any Q		5	12	20	ns
$t_{pd(5)}$	MSEL	Any Q		8	15	26	ns
$t_{pd(6)}$	LE↑	Any Q			15	27	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			15	28	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			16	27	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		7	14	28	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	12	25	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		4	11	23	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			14	27	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			11	22	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			12	22	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			13	23	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			13	22	ns

† See Figures 10, 11, 12, and 13 for test circuit and switching waveforms.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

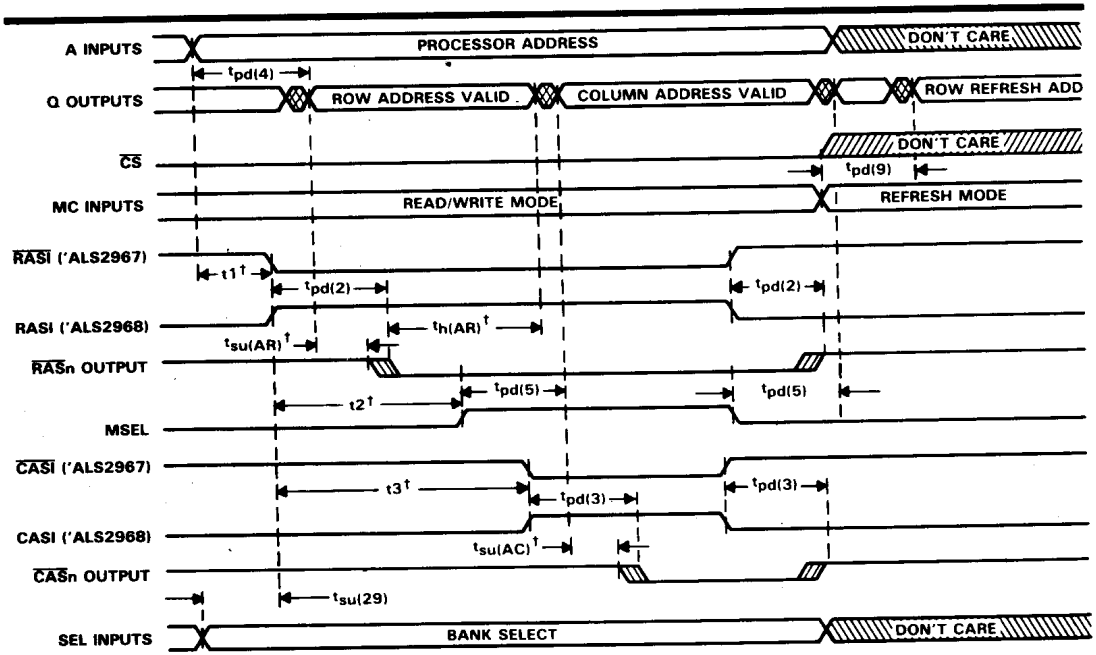

FIGURE 4. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t1, t2, and t3 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for t1, t2, and t3 are as follows:

$t1(min) = t_{pd(4)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$
$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AR)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

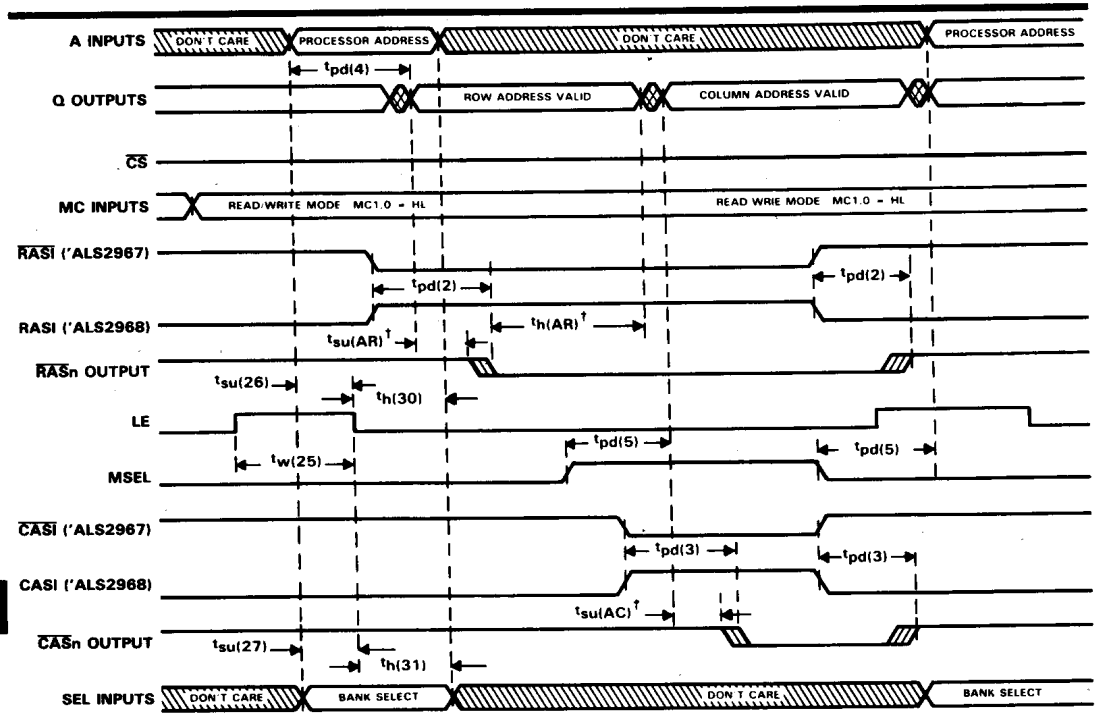

FIGURE 5. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MC0 = H, L)

† $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

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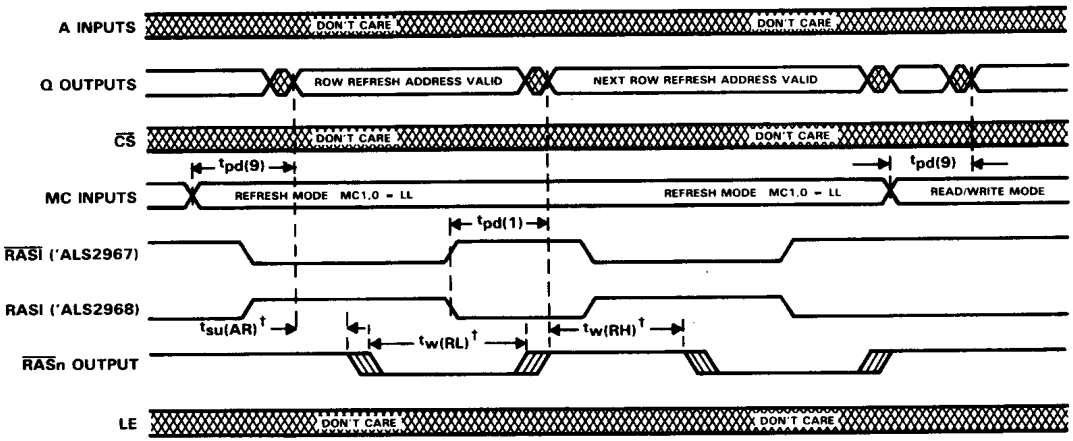


FIGURE 6. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

† $t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

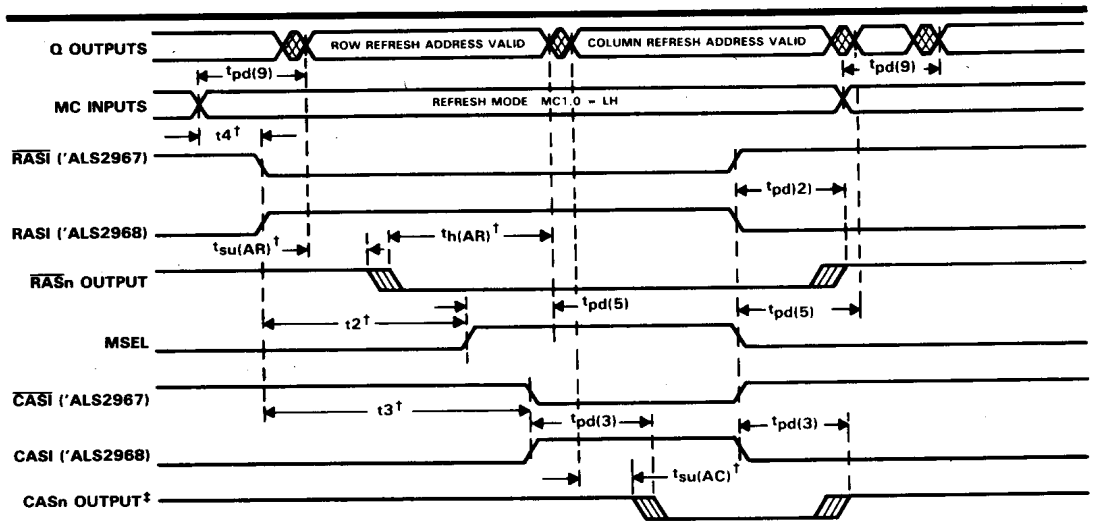


FIGURE 7. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t2, t3, and t4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t2, t3, and t4 are as follows:

$$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$$
$$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$$
$$t4(min) = t_{pd(9)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

‡ A $\overline{CAS}$n output is selected by the bank counter. All other $\overline{CAS}$n outputs will remain high.

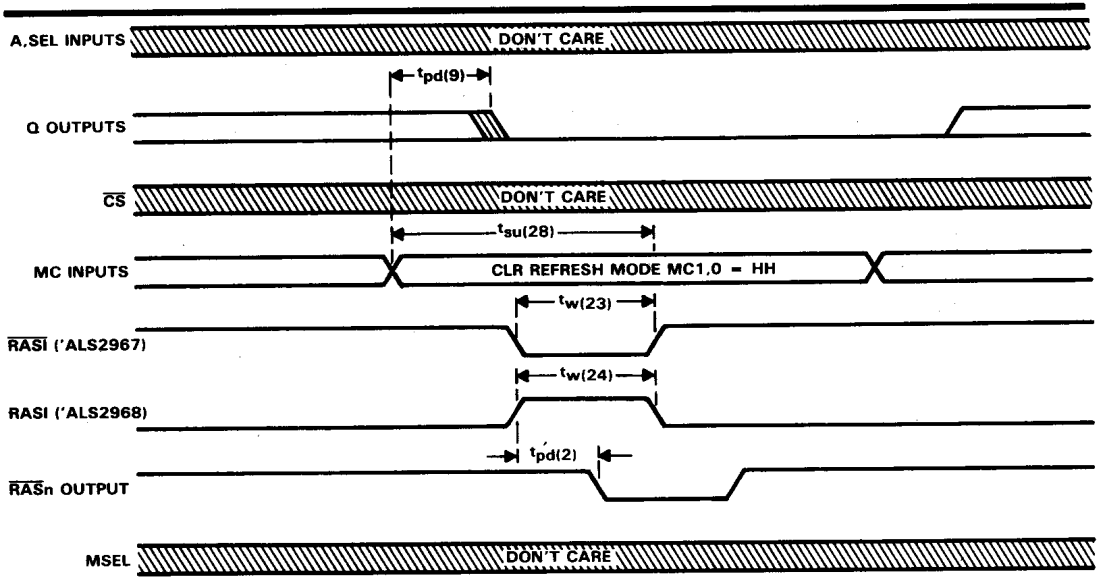
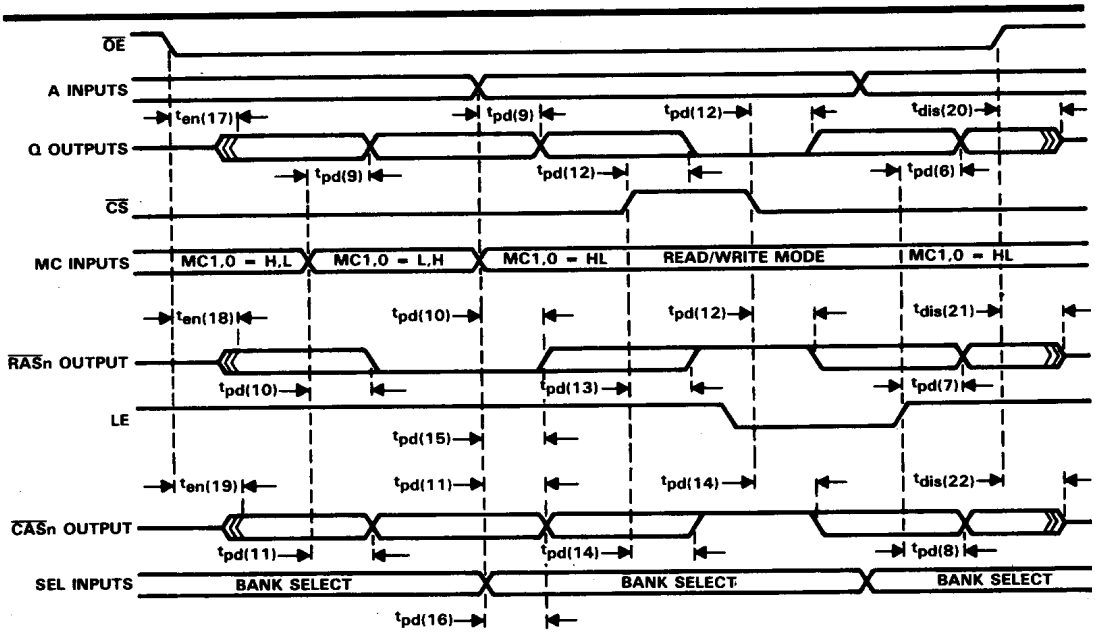


FIGURE 8. REFRESH COUNTER RESET (MC1, MC0 = H, H)



$\overline{RASI}$ ('ALS2967) = L, RASI ('ALS2968) = H, MSEL = H or L, $\overline{CASI}$ ('ALS2967) = L, CASI ('ALS2968) = H

FIGURE 9. MISCELLANEOUS TIMING

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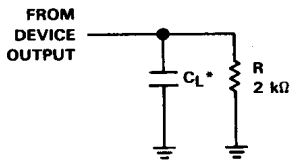
SWITCHING TEST CIRCUIT



* t_{pd} specified at C_L = 50, 150 pF

FIGURE 10. CAPACITIVE LOAD SWITCHING

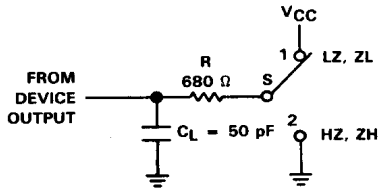
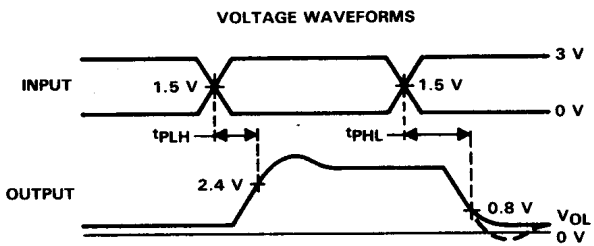


FIGURE 11. THREE-STATE ENABLE/DISABLE

TYPICAL SWITCHING CHARACTERISTICS



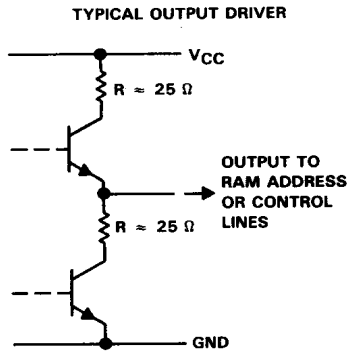
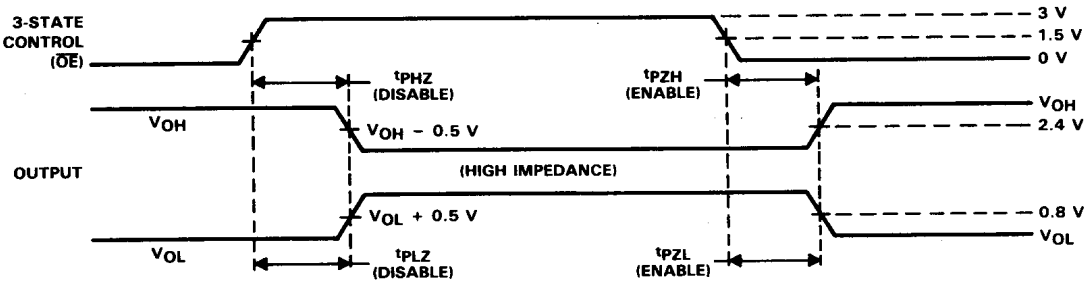


FIGURE 12. OUTPUT DRIVE LEVELS

THREE-STATE TIMING



NOTE: Decoupling is needed for all AC tests

FIGURE 13. THREE-STATE CONTROL LEVELS