PLL620-38/39

PECL and LVDS Low Phase Noise XO (32.5 to 130MHz output)

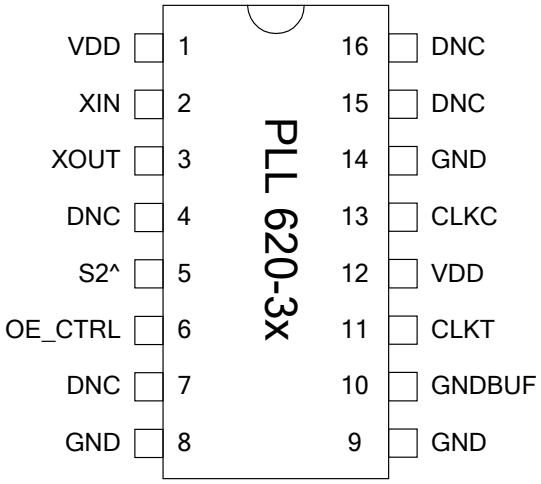
FEATURES

- 65MHz to 130MHz Crystal input.
- Output range: 32.5MHz – 130MHz (no PLL).
- Low Injection Power for crystal, 50uW.
- PECL (PLL620-38) or LVDS output (PLL620-39).
- Supports 2.5V or 3.3V-Power Supply.
- Available in 16-Pin TSSOP.

DESCRIPTION

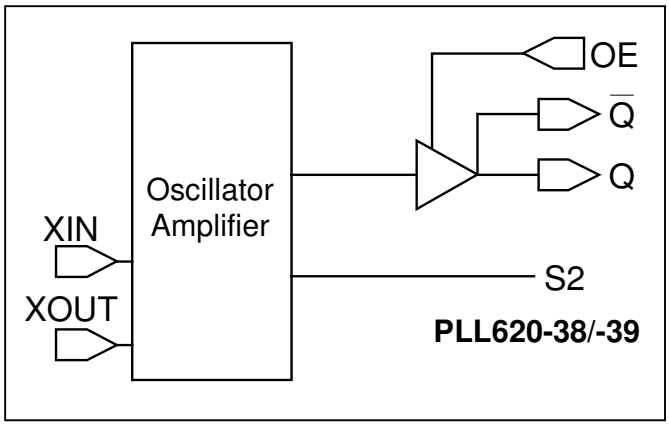
The PLL620-38/-39 is a family of XO IC's specifically designed to work with high frequency fundamental or 3rd OT crystals from 65MHz to 130MHz, with selectable PECL or LVDS outputs. They achieve very low current into the crystal resulting in better overall stability. Their very low jitter makes them ideal for the most demanding timing requirements.

PIN CONFIGURATION



Note: ^ designates internal pull-up resistor.

BLOCK DIAGRAM



OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL620-38	0 (Default)	Output enabled
	1	Tri-state
PLL620-39	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL620-38
Logical states defined by CMOS levels for PLL620-39

OUTPUT FREQUENCY SELECTOR

S2	Output
0	Input/2
1(Default)*	Input

*Internally set to 'Default' through 60KΩ pull-up resistor

PECL and LVDS Low Phase Noise XO (for 32.5-130MHz Output)

PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	2	I	Crystal input. See Crystal Specifications on page 2.
XOUT	3	I	Crystal output. See Crystal Specifications on page 2.
S2	5	I	When pulled low the output is equal to the input divided by 2. Internal pull up.
OE_CTRL	6	I	Output enable. See Output Enable Logic table on page 1.
GND	8, 14	P	Ground.
CLKT	11	O	True output PECL (PLL620-38) or LVDS (PLL620-39).
CLKC	13	O	Complementary output PECL (PLL620-38) or LVDS (PLL620-39).
DNC	4,7,10,15,16	-	Do Not connect.
VDD	1, 12	P	Power supply.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Loading Rating	$C_{L\ (xtal)}$	65MHz to 130MHz (VDD=3.3V)		8.5		pF
Inter-electrode capacitance	C_0			2.6		
Crystal Resonator Frequency	F_{XIN}	Fund.	65		130	MHz

PECL and LVDS Low Phase Noise XO (for 32.5-130MHz Output)

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS			100/80	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ V_{DD} – 1.3V (PECL)	45 45	50 50	55 55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	77.76MHz		2.5		ps
Period jitter peak-to-peak	77.76MHz		18.5		ps
Integrated jitter RMS	Integrated 12kHz to 20MHz at 77.76MHz		0.5		ps

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	77.76MHz	-75	-95	-125	-145	-155	dBc/Hz

PECL and LVDS Low Phase Noise XO (for 32.5-130MHz Output)

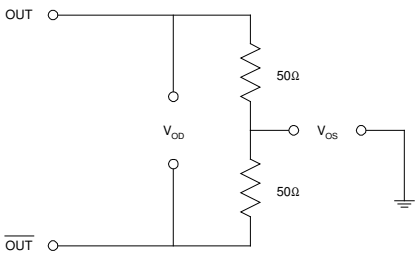
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

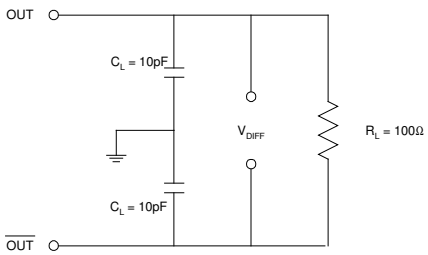
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

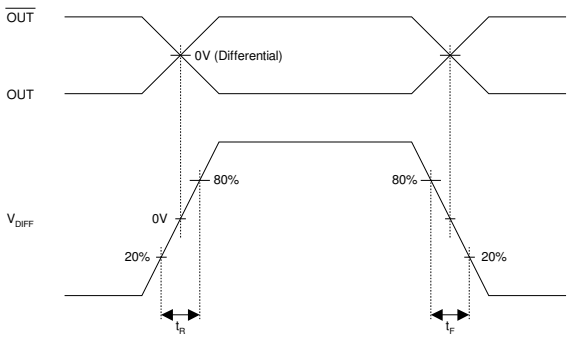
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



PECL and LVDS Low Phase Noise XO (for 32.5-130MHz Output)

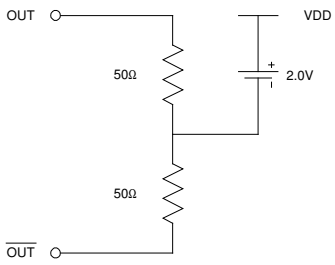
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

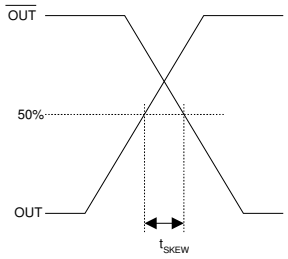
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

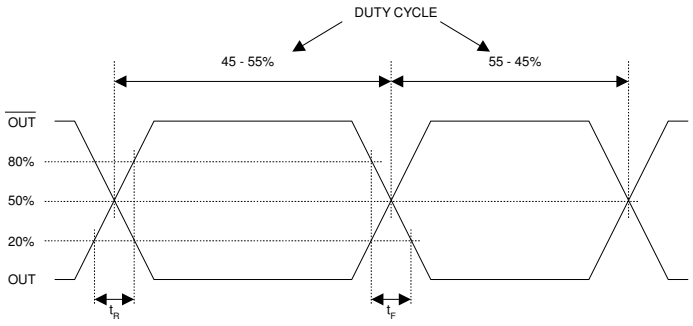
PECL Levels Test Circuit



PECL Output Skew



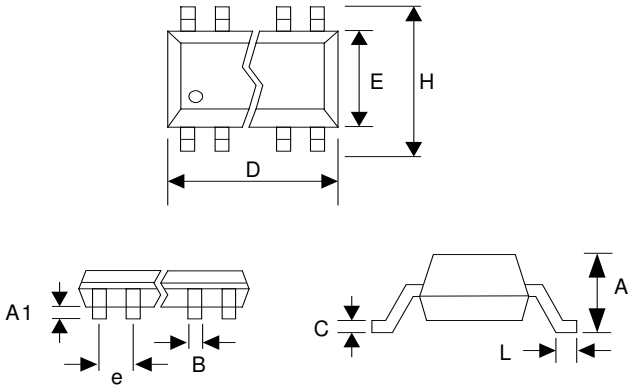
PECL Transition Time Waveform



PECL and LVDS Low Phase Noise XO (for 32.5-130MHz Output)

PACKAGE INFORMATION

16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL620-3X X X X R

PART NUMBER

FAMILY DESIGNATOR

PACKAGE TYPE
O= TSSOP

NONE= TUBE
R=TAPE AND REEL

NONE=NORMAL PACKAGE
L=GREEN PACKAGE

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Part / Order Number	Marking	Package Option
PLL620-3XOC	P620-3XDC	TSSOP - Tube
PLL620-3XOC-R	P620-3XSC	TSSOP (Tape and Reel)
PLL620-3XOCL	P620-3XSCL	TSSOP – Tube (GREEN)
PLL620-3XOCL-R	P620-3XSCL	TSSOP (Tape and Reel) (GREEN)