

74AHC30; 74AHCT30

8-input NAND gate

Rev. 03 — 26 June 2009

Product data sheet

1. General description

The 74AHC30; 74AHCT30 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC30; 74AHCT30 provides an 8-input NAND function.

2. Features

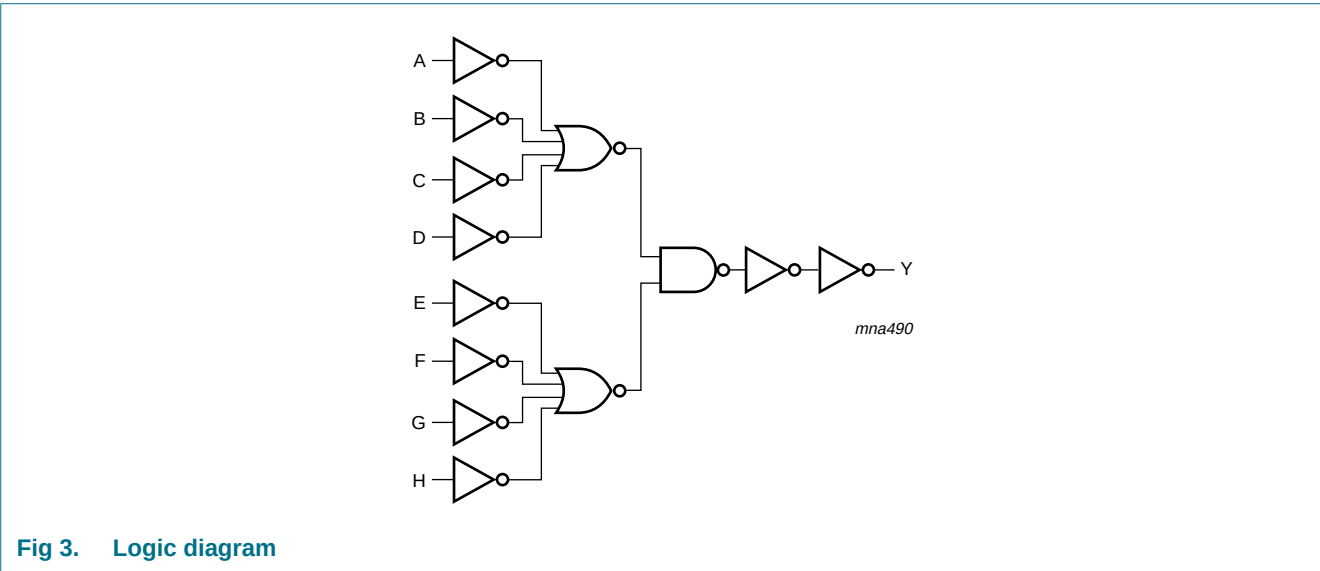
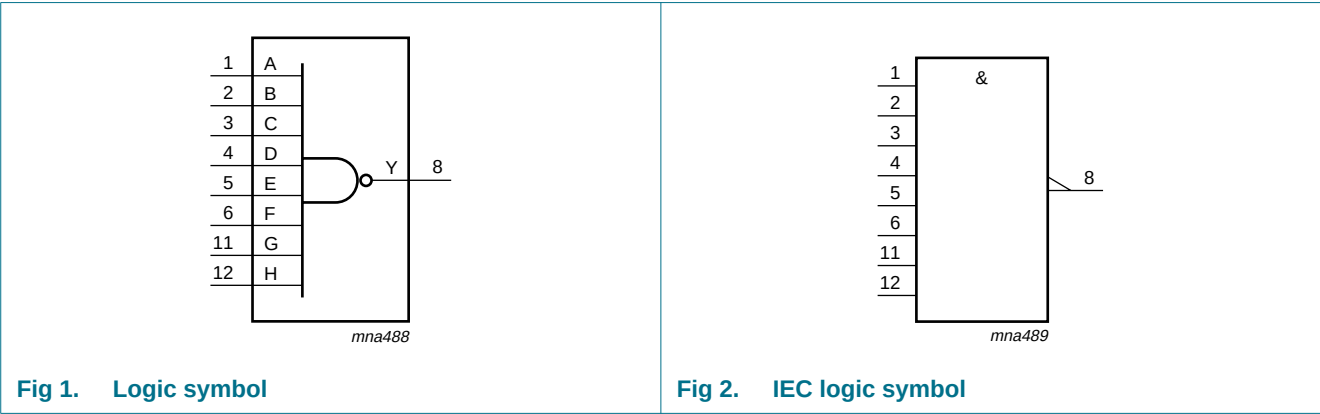
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ For 74AHC30: CMOS level
 - ◆ For 74AHCT30: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

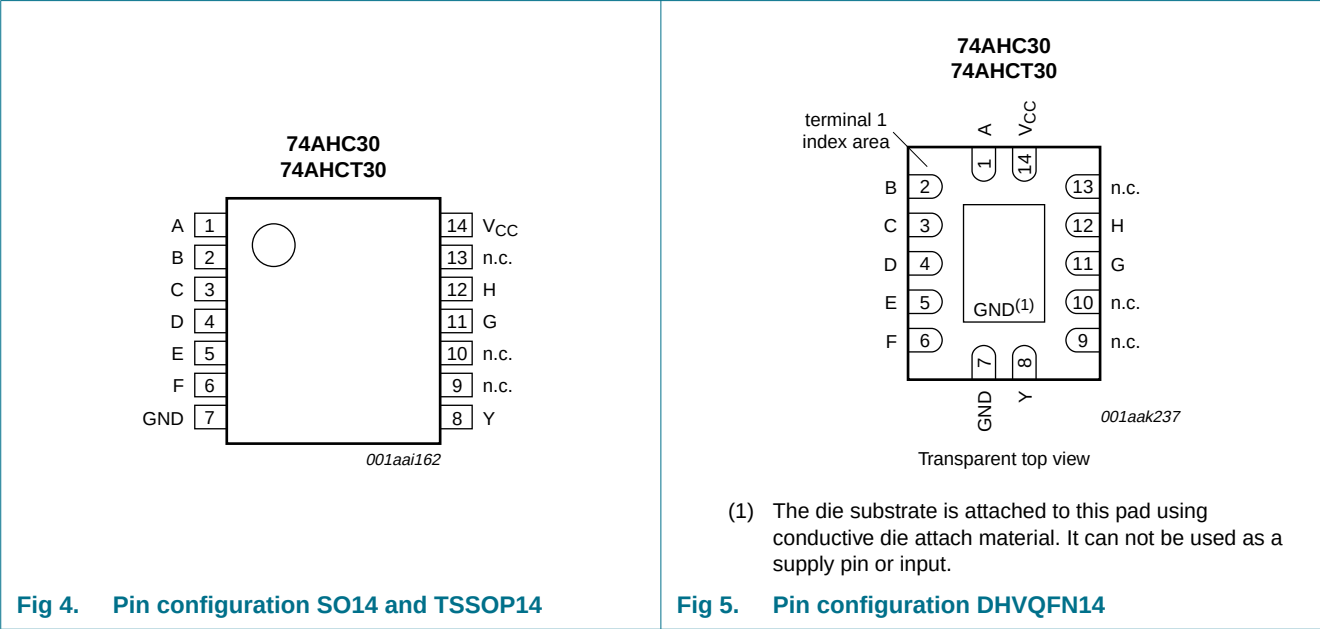
Type number	Package			
	Temperature range	Name	Description	Version
74AHC30D 74AHCT30D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC30PW 74AHCT30PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC30BQ 74AHCT30BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A	1	data input
B	2	data input
C	3	data input
D	4	data input
E	5	data input
F	6	data input
GND	7	ground (0 V)
Y	8	data output
n.c.	9	not connected
n.c.	10	not connected
G	11	data input
H	12	data input
n.c.	13	not connected
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input								Output
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
V _I	input voltage		−0.5	+7.0	V
I _{IK}	input clamping current	V _I < −0.5 V	^[1] −20	-	mA
I _{OK}	output clamping current	V _O < −0.5 V or V _O > V _{CC} + 0.5 V	^[1] −20	+20	mA
I _O	output current	V _O = −0.5 V to (V _{CC} + 0.5 V)	−25	+25	mA
I _{CC}	supply current		-	+75	mA
I _{GND}	ground current		−75	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	T _{amb} = −40 °C to +125 °C	^[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC30			74AHCT30			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC30										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = −50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V _{OL}	LOW-level output voltage	I _O = −8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
		V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
I _I	input leakage current	I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _O	output capacitance		-	4	-	-	-	-	-	pF
74AHCT30										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74AHC30										
t _{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; ^[2] see Figure 6 and 7								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.0	9.5	1.0	11.0	1.0	12.0	ns
		C _L = 50 pF	-	6.7	12.0	1.0	14.5	1.0	15.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.6	6.5	1.0	7.5	1.0	8.0	ns
		C _L = 50 pF	-	4.9	8.0	1.0	9.5	1.0	10.5	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC}	[3]	-	10	-	-	-	-	pF
74AHCT30; V_{CC} = 4.5 V to 5.5 V										
t _{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; [2] see Figure 6 and 7								
		C _L = 15 pF	-	3.3	6.5	1.0	7.5	1.0	8.0	ns
		C _L = 50 pF	-	4.7	8.5	1.0	9.5	1.0	10.5	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC}	[3]	-	12	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

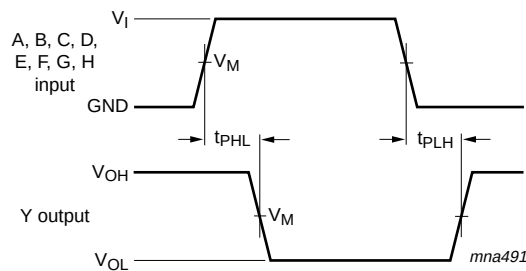
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11. Waveforms

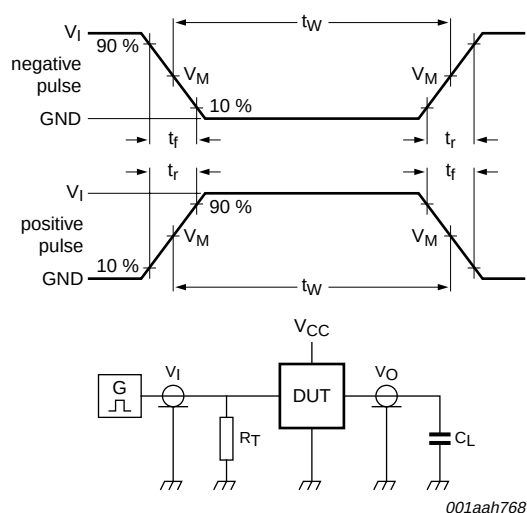


Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays**Table 8.** Measurement points

Type	Input	Output
	V _M	V _M
74AHC30	0.5 × V _{CC}	0.5 × V _{CC}
74AHCT30	1.5 V	0.5 × V _{CC}



Test data is given in Table 9.

Definitions for test circuit:

R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V _I	t _r , t _f	C _L	
74AHC30	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74AHCT30	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

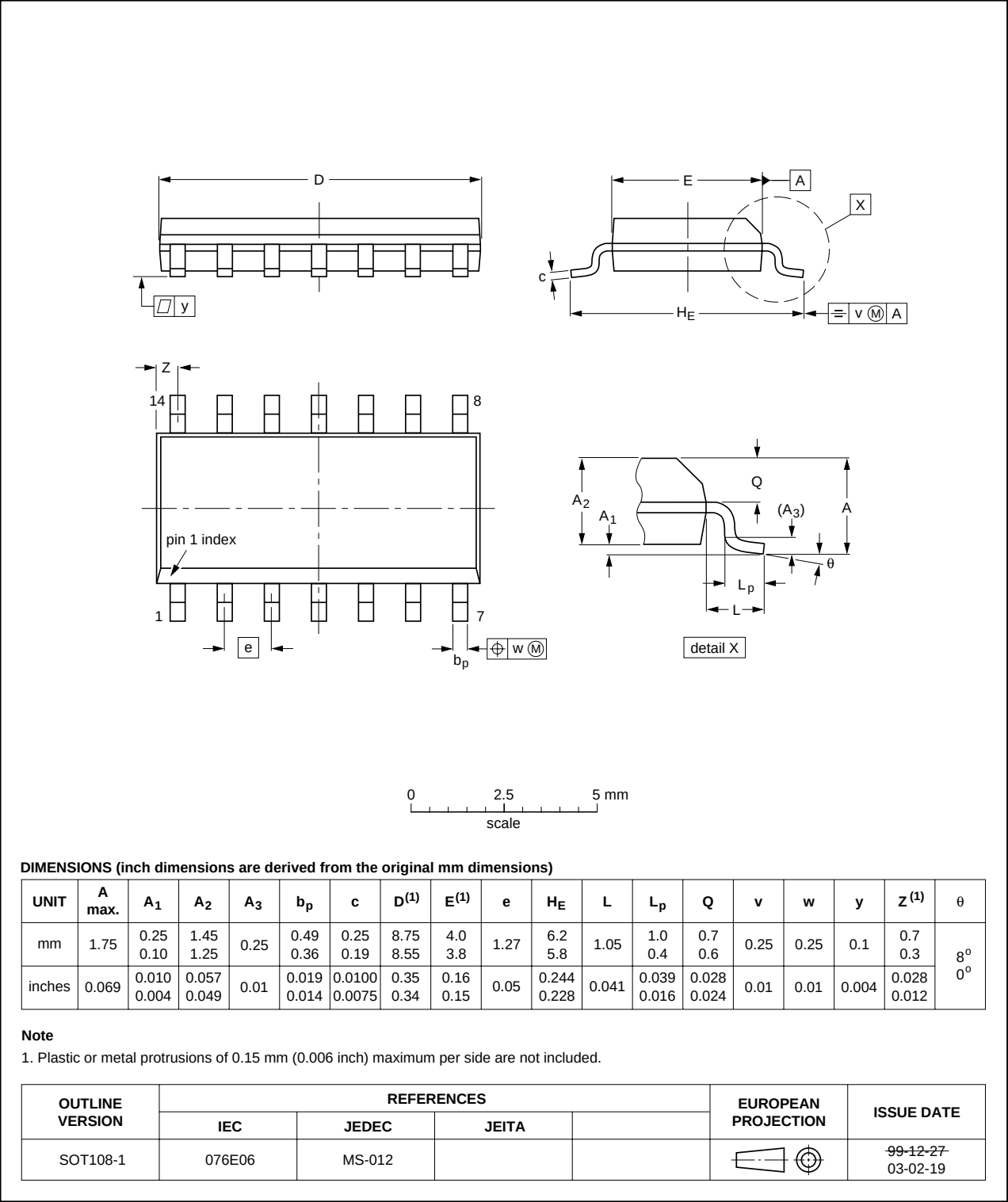


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

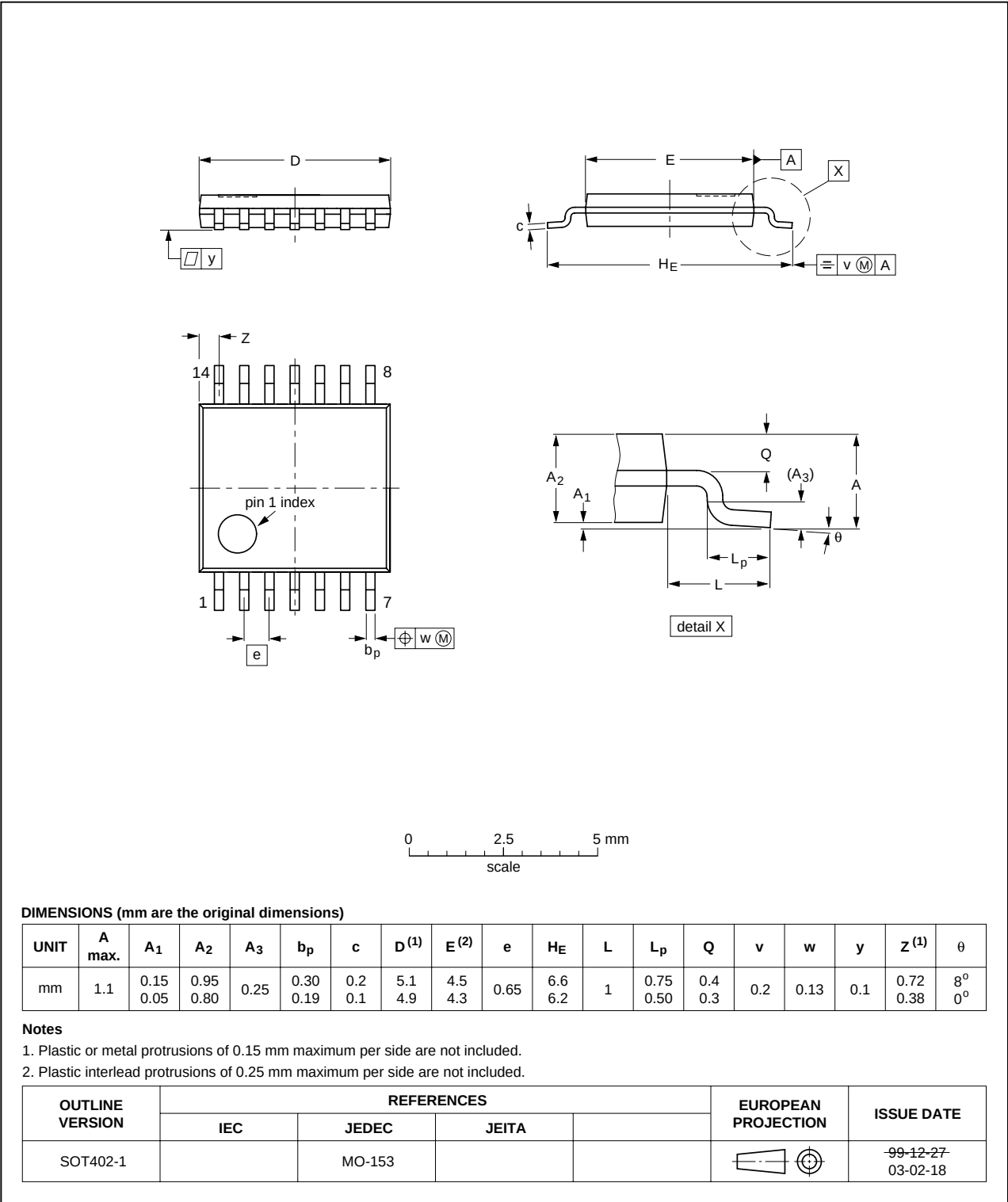


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

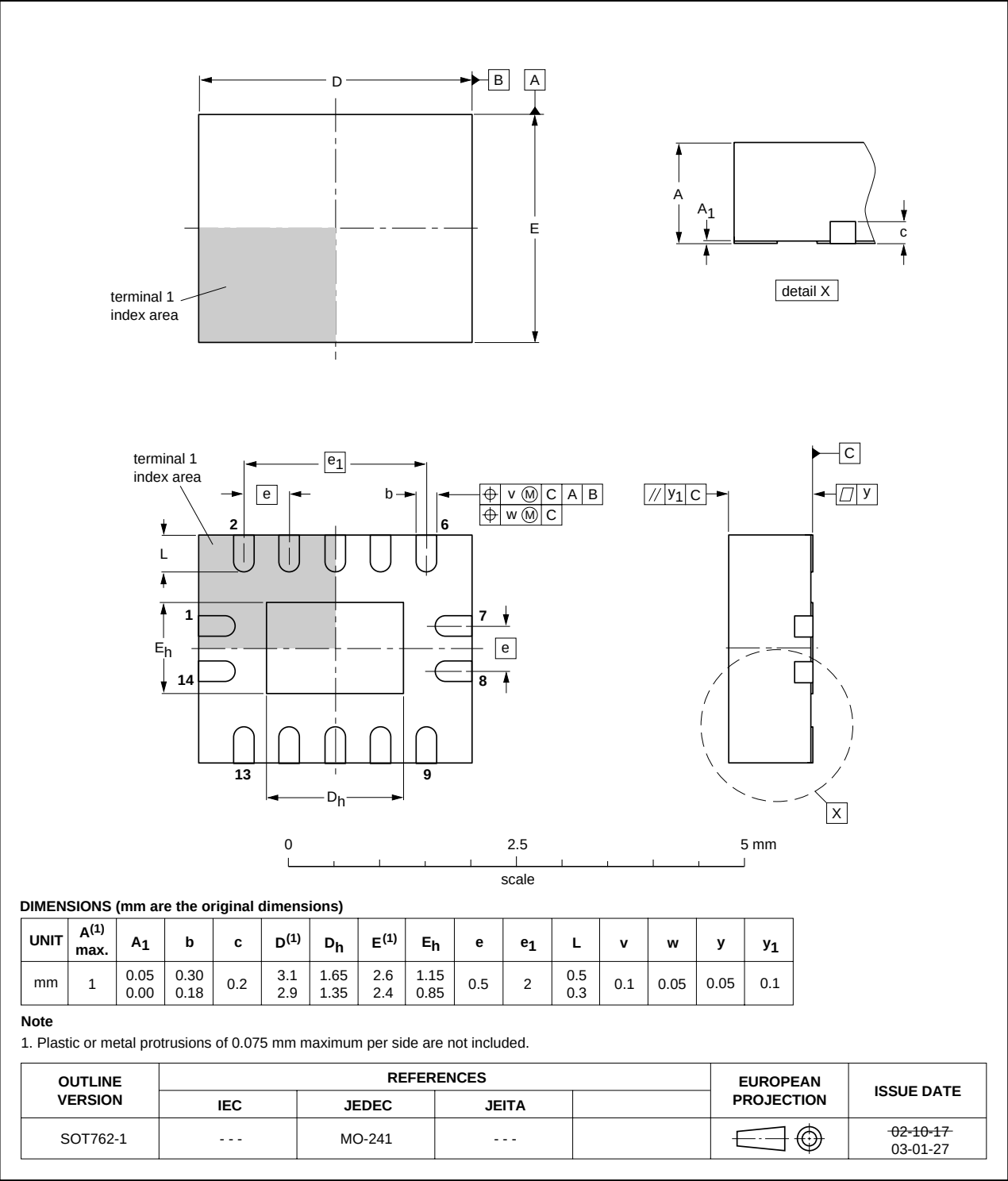


Fig 10. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT30_3	20090626	Product data sheet	-	74AHC_AHCT30_2
Modifications:	• Section 3: DHVQFN14 package added. • Section 7: derating values added for DHVQFN14 package. • Section 12: outline drawing added for DHVQFN14 package.			
74AHC_AHCT30_2	20080530	Product data sheet	-	74AHC_AHCT30_1
74AHC_AHCT30_1	19991130	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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