



500mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3984H is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3984H performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. The LP3984H also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3984H consumes less than 1 μ A in shutdown mode. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 packages.

Order Information

LP3984H	□□□□□	
		F: Pb-Free
		Package Type
		B5: SOT23-5
		Output Type
		18 : 1.8V
		25 : 2.5V
		28 : 2.8V
		30 : 3.0V
		33 : 3.3V
		36 : 3.6V

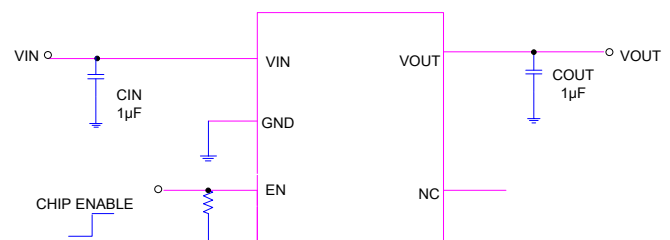
Features

- ◆ Ultra-Low-Noise for RF Application
- ◆ 2.5V- 5.5V Input Voltage Range
- ◆ Low Dropout : 300mV @ 300mA
- ◆ 500mA Output Current
- ◆ High PSRR:-68dB at 1KHz
- ◆ 1 μ A Standby Current When Shutdown
- ◆ Available in SOT23-5 Package
- ◆ TTL-Logic-Controlled Shutdown Input
- ◆ Ultra-Fast Response in Line/Load transient
- ◆ Current Limiting and Thermal Shutdown Protection

Applications

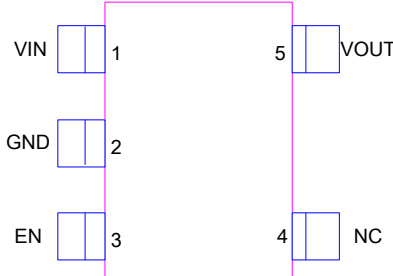
- ◇ Portable Media Players/MP3 players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

Typical Application Circuit





Functional Pin Description

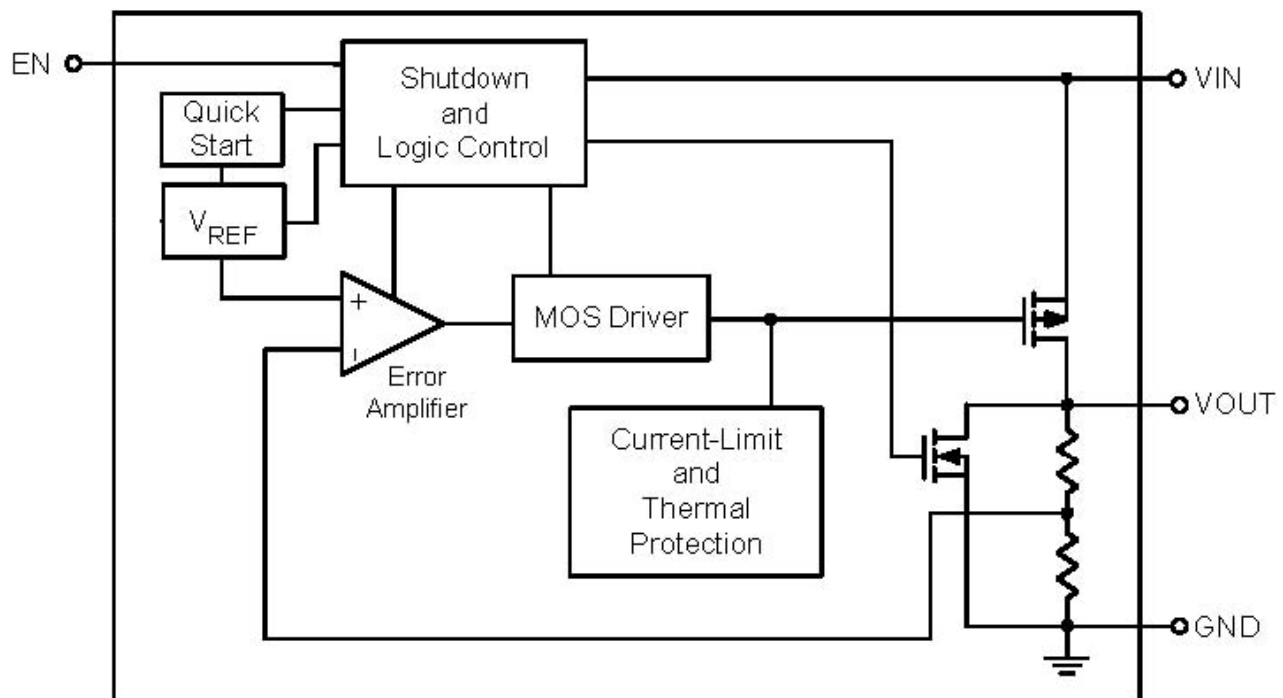
Package Type	Pin Configurations
SOT-23-5	Top View SOT23-5 

Pin Description

Pin	Name	Description
1	VIN	Power Input Voltage.
2	GND	Ground.
3	EN	Chip Enable (Active High).
4	NC	No Connection.
5	VOUT	Output Voltage.



Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ----- 6.5V
- ✧ Other Pin Voltage ----- -0.3V to $V_{IN}+0.3V$
- Power Dissipation, P_D @ $T_A = 25^\circ C$
- ✧ SOT23-5 ----- 500mW
- Package Thermal Resistance
- ✧ Thermal Resistance (SOT23-5) (J_A) ----- $195^\circ C/W$
- ✧ Thermal Resistance (SOT23-5) (J_C) ----- $60^\circ C/W$
- ✧ Maximum Junction Temperature ----- $150^\circ C$
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ----- $260^\circ C$
- ✧ Storage Temperature Range ----- $-65^\circ C$ to $150^\circ C$

ESD Susceptibility

- ✧ HBM (Human Body Mode) ----- 2kV
- ✧ MM (Machine-Mode) ----- 200V

Recommended Operating Conditions

- ✧ Supply Input Voltage ----- 2.5V to 5.5V
- ✧ EN Input Voltage ----- 0V to $V_{IN}+0.3V$
- ✧ Operation Junction Temperature Range ----- $-40^\circ C$ to $125^\circ C$
- ✧ Operation Ambient Temperature Range ----- $-40^\circ C$ to $85^\circ C$



Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	$I_{OUT}=1mA$	-2	--	+2	%
Output Loading Current		I_{LOAD}	$V_{EN}=V_{IN}, V_{IN}>2.8V$		500		mA
Quiescent Current		I_Q	$V_{EN}\geq 1.2V, I_{OUT}=0mA$		50	130	μA
Dropout Voltage		V_{DROP}	$I_{OUT}=200mA, V_{OUT}>2.8V$		200	240	mV
			$I_{OUT}=300mA, V_{OUT}>2.8V$		300	360	
Line Regulation		ΔV_{LINE}	$V_{IN}=(V_{OUT}+1V)$ to 5.5V, $I_{OUT}=50mA$			0.2	%/V
Load Regulation		ΔI_{LOAD}	$1mA<I_{OUT}<300mA$			2	%/A
Standby Current		I_{STBY}	$V_{EN}=GND$, Shutdown		1		μA
EN Input Bias Current		I_{BSD}	$V_{EN}=3V$		1		μA
EN Threshold	Logic-Low Voltage	V_{IL}	$V_{IN}=3V$ to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	$V_{IN}=3V$ to 5.5V, Start-Up	1.2			
Output Noise Voltage			10Hz to 100kHz, $I_{OUT}=200mA$, $C_{OUT}=1\mu F$		300		$\mu VRMS$
Power Supply Rejection Rate		PSRR	$C_{OUT}=1\mu F, f = 1kHz$, $I_{OUT}=100mA$		-68		dB
			$C_{OUT}=1\mu F, f = 10kHz$, $I_{OUT}=100mA$		-60		dB
Thermal Shutdown Temperature		T_{SD}			150		$^\circ C$



Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3984H must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the LP3984H input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3984H is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 25\text{m}\Omega$ on the LP3984H output ensures stability. The LP3984H still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP3984H and returned to a clean analog ground.

Start-up Function Enable Function

The LP3984H features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP3984H have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in LP3984H. When the operation junction temperature exceeds 150°C , the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 20°C . For continue operation, do not exceed absolute maximum operation junction temperature 125°C .

The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3984H, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-5 package is 195°C/W .

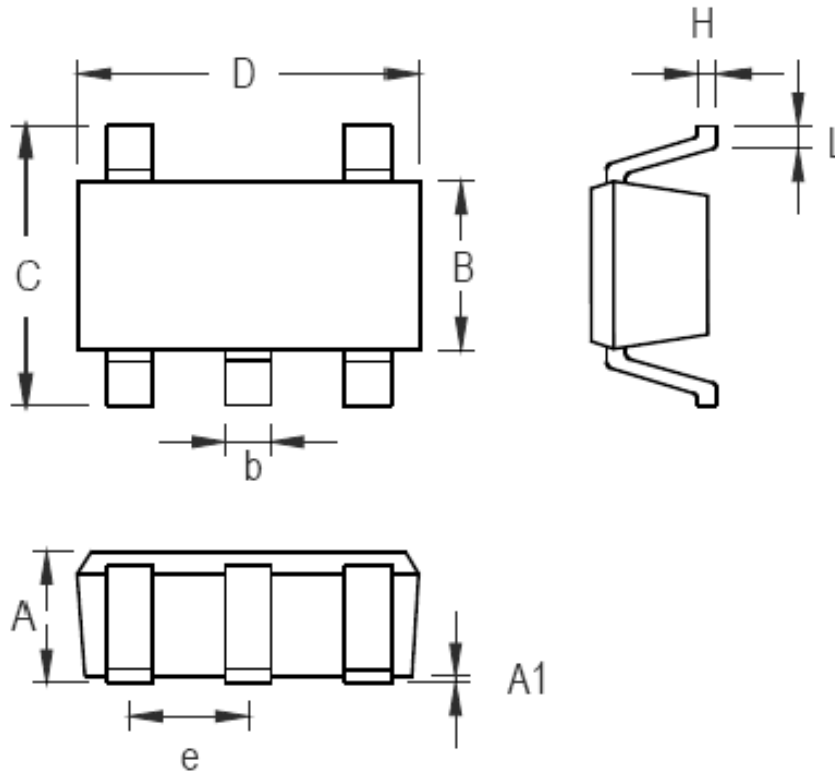
$$P_{D(MAX)} = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / 195 = 500\text{mW}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} .



Packaging Information

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package