INTEGRATED CIRCUITS
UNITRODE

Isolated Drive Transmitter

UC1726
UC2726
UC3726

FEATURES

- 750mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Drive Logic and Power through Low Cost Transformer
- Programmable Operating Frequency
- Up to 750kHz Operation
- Improved Output Control Algorithm Minimizes Output Jitter
- Fault Logic Monitors Isolated High Side IGBT Driver UC1727 for Faults
- User Programmable Fault Timing Screens False Fault Signals
- Shutdown Mode Disables On Chip Logic Reference for Low Standby Power
- Optional External Biasing of Logic Circuitry can Reduce Overall Power Dissipation

DESCRIPTION

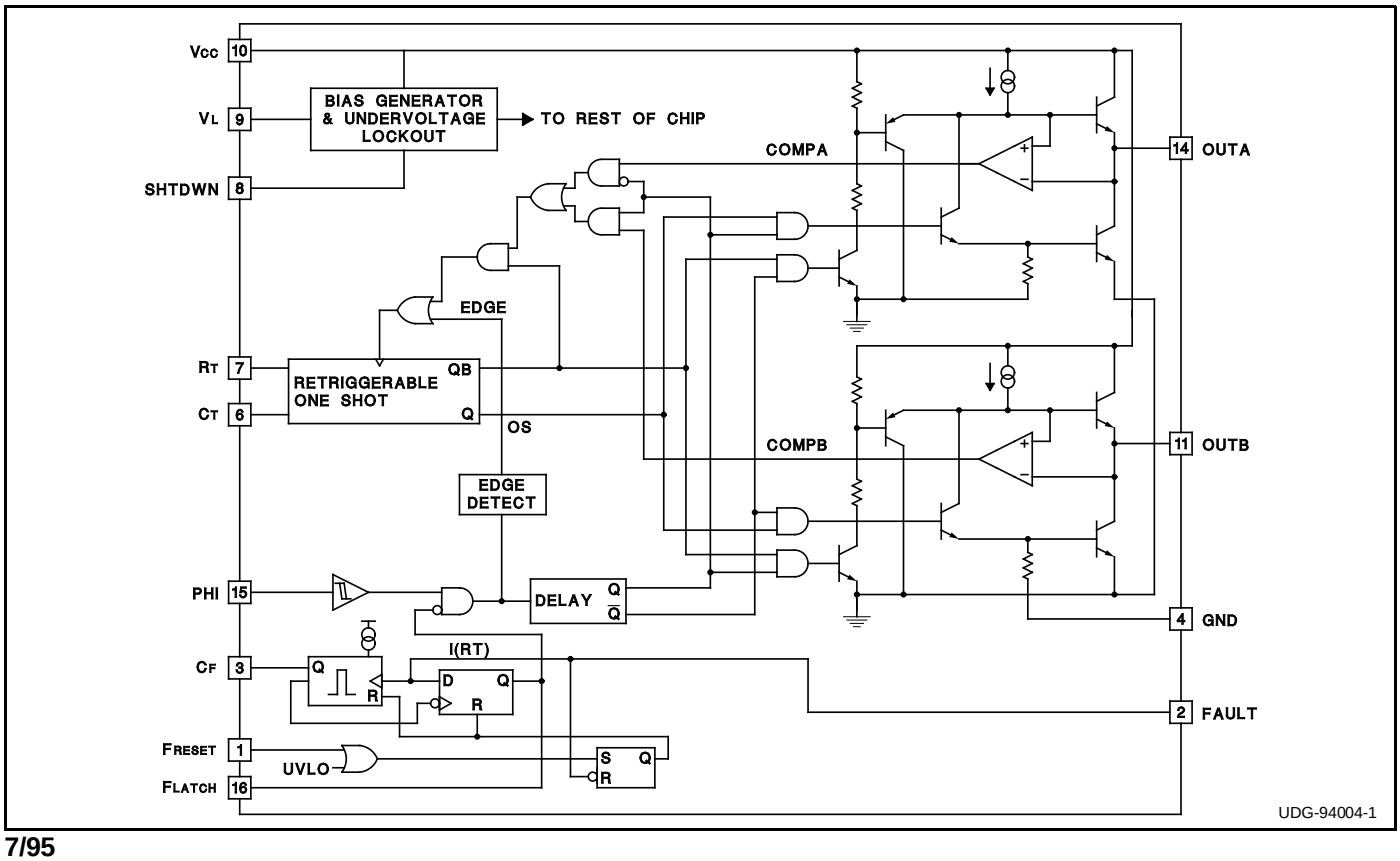
The UC1726 Isolated Drive Transmitter, and its companion chip, the UC1727 Isolated High Side IGBT Driver, provide a unique solution to driving isolated power IGBTs. They are particularly suited to drive the high side devices on a high voltage H-bridge. The UC1726 device transmits the drive logic and drive power, along with transferring and receiving fault information with the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty cycle modulation technique that gives instantaneous response to the drive control transitions, and reliably passes steady state, or DC conditions. High frequency operation, up to 750kHz, allows the cost and size of the coupling transformer to be minimized.

The UC1726 can be powered from a single V_{CC} supply which internally generates a voltage reference for the logic circuitry. It can also be placed into a low power shutdown mode that disables the internal reference. The IC's logic circuitry can be powered from an external supply, V_L, to minimize overall power dissipation. Fault logic monitors the Isolated High Side IGBT Driver UC1727 for faults. Based on user defined timing, the UC1726 distinguishes valid faults, which it responds to by setting the fault latch pin. This also disables the gate drive information until the fault reset pin is toggled to a logic one.

The UC1726 operates over an 8 to 35 volt supply range. The typical V_{CC} voltage will be greater than 28 volts to be compatible with the UC1727. The undervoltage lockout circuitry of the Isolated High Side IGBT Driver UC1727 locks out the drive information during its undervoltage lockout.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 40V
Source/Sink Current (Pulsed). 1.5A
Source/Sink Current (Continuous) 1.0A
Output Voltage (pins 12, 14). . . . . –0.3 to (V_{CC} + 0.3)V
C_F, FRESET, FAULT, SHTDWN,
FLATCH, V_L, PHI, R_T . . . . . –0.3 to 6.0V
C_T . . . . . 1.0 to 6.0V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 seconds). . . . . 300°C

Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.

RECOMMENDED OPERATING CONDITIONS (Note 3)

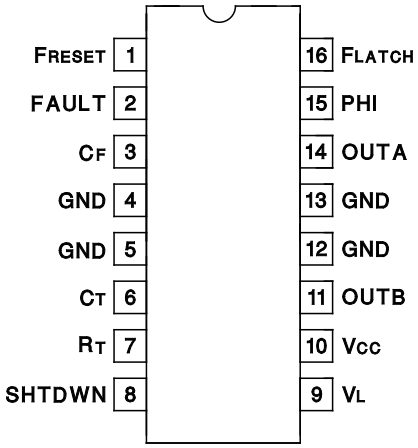
Input Voltage. . . . . +9 to +35.0V
Sink/Source Current (each output). . . . . 0 to 750mA
Timing Resistor. . . . . 2.4k to 200kΩ
Timing Capacitor (C_T). . . . . 75pF to 2.0nF
Timing Capacitor (C_F). . . . . 75pF to 3.0nF

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

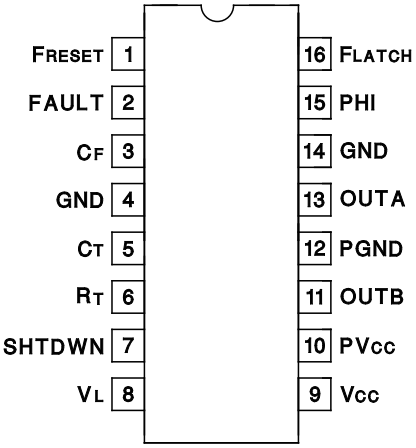
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

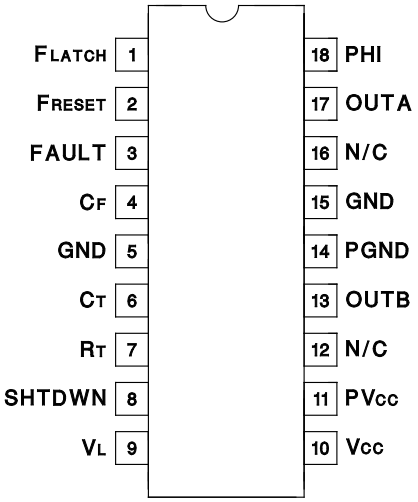
DIL-16 (Top View)
N Package



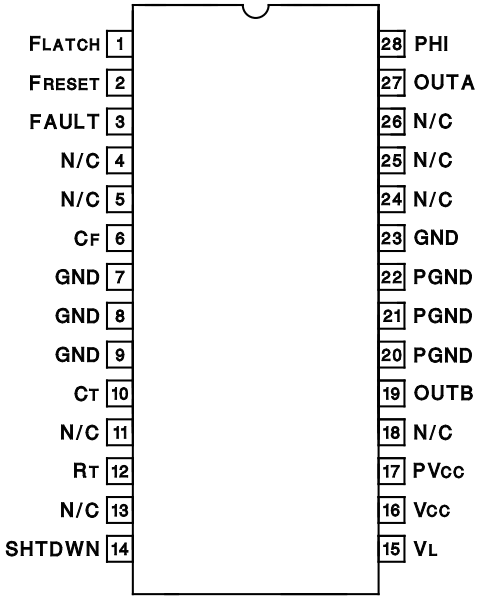
DIL-16 (Top View)
SP Package



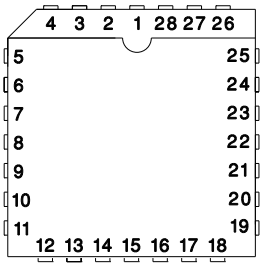
DIL-18 (Top View)
J Package



SOIC-28 (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
GND	1
C_T	2
N/C	3-4
R_T	5
SHTDWN	6
V_L	7
V_{CC}	8
N/C	9
PV_{CC}	10
OUTB	11
PGND	12-18
GND	19
OUTA	20
PHI	21
FLATCH	22
FRESET	23
FAULT	24
N/C	25
C_F	26
N/C	27
N/C	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 20V, R_T = 4.32kΩ, C_T = 330pF and C_F = 2.2nF, no load on any output, and –55°C < T_A < 125°C for the UC1726, –40°C < T_A < 85°C for the UC2726, and 0°C < T_A < 70°C for the UC3726, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Retriggerable one shot					
Initial Accuracy	T_J = 25°C	1.400	1.600	1.800	µsec
Temperature Stability	Over operating T_J	1.000		2.200	µsec
Voltage Stability	V_{CC} = 10 to 35V		0.2		%/V
Operating Frequency	L_{LOAD} = 1.5mH		170		kHz
PHI Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current			10		µA
LOW Input Current			-300	–600	µA
Delay to one shot			100	250	nsec
Delay to Output	C_T = 1.4V		250		nsec
Output Drivers					
Output Low Level	I_{SINK} = 20mA		0.3	0.5	V
	I_{SINK} = 400mA		0.5	2.6	V
Output High Level	I_{SOURCE} = –20mA		2.0	2.6	V
(volts below V_{CC})	I_{SOURCE} = –400mA		2.0	2.9	V
Rise and Fall Times	No load		30	60	nsec
Logic Voltage Reference					
V_L - Logic Voltage	Internal Voltage	4.20	4.40	4.60	V
Logic Supply Current	V_L = 4.75V to 5.25V, C_T = 1.4V		13.0	20.0	mA
Shut Down Circuit					
Logic Voltage - Off			0.5		V
High Input Current	V_{IH} = 2.4			-100	µA
Low Input Current	V_{IL} = 0.4			-20	µA
Fault Logic					
Fault Reset High Input Current	V_{IH} = 2.4			±5	µA
Fault Reset Low Input Current	V_{IL} = 0.4			-10	µA
Fault High Input Current	V_{IH} = 2.4			±5	µA
Fault Low Input Current	V_{IL} = 0.4			-60	µA
Fault Pulse Width	C_F = 330pF		3.0		µs
	C_F = 2.2nF		17.0		µs
Fault Latch, V_{OH}	I_{LOAD} = –1mA, Volts below V_L		1.3	1.8	V
Fault Latch, V_{OL}	I_{LOAD} = 1mA		0.25	0.5	V
Fault Latch, V_{OH}	I_{LOAD} = 0, Volts below V_L		0.3		V
Fault Latch, V_{OL}	I_{LOAD} = 0		0.2		V
Fault Reset Pulse Width			500		ns
UVLO					
Turn On Threshold			7.1		V
Total Supply Current					
Supply Current	C_T = 1.4V		22	40	mA
	C_T = 1.4V, V_L = 5.0V		12	20	mA
	C_T = 1.4V, Shutdown = 5.0V		2.5		mA

Refer to Typical Application on Page 5 and Application Note U-143A "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

C_F: The timing input to the fault logic. A capacitor is placed across the input of C_F and ground. The timing window is approximately $t = 2.1C_FR_T$.

C_T: The connection to the timing capacitor that controls the operating frequency. A capacitor to ground is repetitively charged during the one shot pulse width. It is discharged when a comparator senses zero current in the primary side of the transformer. The one shot pulse width is consequently determined by the time it takes to charge the capacitor from a threshold voltage of $V_L/4$ to $V_L/2$. This pin must be tied to a capacitor. See Recommended Operating Conditions.

FAULT: This input to the fault logic initiates the user programmable timer. This time interval, specified by the capacitor on C_F, determines the validity of the fault. The pin is tied to a low cost optocoupler, and is high until the UC1727 sends drive information from the PHI pin through the transformer while the FAULT pin stays low. Once this pin goes high, it must stay high during the entire fault window to be accepted as a valid fault. A valid fault sets the F_{LATCH} pin high and prevents the transmitting of gate drive information until the F_{RESET} is toggled high. If fault logic is not used, the FAULT pin must be grounded.

F_{LATCH}: A valid fault sets this pin to a logic one and prevents the transmitting of gate drive information. The F_{LATCH} pin can only be reset by connecting the F_{RESET} to a logic 0.

F_{RESET}: The input to the fault logic that resets the fault logic latch (F_{LATCH}) and enables drive transmit data. This input must be low when powered up and stay low until after the fault latch has been set.

GND: The signal and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground which biases the remainder of the device.

OUTA: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between 0.3V during the one shot charge time and approximately V_{CC} + 0.4V during the remainder of the period. When PHI is low the output toggles between V_{CC} - 2V during the one shot charge time and approximately $0.6V_{CC}$ during the remainder of the period.

OUTB: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between V_{CC} - 2V during the one shot charge time and approximately $0.6V_{CC}$ during the remainder of the period. When PHI is low the output toggles between 0.3V during the one shot charge time and approximately V_{CC} + 0.4V during the remainder of the period.

PGND: This is the ground for the output transistors bonded in the 28 pin packages. On the sixteen pin packages it is bonded separately to the GND pin.

PHI: A logic control input to the isolated gate drive that changes the outputs as described above. This changes the duty cycle of the voltage wave form applied across the transformer. The Isolated High Side IGBT Driver UC1727 senses the different duty cycles as different drive commands.

PV_{CC}: This is the input voltage for the output transistors on the 28 pin package. On the sixteen pin packages it is bonded separately to the V_{CC} pin.

R_T: The input that sets the C_T and C_F capacitor currents with a resistor to ground. The voltage on R_T is approximately $0.3V_L$. The resulting charge currents are: $IC_T = IC_F = V_L / 4R_T$.

SHTDWN: This input shuts down the internal reference. A TTL logic one puts the UC1726 into a low standby current mode. This input has a pull down resistor on the chip to guarantee proper operation when left open. If an external logic voltage is applied to V_L, this shutdown feature cannot be used without bringing the external voltage source to zero volts.

V_{CC}: The input voltage that biases the outputs and the internal reference. It can vary between 8V to 35V. This supply pin will typically be greater than 28V to be compatible with the UC1727. In order to minimize power dissipation use an external logic supply, V_{CC} approximately 15V, and a step up transformer (N = 2).

V_L: The logic supply pin that biases all circuits except for the totem pole outputs. A bypass capacitor is recommended on this pin when left unconnected. The internal reference is approximately 4.4V. A 5.0V supply can be applied to this pin to assure minimum power dissipation. When an external supply higher than the V_L voltage is applied to this pin, the internal reference turns off.

OPERATING FREQUENCY:

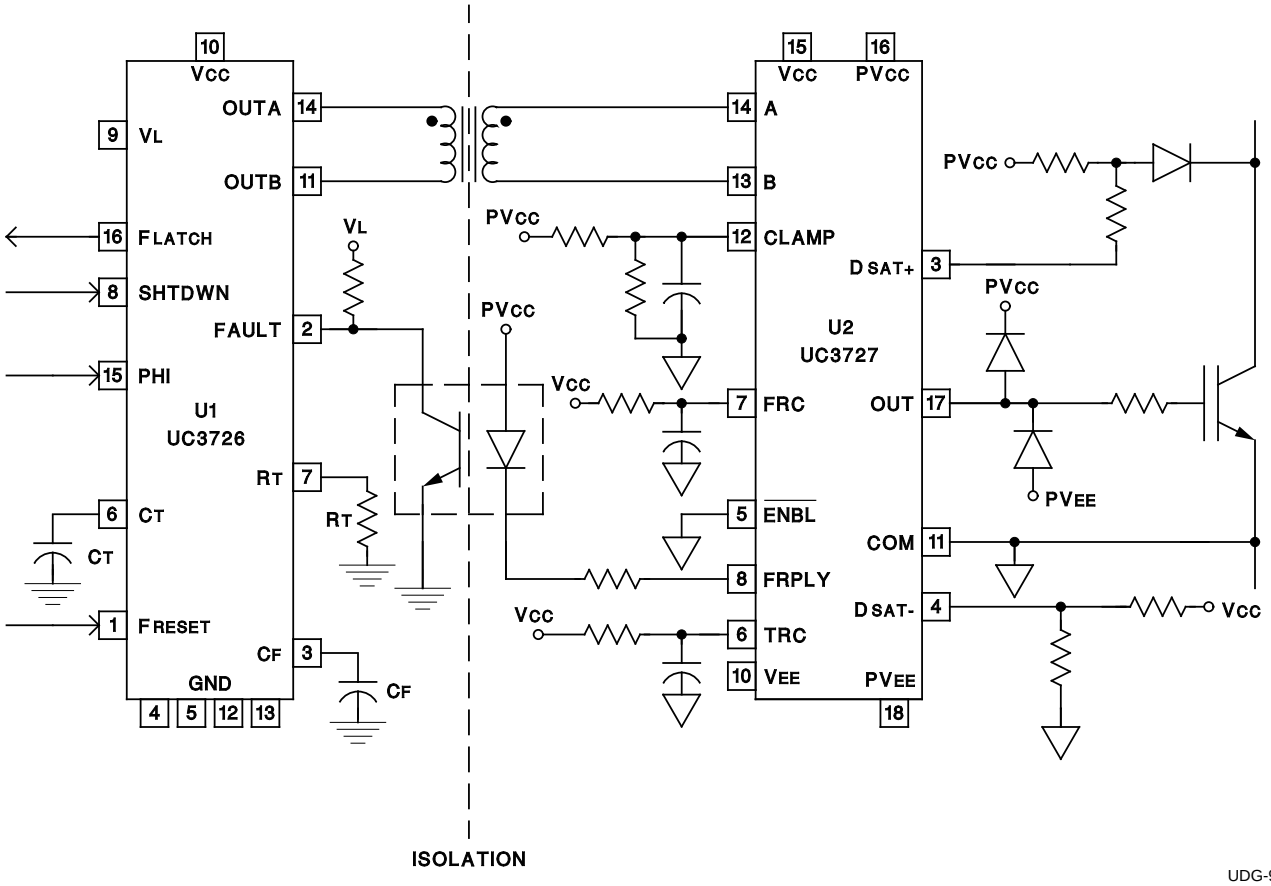
The chip operating frequency is determined by the values of components connected to the R_T and C_T pins. A resistor connected between R_T and ground sets the charge current to $IC_T = V_L / 4R_T$. The operating frequency varies slightly depending on the V_{CC} and V_L voltages. The following equations approximate the one shot pulse width at operating frequency when V_{CC} = 20V.

$$T_{PW} = 1.1R_T(C_T + 50pF)$$

$$F_O = \frac{1}{3.3R_T(C_T + 50pF)}$$

The 50pF additional capacity represents internal chip capacitance at the C_T input.

TYPICAL APPLICATION



IF FAULT LOGIC NOT USED, GROUND FAULT PIN.

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UC2726DWP	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
UC2726DWPTR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI
UC2726N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
UC3726DWP	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3726DWPTR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3726N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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