

# **N588Hxxx**

## **Data Sheet**

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## 1. General Description

The N588Hxxx is an advanced 3-ch Voice/Melody IC that combines with the technology of 8-bit 65C02 core and new 4-bit or 5-bit MDPCM synthesizer to implement sophisticated applications in high level of sound quality.

The N588Hxxx improves the structure to minimize the external components for various applications. In addition, it allows customers to use internal Rosc with precise frequency control to save BOM cost and gain lower frequency deviation.

Furthermore, the N588Hxxx provides lots of function includes 16 ~ 24 I/Os where one port with high drive current, 128 ~ 192 Bytes RAM, H/W IR carrier, 2-ch Comparator and Low Voltage Detection. Meanwhile, N588Hxxx builds in 3-pair output pins with 64-level control for the applications of motors tiny control. The N588Hxxx also build in Watch Dog Timer and Low Voltage Reset to prevent latch-up situation occurring.

The N588Hxxx family contains several items with different playback ROM size and duration as shown below table:

| N588Hxxx        | H061 | H081 | H120 | H170 | H200 | *H201 | H250 | *H251 | H340 | *H341 | H480 | H650 |
|-----------------|------|------|------|------|------|-------|------|-------|------|-------|------|------|
| ROM (KB)        | 206  | 254  | 414  | 510  | 704  | 704   | 830  | 830   | 1020 | 1020  | 1534 | 2044 |
| Sec. @NM4, 6KHz | 65   | 80   | 131  | 162  | 223  | 223   | 263  | 263   | 324  | 324   | 486  | 648  |
| I/O             | 16   | 16   | 16   | 16   | 24   | 24    | 24   | 24    | 24   | 24    | 24   | 24   |

\*N588H201, N588H251, N588H341 no support LVD

## 2. Features

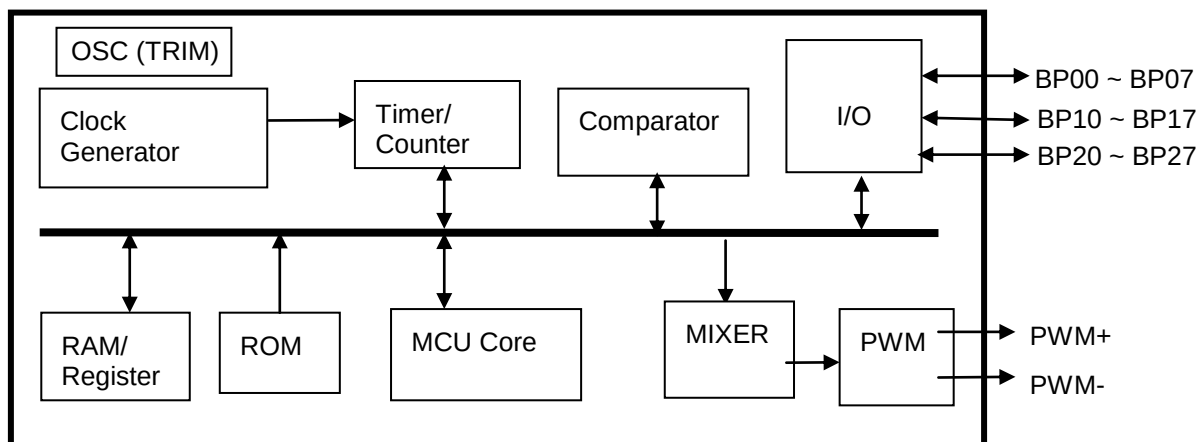
- VDD range:
  - 4MHz/6MHz: 2.2 ~ 5.5V
  - 8MHz: 2.6 ~ 5.5V
- System clock: 4, 6, 8 MHz
- Oscillator: builds in internal Rosc (TRIM)
- RAM: 128B ~ 192B
- 16 ~ 24 bi-directional I/O pins
  - BP00 ~ BP07, BP10 ~ BP17 can be set as Input or Output status individually
- Provides 8-pin with high sink current capability to drive LEDs
- 3-pair H/W PWM I/O pins with 6-bit resolutions to control motor
  - BP00/02/04 are defined as 3 H/W PWM I/O pins. They can be paired with BP01/03/05 respectively by same (or opposite) phase of output waveform
- Builds in IR carrier generation circuit for simplifying firmware IR application
- Algorithm: 4-bit NM4, 4-bit NM4S, 5-bit MDM
- Audio output: 12-bit PWM
- Channel: 3-channel Voice or Melody
  - 3-ch Voice
  - 3-ch Melody
  - 1-ch Voice + Dual tone melody
- Built-in Watch-Dog Timer (WDT)
- 3 voltage levels of Low Voltage Reset (LVR) by mask option
  - LVR: 2.0V, 2.2V, 2.7V
- Builds in Low Voltage Detection (LVD) with 4 voltage levels
  - LVD: 2.2V, 2.4V, 2.7V, 3.3V (N588H201, N588H251, N588H341 no support LVD)
- Built-in 2-channel comparator
- Support **PowerScript™** for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger (Assembly & **PowerScript™** format)
  - **Ultra I/O™** tool for event synchronization mechanism
- Available package form:
  - COB is essential

### 3. Pin Description

| Pin Name     | I/O   | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| /RESET       | I     | IC reset input, low active.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| BP00 ~ BP07  | I/O   | <ul style="list-style-type: none"> <li>● General input/output pins.</li> <li>● Each pin can be set as Input or Output individually.</li> <li>● When the pin will be set output by BP0D, user needs to set BP0x value of 0/1 first.</li> <li>● For output pin, BP0 provides high-sink current.</li> <li>● For input pin, it can be set as pull-high or floating</li> <li>● BP00/02/04 can be set as 3-pin H/W PWM output with 64-level resolution. They can be paired with BP01/03/05 (also H/W PWM output) respectively with same or opposite phase of output waveform</li> <li>● BP07 can be configured as IR carrier output</li> </ul> |
| BP10 ~ BP17  | I/O   | <ul style="list-style-type: none"> <li>● General input/output pins.</li> <li>● Each pin can be set as Input or Output individually.</li> <li>● When the pin will be set output by BP1D, user needs to set BP1x value of 0/1 first.</li> <li>● For input pin, it can be set as pull-high or floating.</li> <li>● BP1 can generate interrupt request to release IC from STOP mode</li> </ul>                                                                                                                                                                                                                                               |
| *BP20 ~ BP27 | I/O   | <ul style="list-style-type: none"> <li>● General input/output pins.</li> <li>● Each pin can be set as Input or Output by group, BP20 ~ BP23 configured by BP2D[0], and BP24 ~ BP27 by BP2D[1].</li> <li>● When the pin will be set output by BP2D, user needs to set BP2x value of 0/1 first.</li> </ul>                                                                                                                                                                                                                                                                                                                                 |
| PWM+         | O     | PWM driver positive output to drive speaker directly                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| PWM-         | O     | PWM driver negative output to drive speaker directly                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDD          | Power | Positive power supply for uP and peripherals                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VSS          | Power | Negative power supply for oscillation, uP and peripherals                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| VDD_IO       | Power | Positive power supply for I/O                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| VSS_IO       | Power | Negative power supply for I/O                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| VDD_SPK      | Power | Positive power supply for speaker driver                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| VSS_SPK      | Power | Negative power supply for speaker driver                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

Note: BP20 ~ BP27 only provides in N588H200/201, N588H250/251, N588H340/341, N588H480 and N588H650

## 4. Block Diagram



## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

| Parameter       | Symbol  | Conditions | Rated Value          | Unit |
|-----------------|---------|------------|----------------------|------|
| Power Supply    | VDD–VSS | -          | -0.3 to +7.0         | V    |
| Input Voltage   | VIN     | All Inputs | VSS -0.3 to VDD +0.3 | V    |
| Storage Temp.   | TSTG    | -          | -55 to +150          | °C   |
| Operating Temp. | TOPR    | -          | 0 to +70             | °C   |

Note: Exposure to conditions beyond those listed under the Absolute Maximum Ratings table may adversely affect the life and reliability of the device.

### 5.2 D.C. Characteristics

(VDD – VSS = 4.5V, TA = 25° C, No Load unless otherwise specified)

| Parameter         | Sym              | Conditions                                               | Min | Typ | Max | Unit |
|-------------------|------------------|----------------------------------------------------------|-----|-----|-----|------|
| Operating Voltage | V <sub>DD</sub>  | F <sub>OSC</sub> = 4 MHz                                 | 2.2 | -   | 5.5 | V    |
|                   |                  | F <sub>OSC</sub> = 6 MHz                                 | 2.2 | -   | 5.5 | V    |
|                   |                  | F <sub>OSC</sub> = 8 MHz                                 | 2.6 |     | 5.5 | V    |
| Operating Current | I <sub>OP1</sub> | No load, F <sub>OSC</sub> = 6 MHz<br>N588H061 ~ N588H341 | -   | 5   | 7   | mA   |
|                   |                  | No load, F <sub>OSC</sub> = 6 MHz                        | -   | 7.5 | 9.5 | mA   |

|                                    |                  |                                                                                          |                     |                          |                      |    |
|------------------------------------|------------------|------------------------------------------------------------------------------------------|---------------------|--------------------------|----------------------|----|
|                                    |                  | N588H480, N588H650                                                                       |                     |                          |                      |    |
| Standby Current (STOP)             | I <sub>DD1</sub> | No load                                                                                  | -                   | 1                        | 2                    | μA |
| Input Low Voltage                  | V <sub>IL</sub>  | All input pins                                                                           | V <sub>SS</sub>     | -                        | 0.3 V <sub>DD</sub>  | V  |
| Input High Voltage                 | V <sub>IH</sub>  | All input pins                                                                           | 0.7 V <sub>DD</sub> | -                        | V <sub>DD</sub>      | V  |
| Input Current BP0, BP1, BP2        | IIN1             | VIN = 0V, pulled-high resistor = 500KΩ                                                   | -5                  | -9                       | -14                  | μA |
| Input Current BP0,BP1, BP2         | IIN2             | VIN = 0V, pulled-high resistor = 150KΩ                                                   | -15                 | -30                      | -45                  | μA |
| Output Current (BP0)               | I <sub>OL</sub>  | V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 0.4V                                            | 8                   | 12                       | -                    | mA |
|                                    | I <sub>OH</sub>  | V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 2.6V                                            | -4                  | -6                       | -                    | mA |
|                                    | I <sub>OL</sub>  | V <sub>DD</sub> = 4.5V, V <sub>OUT</sub> = 1.0V                                          | -                   | 25                       | -                    | mA |
|                                    | I <sub>OH</sub>  | V <sub>DD</sub> = 4.5V, V <sub>OUT</sub> = 3.5V                                          | -                   | -12                      | -                    | mA |
| Output Current (BP1, BP2)          | I <sub>OL</sub>  | V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 0.4V                                            | 4                   | 5                        | -                    | mA |
|                                    | I <sub>OH</sub>  | V <sub>DD</sub> = 3V, V <sub>OUT</sub> = 2.6V                                            | -4                  | -6                       | -                    | mA |
|                                    | I <sub>OL</sub>  | V <sub>DD</sub> = 4.5V, V <sub>OUT</sub> = 1.0V                                          | -                   | 12                       | -                    | mA |
|                                    | I <sub>OH</sub>  | V <sub>DD</sub> = 4.5V, V <sub>OUT</sub> = 3.5V                                          | -                   | -12                      | -                    | mA |
| Output Current PWM+ / PWM-         | I <sub>OL1</sub> | RL= 8Ω                                                                                   | +250                | -                        | -                    | mA |
|                                    | I <sub>OH1</sub> | [PWM+]---[RL]----[PWM-]<br>]                                                             | -250                | -                        | -                    | mA |
| Comparator input common mode range | V <sub>CM</sub>  | V <sub>DD</sub> =2.2 ~ 5.5V                                                              | 0.1                 |                          | V <sub>DD</sub> -1.5 | V  |
| Comparator input offset voltage    | V <sub>OS</sub>  | External (V <sub>cm</sub> =2.5V)                                                         |                     | 50                       | -                    | mV |
| *LVD detect voltage                | V <sub>LVD</sub> | CTL_CPU [5,3] = 0_1<br>CTL_CPU [5,3] = 1_1<br>CTL_CPU [5,3] = 0_0<br>CTL_CPU [5,3] = 1_0 | -                   | 2.2<br>2.4<br>2.7<br>3.3 | -                    | V  |

Note\*: N588H201, N588H251, N588H341 no support LVD

### 5.3 A.C. Characteristics

(V<sub>DD</sub> = 4.5V, T<sub>A</sub> = 25°C, No Load unless otherwise specified)

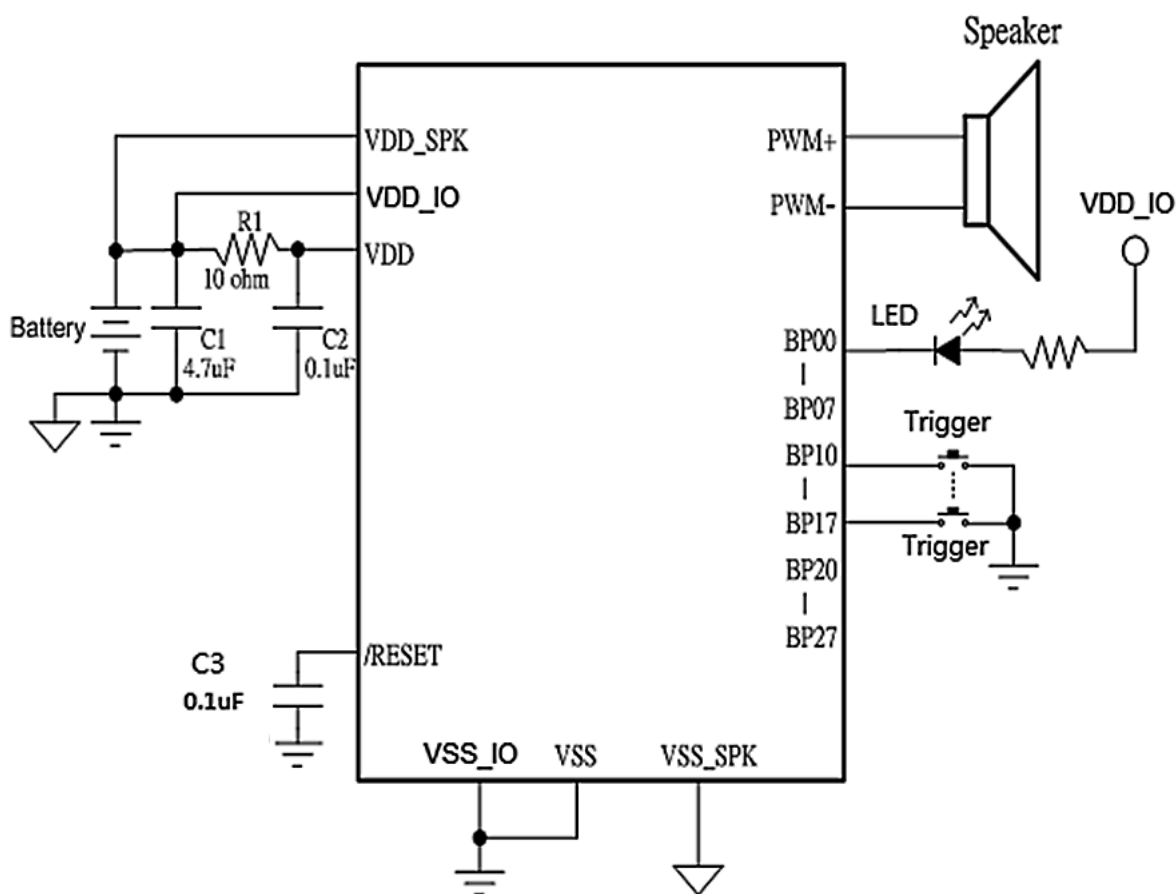
| Parameter            | Sym | Conditions               | Min  | Typ  | Max  | Unit |
|----------------------|-----|--------------------------|------|------|------|------|
| Main Clock Frequency | FM  | F <sub>OSC</sub> = 4 MHz | 3973 | 4096 | 4219 | KHz  |
|                      |     | F <sub>OSC</sub> = 6 MHz | 5960 | 6144 | 6328 |      |
|                      |     | F <sub>OSC</sub> = 8 MHz | 7946 | 8192 | 8438 |      |

Release Date: Jun. 2016

Version A15.0

|                                        |         |                                                   |   |   |   |   |
|----------------------------------------|---------|---------------------------------------------------|---|---|---|---|
| Frequency Deviation<br>by Voltage Drop | F/<br>F | $(F_{max} - F_{min})/F_{min}$<br>@VDD: 2.4 ~ 4.5V | - | 2 | - | % |
|----------------------------------------|---------|---------------------------------------------------|---|---|---|---|

## 6. Application Circuit



Note:

- C1 (4.7uF), C2 (0.1uF), R1 (10Ω) are required for power stability
- C1 value need to be adjusted according to the loading, such as motor control application.
- C3 (0.1uF) is required to stabilize reset signal

## 7. Revision History

| Version | Date      | Substantial Changes                                          | Page |
|---------|-----------|--------------------------------------------------------------|------|
| A1.0    | Jan. 2012 | Initial release.                                             | All  |
| A2.0    | Feb. 2012 | Revise N588H060 ROM size                                     | 2    |
|         |           | Revise Working Voltage                                       | 3    |
|         |           | Revise AC characteristic table                               | 6    |
| A2.1    | Mar. 2012 | Revise BP0, BP2 input description                            | 4    |
|         |           | Revise BP1, BP2 output current                               | 5    |
|         |           | Revise frequency deviation (by voltage drop)                 | 6    |
| A2.2    | May 2012  | Revise VDD range in 8MHz and 6MHz                            | 3, 5 |
|         |           | ADD LVR value                                                | 3    |
|         |           | Add output current of BP1, BP2 at VDD 4.5V                   | 5    |
|         |           | Add comparator and LVD spec                                  | 5, 6 |
|         |           | Revise AP circuit 0.1uF as 4.7uF                             | 6    |
| A2.3    | Jun. 2012 | Revise duration                                              | 2    |
| A3.0    | Oct. 2012 | Remove the word of "preliminary"                             |      |
|         |           | Rename part number of N588H060, H080 as N588H061, H081       |      |
| A4.0    | Dec. 2012 | Resume N588H060, N588H080                                    | 2    |
|         |           | Add availability note of N588H061, N588H081                  | 2    |
| A5.0    | Dec. 2012 | Revise ROM size on N588H060, N588H120, N588H250              | 2    |
| A6.0    | Sep. 2013 | Remove N588H060, N588H080                                    | 2    |
|         |           | Revise application circuit in                                | 7, 8 |
| A7.0    | Feb. 2014 | Modify the description of 3-pair H/W PWM I/O                 |      |
| A8.0    | Mar. 2014 | Revise AP circuit: C1 4.7uF change as 0.1uF                  | 7    |
| A9.0    | Dec. 2014 | Add N588H200 part number                                     | 2    |
|         |           | Revise duration                                              | 2    |
|         |           | Revise LVD level on page                                     | 3, 6 |
|         |           | Update application circuits                                  | 7, 8 |
| A10.0   | Mar. 2015 | Revise VDD range and LVD level                               | 3, 6 |
| A11.0   | Sep. 2015 | Add item of N588H201, N588H251, N588H341, N588H480, N588H650 | 2    |
| A12.0   | Nov. 2015 | Revise application circuit                                   | 7    |
| A13.0   | Dec. 2015 | Update pad name of VDD_IO and VSS_IO                         | 4, 7 |
| A14.1   | Feb. 2016 | Revise operation current in DC Characteristics               | 6    |
| A15.0   | Jun. 2016 | Modify note                                                  | 8    |

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