Programmable SMPS and USB Type-C Controller

General Description

The RT7205A is a highly integrated and programmable SMPS controller at the secondary side. It provides the necessary functions and protections for high efficient and high power density off-line AC-DC converter designs. The RT7205A integrates an MCU to handle various proprietary protocols (e.g., FCP, SCP and AFC) through D+/D- interface and also support USB Type-C via CC1/CC2 pins. An internal synchronous rectifier controller can optimize efficiency and provide safe operate in both continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) even in the condition of a wide output voltage range of 3V to 12V. Dual operational amplifiers with respectively programmable reference voltages are included for voltage-loop and current-loop regulation to provide programmable constant-voltage (CV) and constant-current (CC) regulation in high precision.

Ordering Information

RT7205A□□□-□

- □ (Programmed Firmware Code AABBX)
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- □ (Package Type)
  - QW : WQFN-24L 4x4 (W-Type) (Exposed Pad-Option 2)
- □ (Lead Plating System)
  - G : Green (Halogen Free and Pb Free)
- RT7205A Version (Refer to Version Table)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Protocols Supported**
  - **SCP, FCP, AFC and Proprietary Protocols**
  - **USB Type-C**
- **Highly Integrated**
  - **Embedded MCU with an Mask-ROM of 16kB, an OTP-ROM of 8kB, and an SRAM of 0.75kB**
  - **Built-in Synchronous Rectifier Driver and Controller**
  - **Built-in Charge Pump for a Wide V_{DD} Operation Range of 3V to 12V**
  - **Built-in Shunt Regulator for Programmable Constant-Voltage and Constant-Current Control**
  - **Programmable Cable Compensation**
  - **BLD Pin for Quick Discharge of Output Capacitor**
  - **USBP Pin for Direct Drive of External Blocking N-MOSFET**
  - **Power-Saving Mode in Standby Mode**
- **Protection**
  - **Adaptive Over-Voltage Protection**
  - **Adaptive Under-Voltage Protection**
  - **Firmware-Programmable Over-Current Protection**
  - **Firmware-Programmable Over-Temperature Protection**

Applications

- Travel Adaptors with Fast Charge Protocols (e.g., FCP, SCP and AFC)
- Travel Adaptors with USB Type-C Control (e.g., 5V/1.5A and 5V/3A)

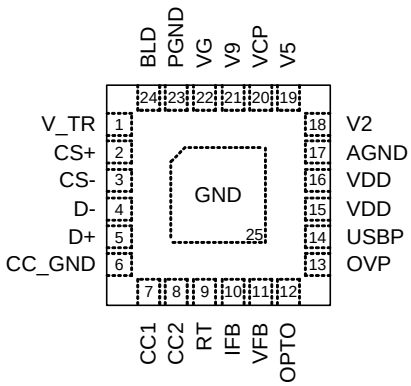
Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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Pin Configuration

(TOP VIEW)



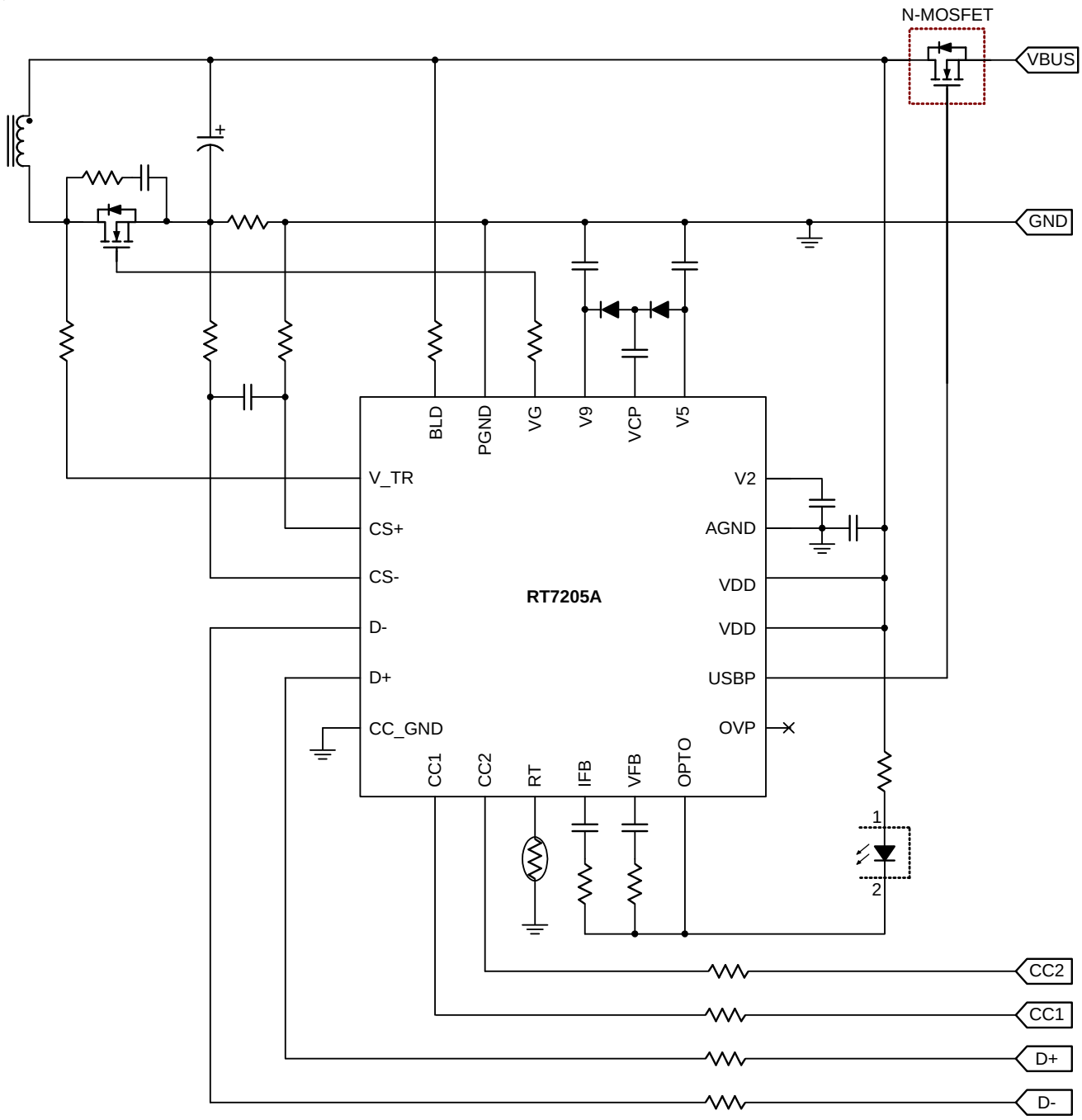
WQFN-24L 4x4

RT7205A Version Table

Version	RT7205A	RT7205AL
Maximum Output Voltage	12V	5V
V_{DS} SCALE R_{VDS2} / (R_{VDS1} + R_{VDS2})	1/26	1/13
V_{OUT} SCALE R_{FB2} / (R_{FB1} + R_{FB2})	1/5	1/2.5
Built-in FB Resistors	O	O
Blocking MOSFET Driver	N-MOSFET	N-MOSFET

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Simplified Application Circuit



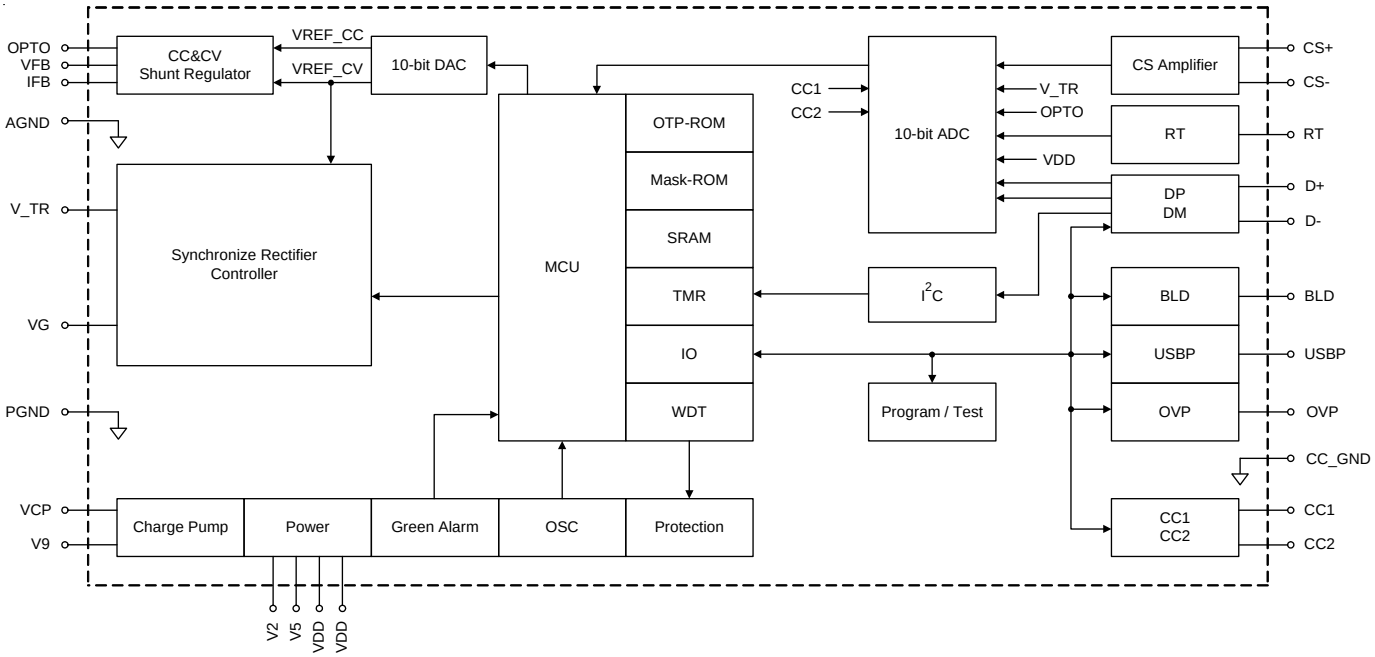
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Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	V_TR	AI	Transformer voltage sense node.
2	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
3	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
4	D-	A/D IO	USB D- channel.
5	D+	A/D IO	USB D+ channel.
6	CC_GND	GND	Alternative ground for CC1 and CC2.
7	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
8	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
9	RT	A/D I	Remote thermal sensor connection node for over-temperature protection.
10	IFB	AI	Feedback input for the constant-current loop.
11	VFB	AI	Feedback input for the constant-voltage loop.
12	OPTO	AO	Current sink output for optocoupler connection.
13	OVP	AO	Over-voltage fault indication output, used to pull low an optocoupler.
14	USBP	D IO	Control signal of the blocking N-MOSFET
15	VDD	PWR	Supply input voltage.
16	VDD	PWR	Supply input voltage.
17	AGND	GND	Analog ground.
18	V2	PWR	Regulated DC bias to supply for the MCU.
19	V5	PWR	Regulated DC bias to supply for internal circuitry.
20	VCP	AO	Charge pump driver output.
21	V9	PWR	Regulated DC bias to supply for the synchronous rectifier driver.
22	VG	AO	Gate driver output for the SR MOSFET.
23	PGND	GND	Power ground.
24	BLD	D IO	Bleeder connection node to provide another path to discharge the output capacitor.
25 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

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Functional Block Diagram



Operation

The RT7205A is a highly integrated secondary-side programmable SMPS and USB Type-C controller with various functions and protections for off-line AC-DC converters.

Power Structure

Biased by the VDD pin, the RT7205A has two regulated DC output voltages, V_5 and V_2, to supply the internal circuit and the internal microprocessor (MCU). The bypass capacitors at the V2 and V5 pins are required to improve stability of the internal LDO and to minimize regulated ripple voltages. The RT7205A also integrates a charge pump to generate a boost voltage V_9 from V_5 with VCP pin for capacitor connection so that the V9 voltage can be nearly 2 times of the V5 voltage and the VG pin can directly drive the SR MOSFET. Besides, the charge pump allows the controller to operate under low supply voltage condition as long as the output voltage is not below the programmed UVP level.

Constant-Voltage and Constant-Current (CV/CC) Regulators

Two regulators are paralleled and connected to an open-drain output, OPTO pin. The operation of each feedback loop is similar to that of the traditional TL431 shunt regulator except that V_{OPTO} operating range is wider, from 0.3V to 16.5V, which enables easy design of converters with a wider output range. The OPTO pin will be in high-impedance state, if the VDD voltage is still below a UVLO threshold V_{VDD_ON}, which ensures a smooth power-on sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, for the voltage and current feedback loops, respectively, are analog output voltages from the embedded DAC, and their digital counterparts are from the MCU. The analog output range of the 10-bit DAC is from 0 to V_{DAC_MAX} (typical 2.7V), which makes output voltage resolution as small as 13.2mV and 6.6mV for the RT7205A and RT7205AL, respectively, to achieve high-precision CV regulation.

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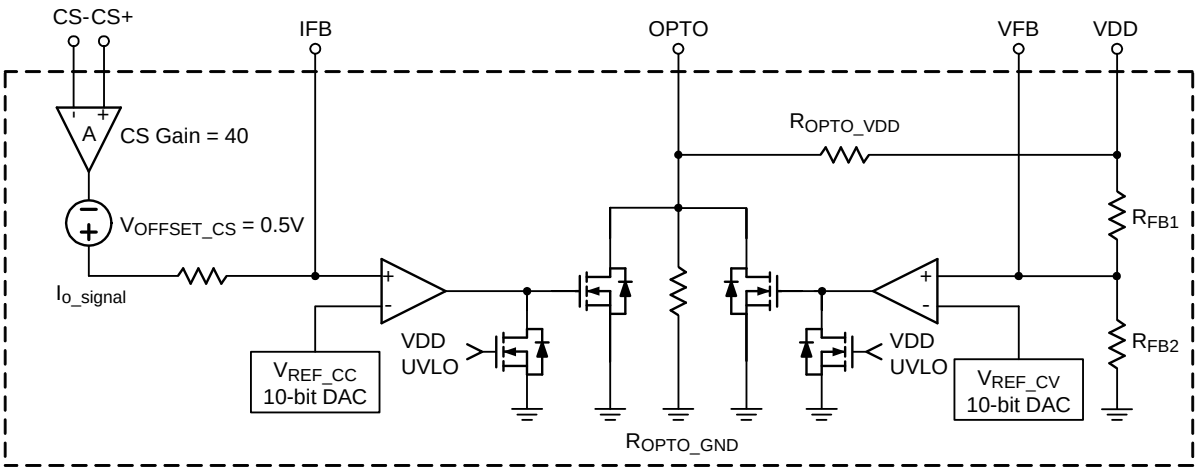


Figure 1. CV and CC Loops

Current-Sense Amplifier

To minimize power loss of the current sense resistor in the converter, the RT7205A includes an amplifier with virtually zero input offset voltage and with a voltage gain of 40. The sensed output current is amplified by the current-sense amplifier, shown as "Io_signal" in Figure 1, which is then sent to the current-loop regulator for constant-current regulation and also sent to the MCU, by way of an 10-bit ADC for analog-to-digital conversion, to update the output current status for the MCU.

External Temperature Sensing

The RT7205A provides the RT pin, as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC), as shown in Figure 2. If the RT voltage is below an over-temperature protection (OTP) threshold and the condition sustains for a programmed time delay, the OTP will be triggered.

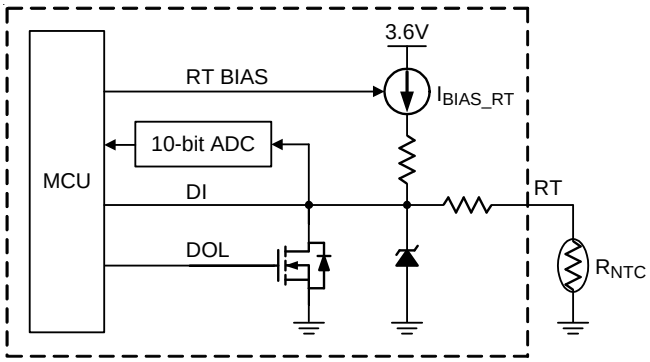


Figure 2. External Temperature Sensing

Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU via an ADC, can be reprogrammed for other purposes since they can be used as an analog/digital input or output.

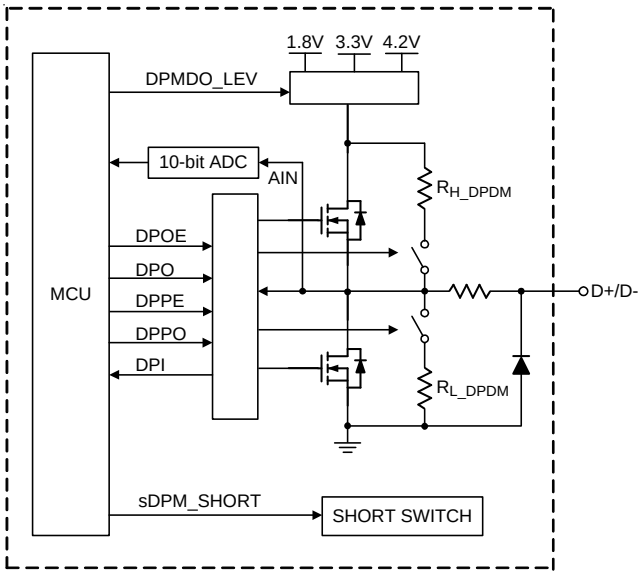


Figure 3. Interface of D+ and D-

Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with USB Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80µA, 180µA, and 330µA, provided by each of the CC pins, will

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be advertised to an Upstream Facing Port (UFP) as default USB current, 1.5A, and 3.0A, respectively.

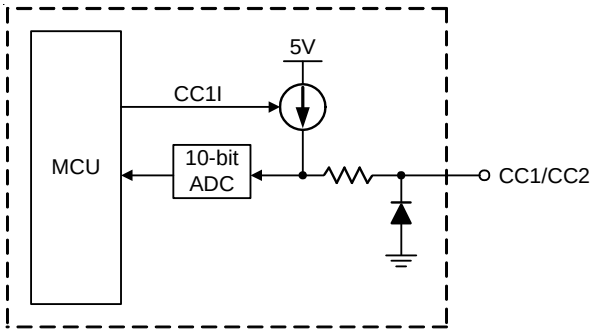


Figure 4. Interface of CC1 and CC2

Open-Drain Drivers for BLD and OVP Pins

The BLD and OVP pins with their specific functions are driven by open-drain drivers, as shown in Figure 5 and explained below.

The BLD pin is used as a bleeder to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 12V to 5V. A resistor is connected between V_{OUT} and the BLD pin and a power resistor can be used for better power dissipation capability.

The OVP pin is pulled low when output over-voltage condition (register-programmable : 115%, 120%, 125%) occurs. By way of an optocoupler, it can shut down the primary-side controller (for example, RT7752).

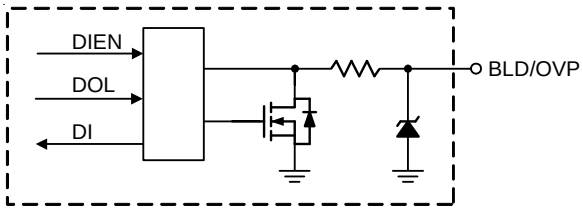


Figure 5. Interface of BLD and OVP Pins

SR Control

To improve the AC-DC converter's efficiency, the RT7205A includes a SR controller, which has proprietary auto-tracking function to minimize dead time between the conduction intervals of the SR MOSFET and the main switch MOSFET, while it can still ensure safe operation in both DCM and CCM conditions and even in a wide output range. To prevent the on-time overlap of the main switch MOSFET and the SR MOSFET, the SR controller will be temporarily turned off under conditions of load transition, output voltage transition, output short circuit, or low output or input voltages with programmable thresholds. At light load or no load condition, the SR controller will also be disabled to reduce power consumption.

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Absolute Maximum Ratings (Note 1)

- USBP to GND ---------- –0.3V to 25V
- VDD, OPTO, BLD, OVP to GND ---------- –0.3V to 16.5V
- V9, VG to GND ---------- –0.3V to 13V
- V5, VCP, VFB, IFB, V_TR, RT, CC1, CC2, D+, D-, CS+, CS- to GND ---------- –0.3V to 6.5V
- V2 to GND ---------- –0.3V to 2.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  WQFN-24L 4x4, θ_{JA} ---------- 28°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 7.1°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 3V to 13V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold Voltage	V_{VDD_ON}		2.9	3.0	3.1	V
VDD Turn-Off Threshold Voltage	V_{VDD_OFF}		2.55	2.7	2.85	V
VDD Turn-On/-Off Hysteresis	V_{VDD_HYS}		--	0.3	--	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.6V	--	200	300	µA
VDD Operating Current	I_{DD_OP}	SR driver is disabled	--	10	--	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	In sleep mode	--	900	--	µA
VDD Over-Voltage Protection Threshold Voltage	V_{VDD_OVP}		14.5	15.5	16.5	V
VDD Over-Voltage Protection Threshold Voltage for Disable SR Driver	$V_{VDD_OVP_SR}$	With respect to V_{REF_CV}	104.5	110	115.5	%
VDD Over-Voltage Protection Deglitch Time	t_{D_VDDOVP}	(Note 5)	--	50	--	µs
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} = 5V	20.5	21.6	22.7	MHz

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Internal Bias							
V5 Bias	V_{BIAS_V5}	6V < V_{DD} < 16.5V		4.75	5	5.25	V
V5 Load Regulation		1mA < I_{BIAS_V5} < 30mA		--	--	150	mV
V5 Output Short Circuit Current	I_{V5_SC}			60	90	120	mA
V2 Bias	V_{BIAS_V2}	3V < V_{DD} < 16.5V		1.71	1.8	1.89	V
V2 Load Regulation		1mA < I_{BIAS_V2} < 20mA		--	--	20	mV
V2 Output Short Circuit Current	I_{V2_SC}			30	50	70	mA
Regulator Section							
Internal Resistor between VFB and VDD	R_{FB1}	For RT7205A		64	80	96	kΩ
		For RT7205AL		24	30	36	
Internal Resistor between VFB and GND	R_{FB2}			16	20	24	kΩ
V_{OUT} Scaling Factor	K_{VOUT}	(R_{FB1} + R_{FB2}) / R_{FB2} For RT7205A		4.95	5	5.05	--
		(R_{FB1} + R_{FB2}) / R_{FB2} For RT7205AL		2.475	2.5	2.525	
Default Reference Voltage for CV Regulators	$V_{REF_CV_ST}$	For RT7205A		0.97	1	1.03	V
		For RT7205AL		1.94	2	2.06	
Register -Programmable Default Reference Voltage for CC Regulators	$V_{REF_CC_ST}$		0	0.72	0.8	0.88	V
			1	0.99	1.1	1.21	
Maximum DAC Output Voltage for CV Regulators	$V_{REF_CV_MAX}$	With 10-bit Digital to Analog Converter		2.67	2.70	2.73	V
Maximum DAC Output Voltage for CC Regulators	$V_{REF_CC_MAX}$	With 10-bit Digital to Analog Converter		2.67	2.70	2.73	V
Maximum ADC Sense Voltage	V_{ADC_MAX}	10-bit A/D conversion		2.67	2.70	2.73	V
Ratio of Change in Reference Input Voltage to Change in OPTO Voltage	$\frac{\Delta V_{REF}}{\Delta V_{OPTO}}$	ΔV_{OPTO} = 16.5V to V_{REF} (Note 5)		–2.4	–1.2	--	mV/V
Reference Input Current	I_{REF}	(Note 5)		--	0.1	--	µA
Off-State OPTO Current	I_{OPTO_OFF}	OPTO pin is open-circuited (Note 5)		--	230	500	nA
Dynamic Impedance	$\lvert Z_{OPTO} \rvert$	V_{OPTO} = V_{REF}, I_{OPTO} = 1mA, f < 1kHz (Note 5)		--	0.22	0.5	Ω
OPTO Turn-On Impedance	R_{ON_OPTO}	I_{OPTO_SINK} = 20mA		--	--	200	Ω
Maximum OPTO Sinking Current	I_{OPTO_MAX}			2	--	20	mA
Internal Resistor between OPTO and VDD	R_{OPTO_VDD}			40.8	51	61.2	kΩ
Internal Resistor between OPTO and GND	R_{OPTO_GND}			50	60	70	kΩ

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Current Sense Amplifier							
Current-Sense Voltage Gain	K_{CS}			--	40	--	V/V
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			--	0.5	--	V
Unit Gain Bandwidth		(Note 5)		1000	--	--	kHz
Output Current		(Note 5)		--	0.1	--	mA
Charge Pump Section							
Charge Pump Operating Frequency	f_{CP}			150	170	190	kHz
Rise Time	t_{R_CP}	C_L = 6nF, V_5 = 5V, from 20% to 80%		70	140	210	ns
Fall Time	t_{F_CP}	C_L = 6nF, V_5 = 5V, from 80% to 20%		60	110	160	ns
Charge Pump Driver Impedance	R_{OUT_CP}	(Note 5)		--	--	10	Ω
Debounce Time	t_{D_V9}	(Note 5)		--	50	--	µs
V9 Turn-On Threshold Voltage	V_{V9_ON}			3.1	3.3	3.5	V
V9 Turn-Off Threshold Voltage	V_{V9_OFF}	If $V_9 < V_{V9_OFF}$, the V9 internal circuit will be inactivated.		2.9	3.1	3.3	V
RT Section							
Open-Loop Voltage	V_{RT_OP}	V_{DD} = 5V		3.2	3.6	4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}		00	90	100	110	µA
			01	18	20	22	
			10	3.6	4	4.4	
			11	Open			
OVP Section							
Maximum OVP Sinking Current	I_{OVP_MAX}			2	--	20	mA
Pull-Low Impedance	R_{L_OVP}	I_{OVP_MAX} = 20mA		--	--	200	Ω
Register-Programmable Over-Voltage Protection Threshold	V_{VOUT_OVP}	With respect to V_{REF_CV}	00	109.25	115	120.75	%
			01	114	120	126	
			10	118.75	125	131.25	
			11	Disable			
Debounce Time	$t_{D_VOUTOVP}$	OVP pin is latched till VDD is below V_{VDD_OFF}		--	50	--	µs
BLD Section							
Maximum BLD Sinking Current	I_{BLD_MAX}	V_{BLD} = 12V, In 300ms (Note 5)		0.2	--	0.7	A
Pull-Low Impedance	R_{L_BLD}	I_{BLD} = 50mA		--	--	30	Ω

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
D+, D- Section							
Pull-High Resistance	R_{H_DPDM}			10	12.5	15	kΩ
Pull-Low Resistance	R_{L_DMDM}			15	20	25	kΩ
Register-Programmable Output High Voltage	V_{OH_OP}	V_{DD} = 5V, R_L = 15kΩ	00	Open Drain			V
	$V_{OH_3.3V}$		01	2.97	3.3	3.63	
	$V_{OH_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH_4.2V}$		11	3.78	4.2	4.62	
Output Low Voltage	V_{OL_OP}	R_L = 15kΩ		--	--	0.2	V
	$V_{OL_3.3V}$						
	$V_{OL_1.8V}$						
	$V_{OL_4.2V}$						
Register-Programmable DP and DM Input Level	V_{IN_LEV}		0	--	0	--	V
			1	--	0.4	--	
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	1.3 + V_{IN_LEV}	V
			01	1.2 + V_{IN_LEV}	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	
			10	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	1.5 + V_{IN_LEV}	
			11	1.4 + V_{IN_LEV}	1.5 + V_{IN_LEV}	1.6 + V_{IN_LEV}	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	1.0 + V_{IN_LEV}	V
			01	0.9 + V_{IN_LEV}	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	
			10	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	
			11	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	1.3 + V_{IN_LEV}	
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
DP Comparison Threshold for Cable Detection	$V_{TH_DP_CD}$	Send an interrupt to MCU when cable detached		0.2	0.3	0.4	V
Register-Programmable Cable Detection Debounce Time	t_{DP_CD}	Debounce Time = t_{DP_CD} x K_{tDP_CD} (Note 5)	00	--	1	--	µs
			01	--	2	--	
			10	--	4	--	
			11	--	8	--	

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Register-Programmable Cable Detection Debounce Time Scale	K_{tDP_CD}	(Note 5)	00	--	1	--	--
			01	--	8	--	
			10	--	64	--	
			11	--	512	--	
CC1, CC2 Section							
Register-Programmable Input High Trip Voltage	V_{IH_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Register-Programmable Sourcing Current	I_{CC_SRC}		00	High Impedance			µA
			01	72	80	88	
			10	166	180	194	
			11	304	330	356	
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_OP}			2.5	2.6	2.7	V
USBP Section							
Output High Voltage	V_{OH_USBP}			V_{DD} + 6	V_{DD} + 8	V_{DD} + 10	V
Register-Programmable Rise Time	t_{R_USBP}	C_L = 4nF, V_{DD} = 5V, from 20% to 80%	00	3840	4800	5760	µs
			01	1920	2400	2880	
			10	980	1200	1440	
			11	480	600	720	
Fall Time	t_{F_USBP}	C_L = 4nF, V_{DD} = 5V, from 90% to 10%		--	--	2	µs
Output Low Voltage	V_{OL_USBP}	V_{DD} = 2V, I_{USBP} = 100µA before start-up		--	--	1	V
SR Driver Section							
Output High Voltage	V_{OH_VG}	I_{SOURE} = 50mA, V_9 = 9V		8.5	--	--	V
Output Low Voltage	V_{OL_VG}	I_{SINK} = 50mA, V_9 = 9V		--	--	0.5	V
Rise Time	t_{R_VG}	C_L = 6nF, V_9 = 9V, from 20% to 80%		--	75	125	ns
Fall Time	t_{F_VG}	C_L = 6nF, V_9 = 9V, from 80% to 20%		--	35	85	ns
Propagation Time	t_P			--	100	--	ns

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Initial Output Low Clamping Voltage before Start-up	$V_{OL_VG_INI}$	V_{DD} = 2.5V, I_{SINK} = 50mA		--	--	1	V
Internal Pull-Low Resistor	R_{GS_LOW}			--	20	--	kΩ
V_TR Section							
V_TR Internal Resistance	R_{VDS2}			4.56	4.80	5.04	kΩ
V_TR Sample and Hold Error	E_{SH_VTR}	($\lvert V_{V_TR_HIGH} - V_{VTR_SH} \rvert$ / $V_{V_TR_HIGH}$) x 100		--	5	--	%
V_TR Sample and Hold Threshold	K_{VTR_SH}	$V_{TH_SH} = K_{VTR_SH}$ x $V_{V_TR_HIGH}[n-1]$		--	0.875	--	--
Mask Time	t_{MASK}	$V_{V_TR} > V_{TH_SH}$		--	300	--	ns
Register-Programmable V_TR Blanking Time	t_{BLANK_VTR}	$V_{V_TR} > V_{TH_SH}$ (Note 5)	000	0.4	0.5	0.6	µs
			001	0.6	0.7	0.8	
			010	0.8	0.9	1.0	
			011	1.0	1.1	1.2	
			100	1.2	1.3	1.4	
			101	1.4	1.5	1.6	
			110	1.6	1.7	1.8	
			111	1.8	1.9	2	
Register-Programmable V_TR Under Voltage Threshold	$V_{TH_VTR_UV}$	If $V_{V_TR_HIGH}$ - (V_{OUT} x K_{VDS_SR}) > $V_{TH_VTR_UV}$, SR driver is active.	000	Disable			V
			001	0.3	0.4	0.5	
			010	0.25	0.35	0.45	
			011	0.2	0.3	0.4	
			100	0.15	0.25	0.35	
			101	0.1	0.2	0.3	
			110	0.05	0.15	0.25	
			111	0	0.1	0.2	
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When $V_{V_TR} < K_{VIN_LOW}$ x V_{OUT}, It will send an interrupt to MCU.		2.0	2.2	2.4	--
V_TR Over-Voltage Threshold	$V_{TH_VTR_OV}$	V_9 = 4.5V		2.8	3.0	3.2	V
Low Level Threshold for V_TR Falling Edge Detection and Dead Time Comparison Threshold	$V_{TH_VTR_DT}$			0.05	0.10	0.15	V
Dead Time Comparator Delay	t_{D_DT}	(Note 5)		--	--	40	ns
Dead Time Comparator Blanking Time	t_{BLANK_DT}	Disable dead time comparator on VG rising edge		--	700	--	ns

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Register-Programmable V_TR Falling Time Threshold	$t_{V_TR_FALLING}$	If V_TR falling time < $t_{V_TR_FALLING}$, VG will be triggered.	00	200	250	300	ns
			01	150	200	250	
			10	100	150	200	
			11	50	100	150	
Register-Programmable V_TR Falling Edge Debouce Time	t_{D_VTR}		0	--	0.15	--	µs
			1	--	0	--	
V_TR Rising Edge Threshold for AC OFF Detection	$V_{V_TR_EDGE}$			0.05	0.1	0.15	V
V_TR Rising Edge Debouce Time for AC OFF Detection	$t_{V_TR_EDGE}$	If V_{V_TR} in $t_{V_TR_EDGE}$ is lower than $V_{V_TR_EDGE}$, It will send an AC OFF interrupt to MCU.		20	26	32	ms
SR Control Section							
SR MOSFET V_{DS} Scaling Factor	K_{VDS_SR}	R_{VDS2} / (R_{VDS1} + R_{VDS2}) For RT7205A (Note 5)		--	1/26	--	--
		R_{VDS2} / (R_{VDS1} + R_{VDS2}) For RT7205AL (Note 5)		--	1/13	--	
Register-Programmable gm Ratio	$\frac{gm_{V_TR}}{gm_{VOUT}}$		0	3.84	4.17	4.50	--
			1	3.22	3.57	3.92	
Maximum VG Pulse Width Expansion Limit	t_{SRON_MAX}	$t_{SR_ON}[n] < t_{SR_ON}[n-1] \times t_{SRON_MAX}$ (Note 5)		--	106	--	%
Register-Programmable V_TR Pulse Width Expansion/Shrink Limit	t_{PWLMT_VTR}	If $t_{V_TR}[n] > t_{V_TR}[n-1] + t_{PWLMT_VTR}$ or $t_{V_TR}[n] < t_{V_TR}[n-1] - t_{PWLMT_VTR}$, reset automatic tracking counter (Note 5)	00	--	0.3	--	µs
			01	--	0.5	--	
			10	--	0.7	--	
			11	--	0.9	--	
Register-Programmable Minimum Period	t_{PERIOD_MIN}	Interval limit from V_TR rising edge to VG falling edge. The clock period is based on f_{OSC_MCU} and can be set by the 12-bit register. (Note 5)		--	190	--	µs
Register-Programmable VG Inhibit Time	$t_{INHIBIT_SR}$	Interval limit from VG rising edge to next VG rising edge The clock period is based on f_{OSC_MCU} and can be set by the 9-bit register. (Note 5)		--	24	--	µs

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
PLL Function Section							
Register-Programmable PLL Dead Time	t_{DEAD_PLL}	If VG falling edge to $V_{TH_VTR_DT}$ interval < t_{DEAD_PLL}, reset automatic tracking counter (Note 5)	00	--	1100	--	ns
			01	--	600	--	
			10	--	300	--	
			11	Disable			
Register-Programmable Fault PLL Ratio	K_{FAULT_PLL}	If $t_{PWM}[n] > K_{FAULT_PLL}$ x $t_{PWM}[n-1]$, VG will skipped two cycles and reset automatic tracking counter (Note 5)	0	--	1.5	--	--
			1	Disable			
Automatic Tracking Section							
Register-Programmable Auto-Tracking Dead Time	t_{DEAD_TRACK}	VG falling edge to $V_{TH_VTR_DT}$ interval (Note 5)	00	--	1500	--	ns
			01	--	1000	--	
			10	--	700	--	
			11	--	400	--	
Maximum Step Time for Tracking Up/Down		With respect to V_{REF_CV}		0.5	--	1	%

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

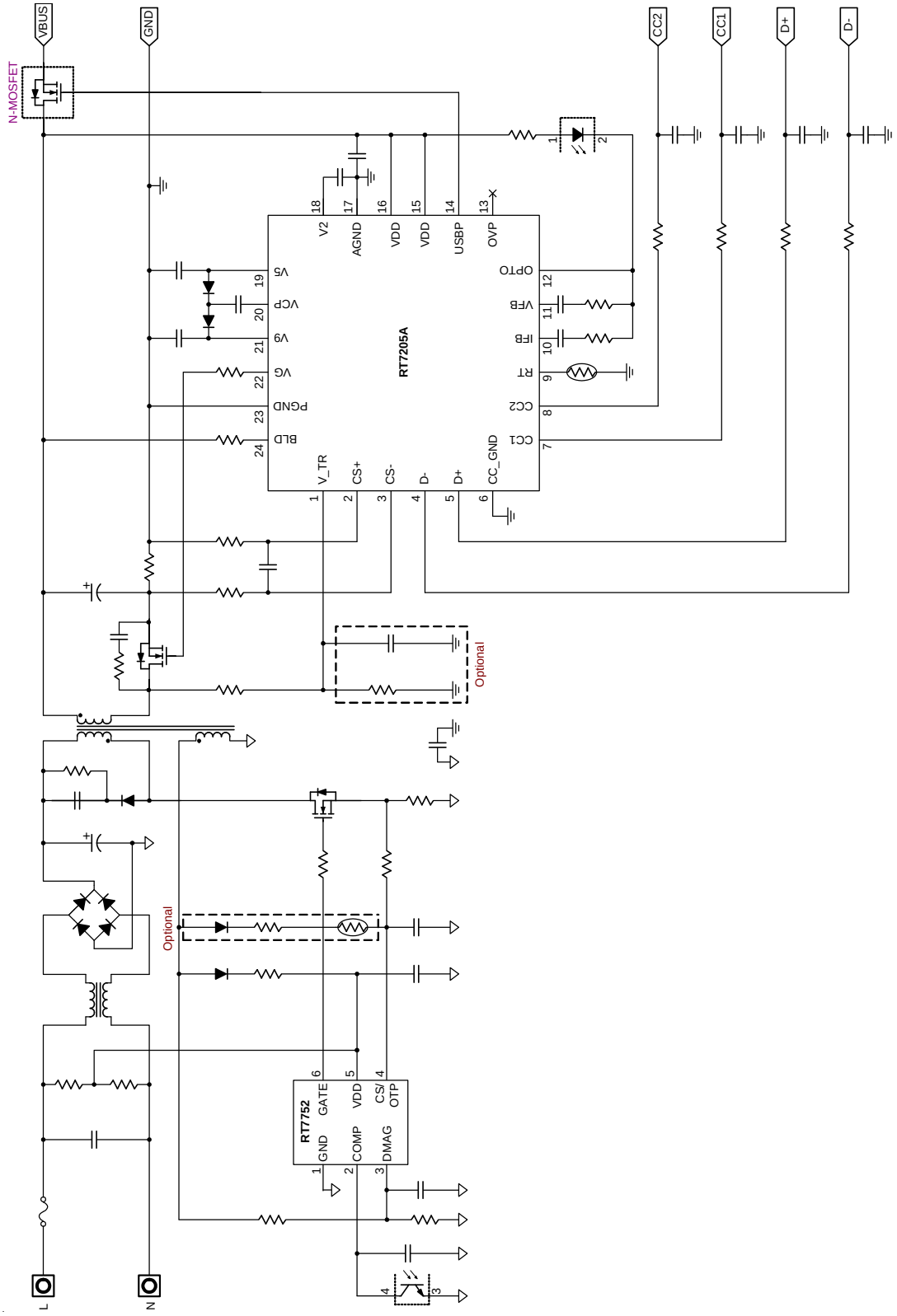
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

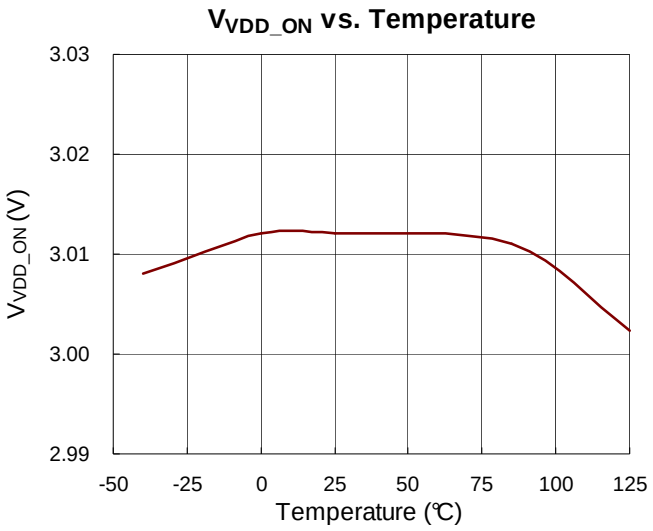
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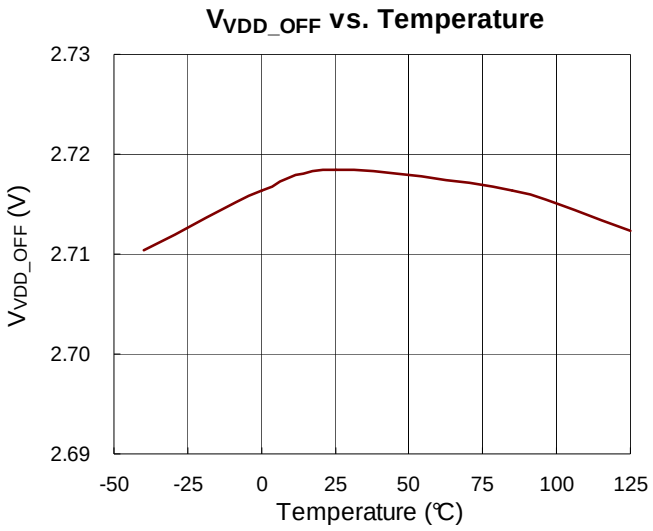
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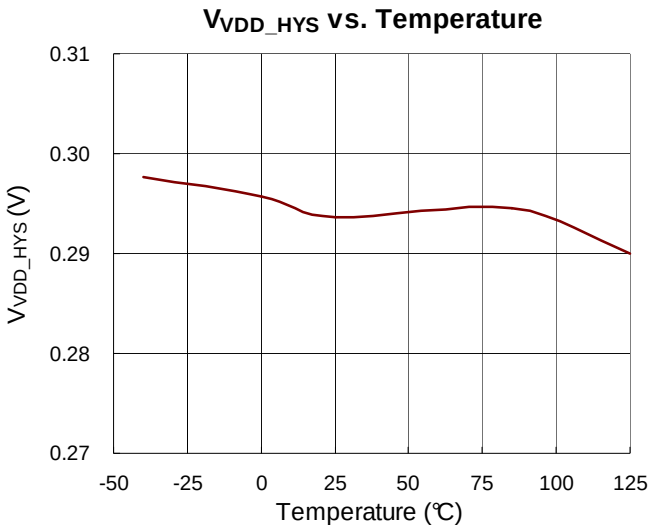


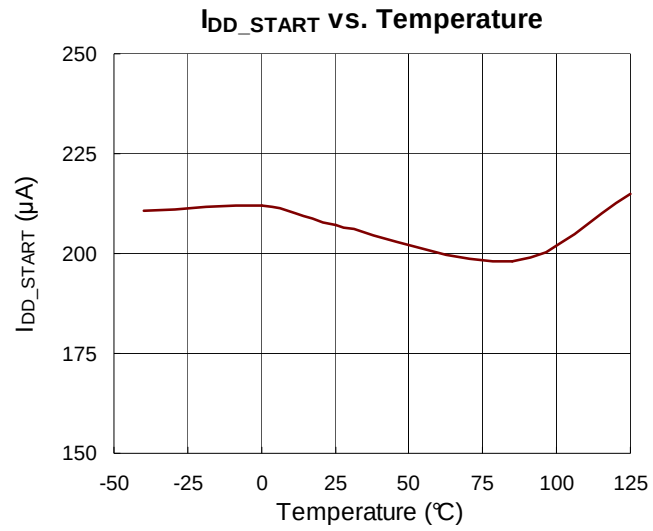
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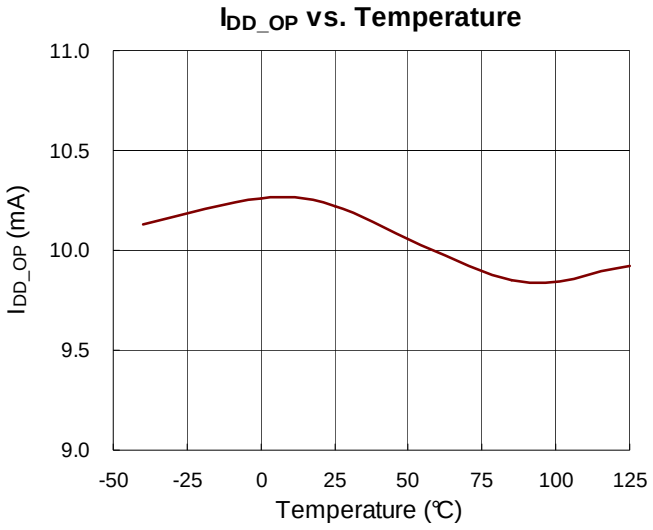
Typical Operating Characteristics

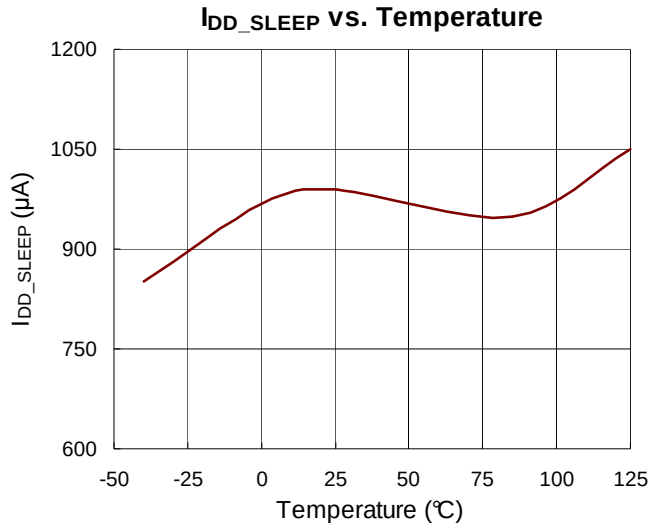




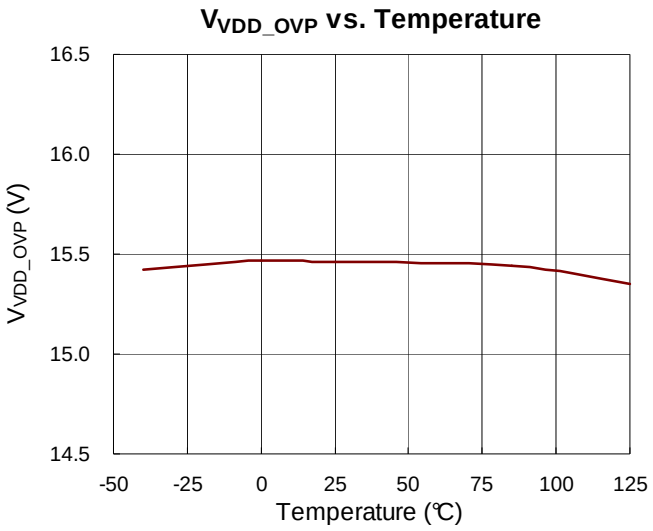


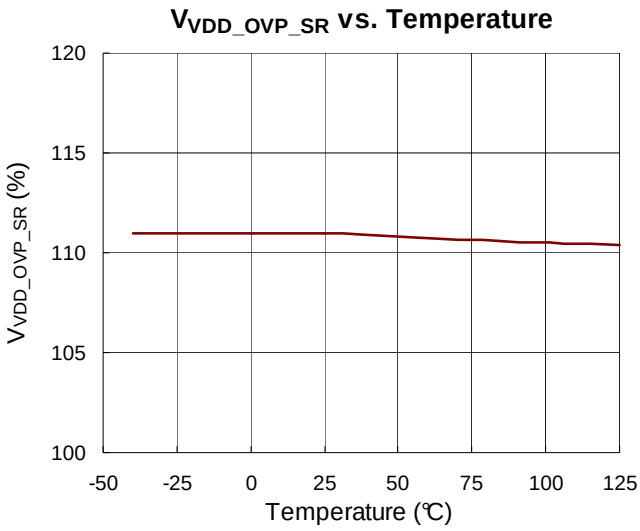


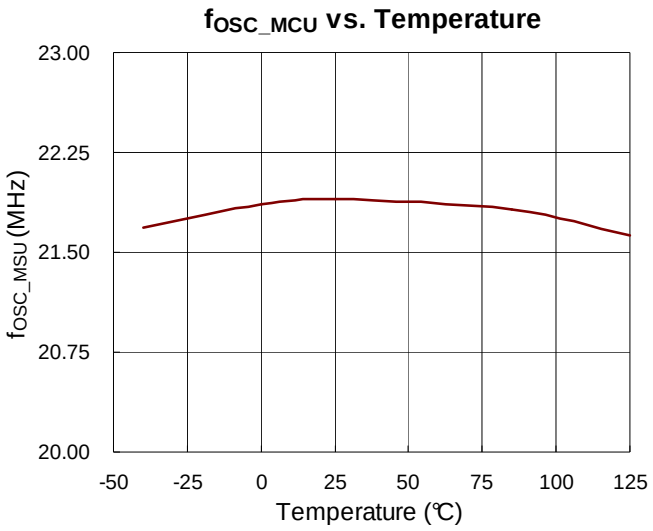


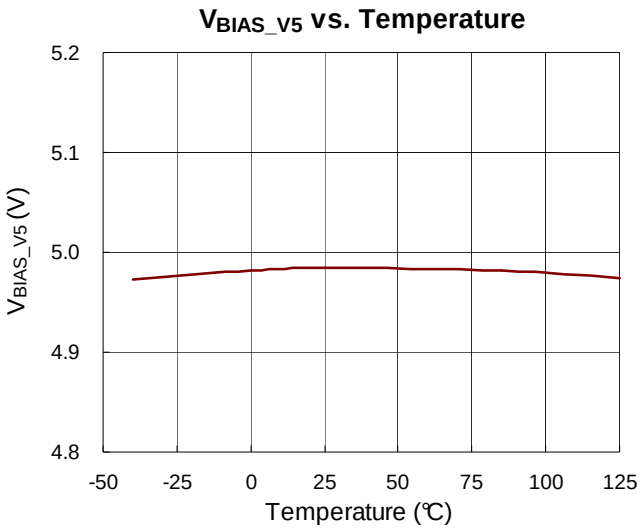


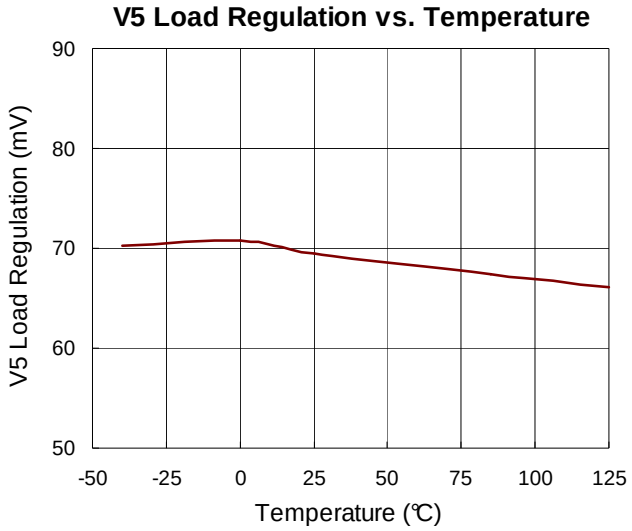
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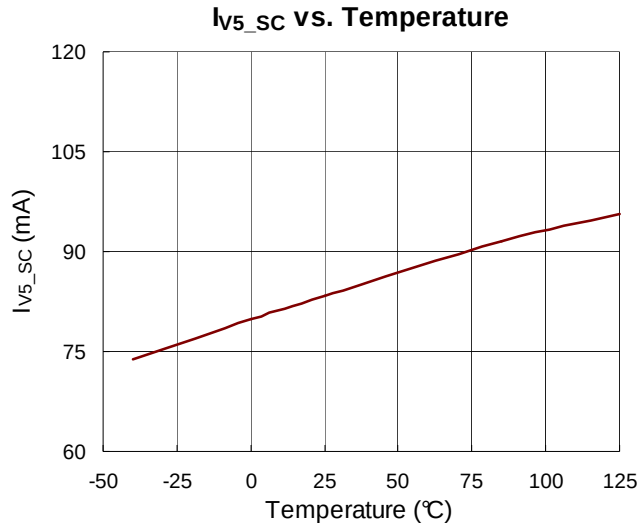




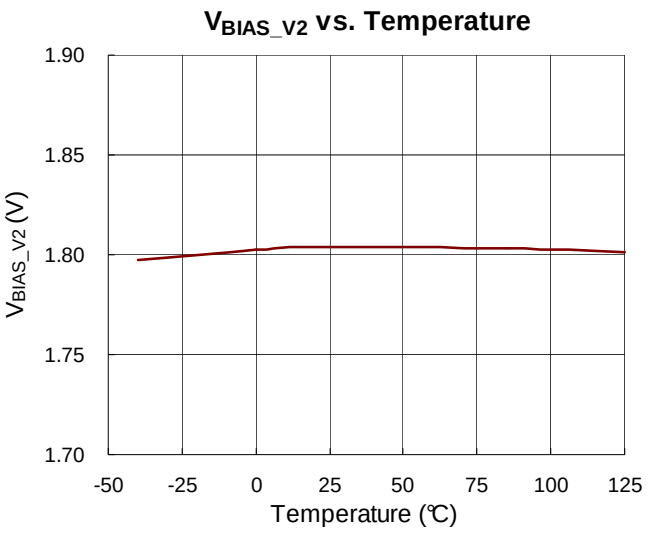


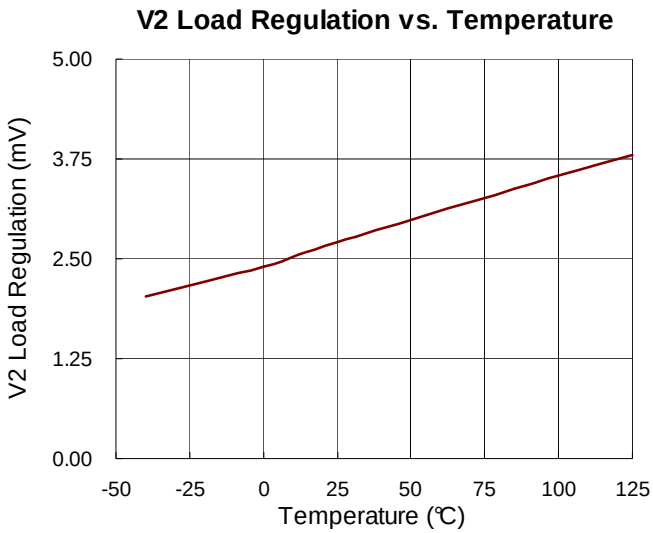


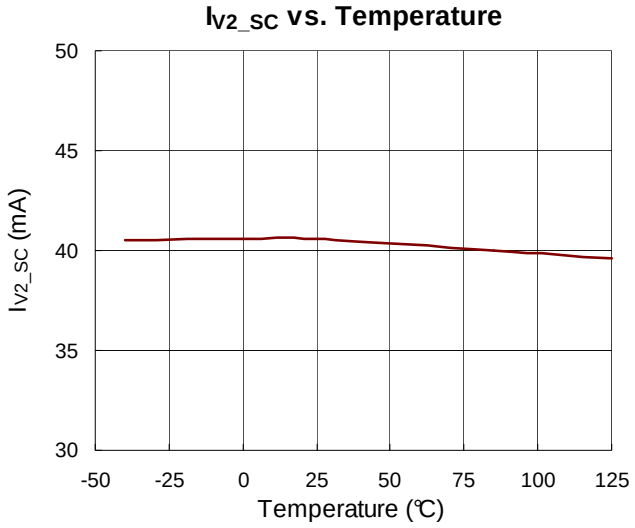


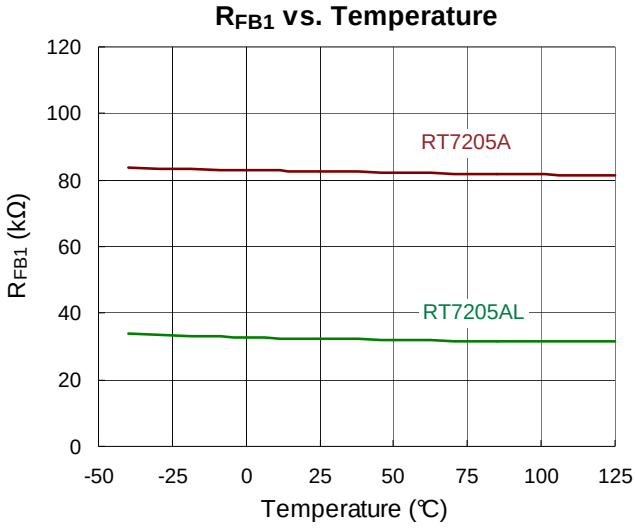


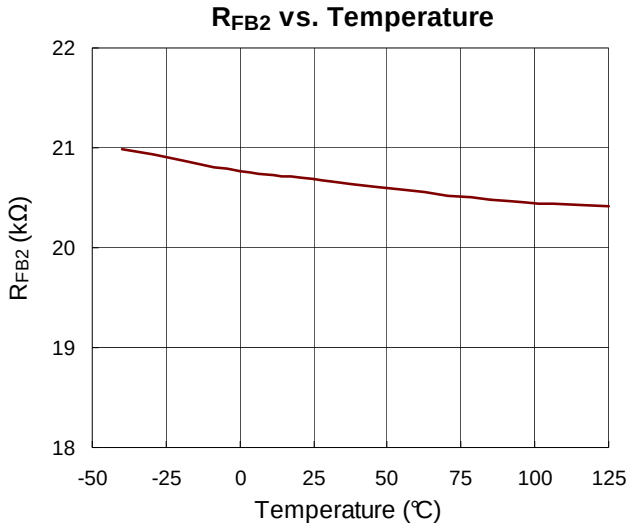
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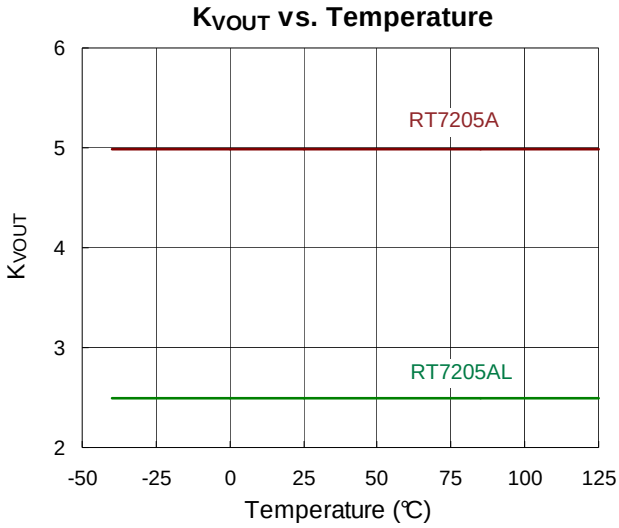




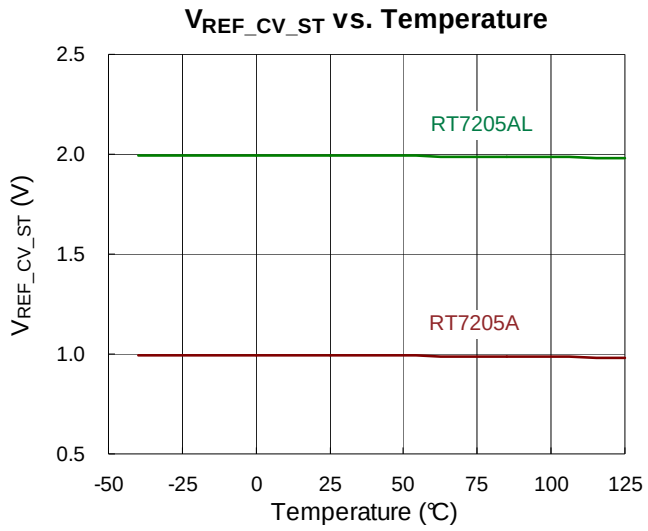


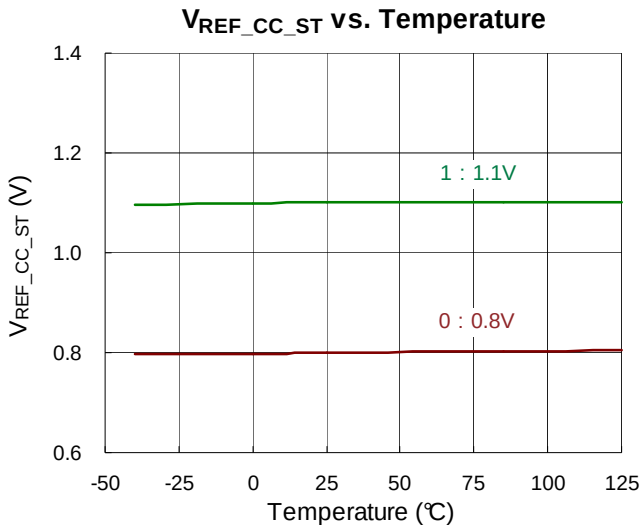


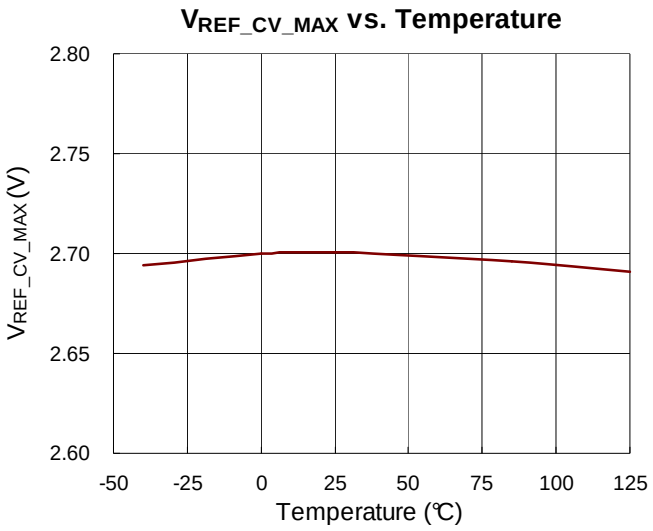


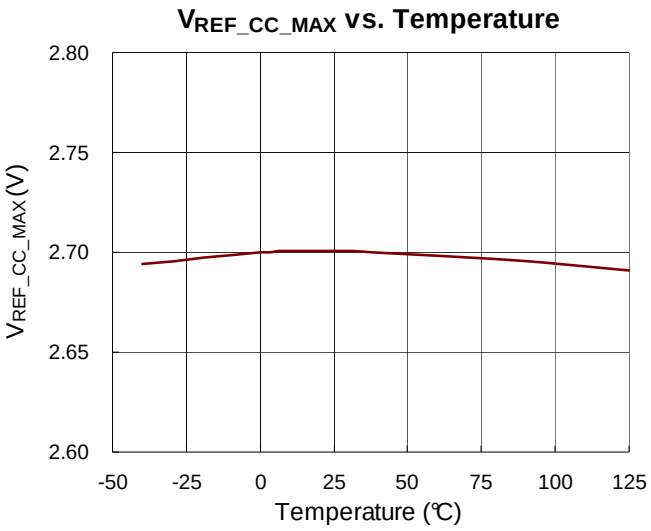


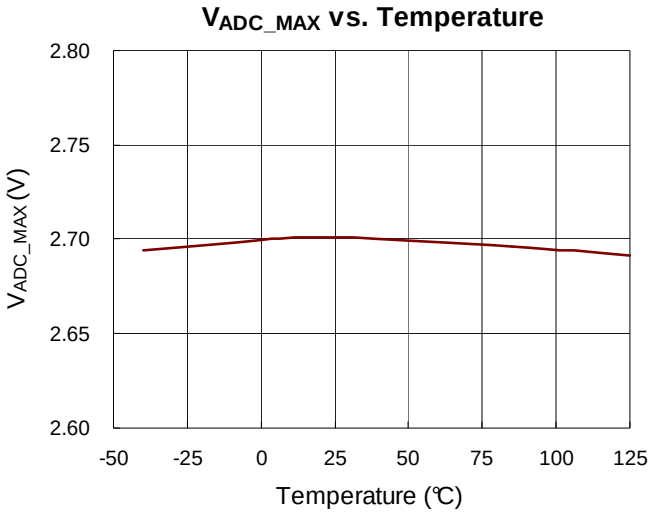
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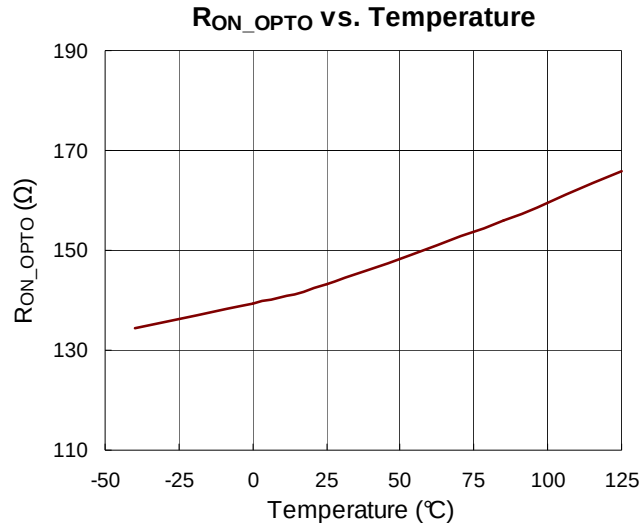






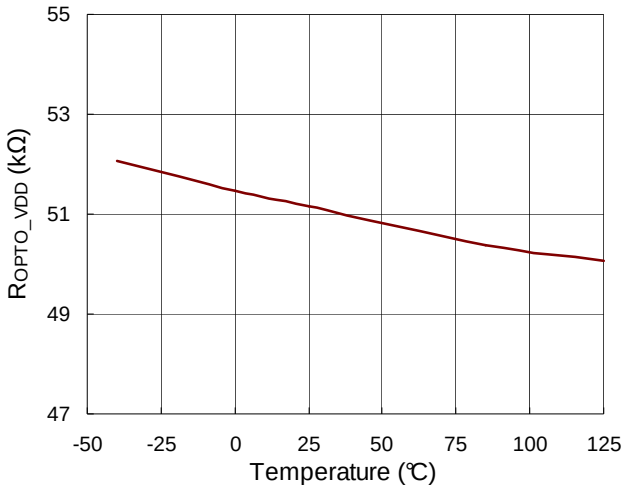




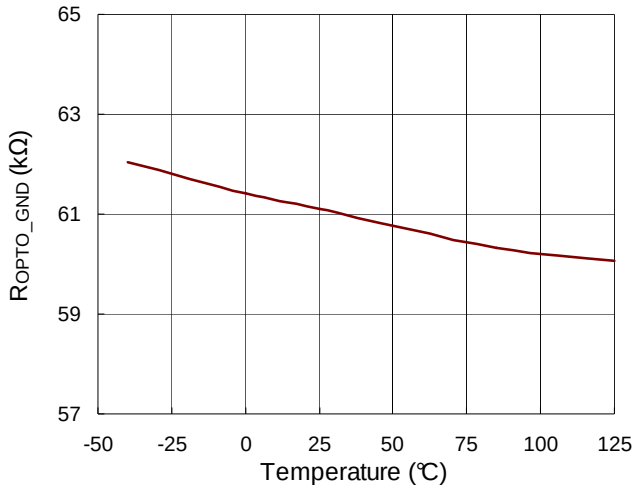


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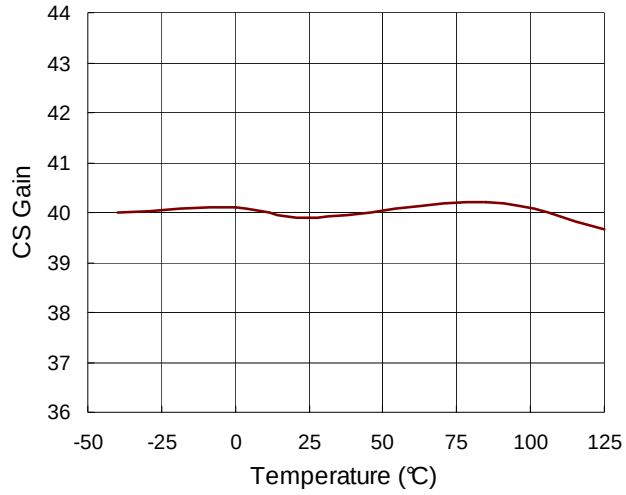
R_{OPTO_VDD} vs. Temperature



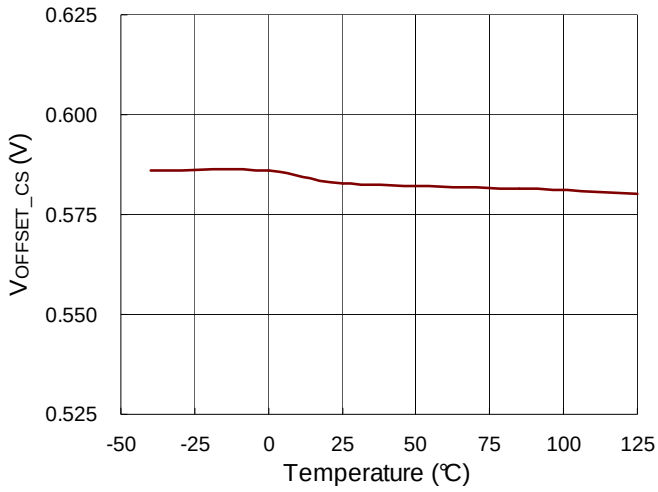
R_{OPTO_GND} vs. Temperature



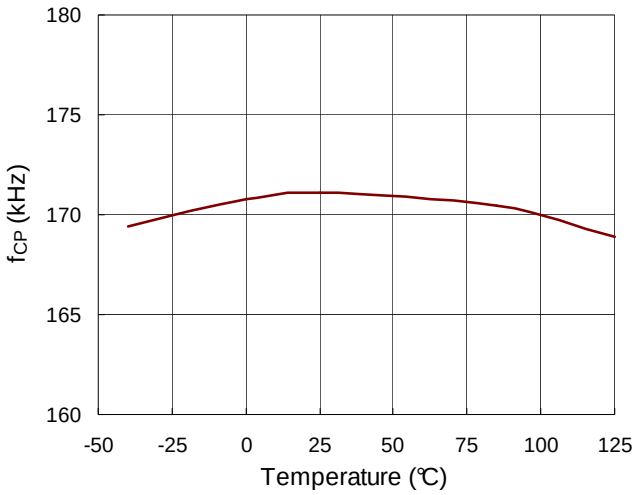
CS Gain vs. Temperature



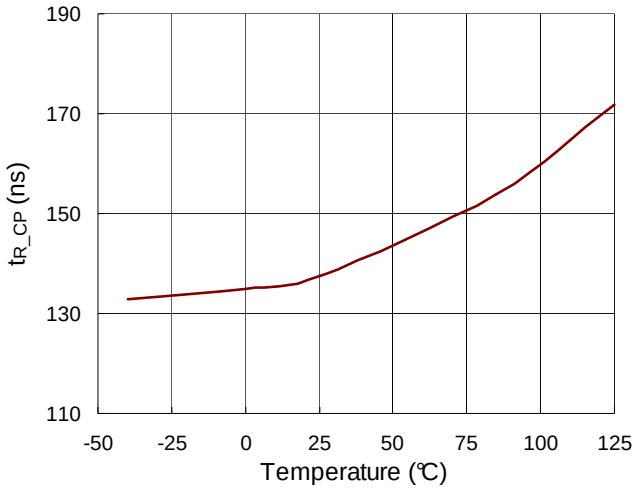
V_{OFFSET_CS} vs. Temperature



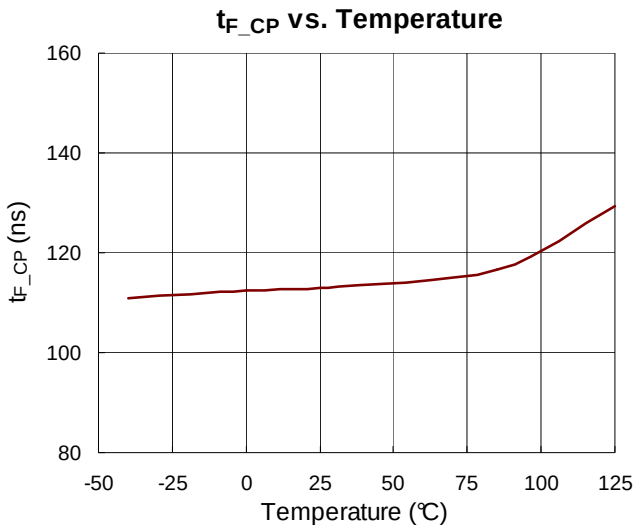
f_{CP} vs. Temperature

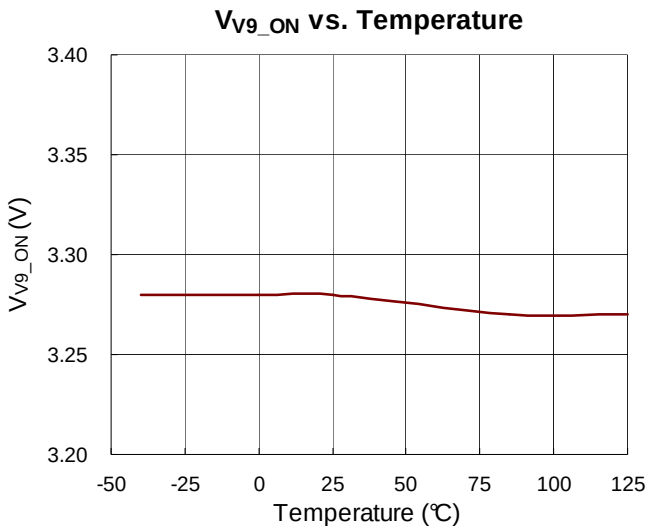


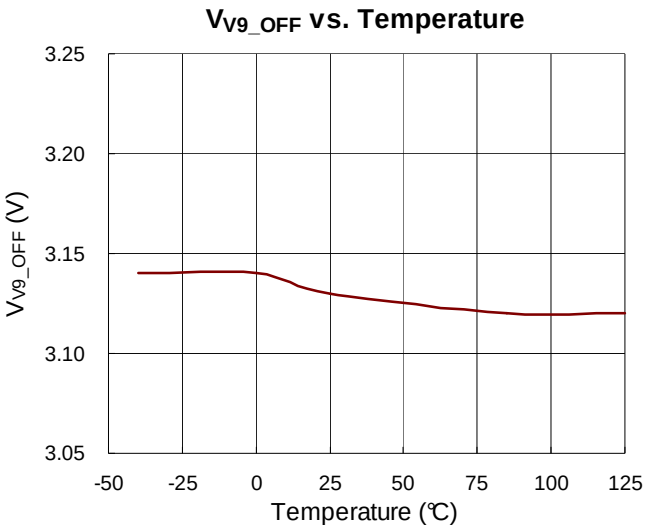
t_{R_CP} vs. Temperature

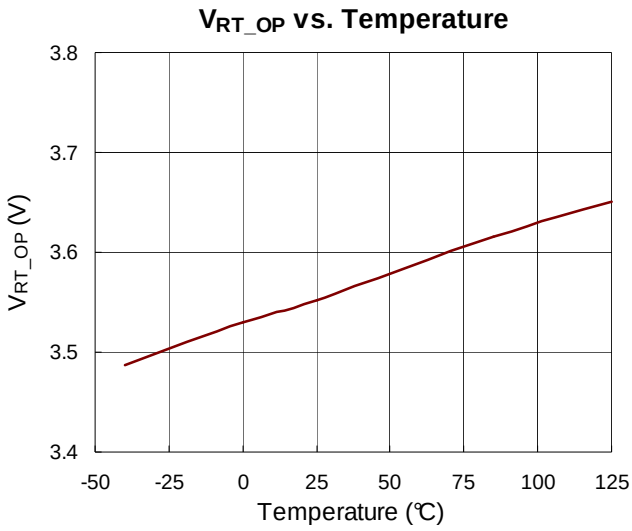


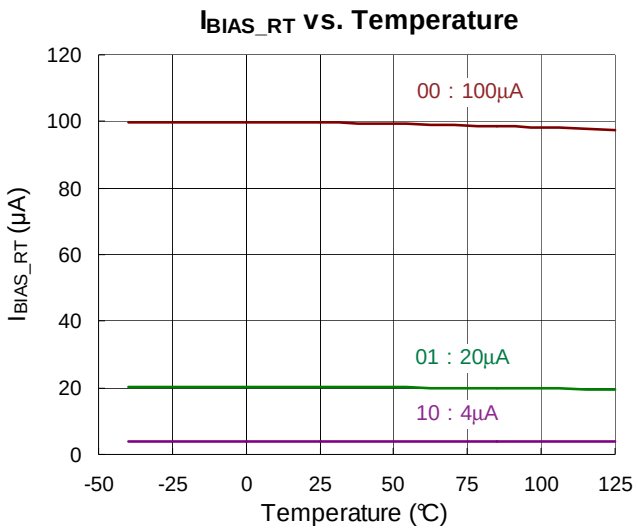
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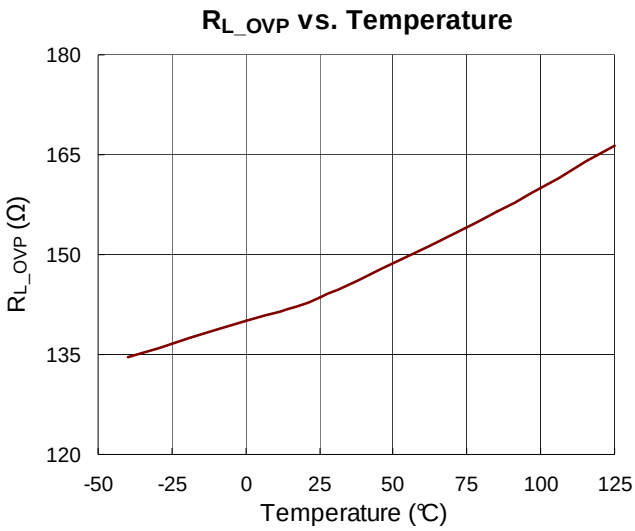




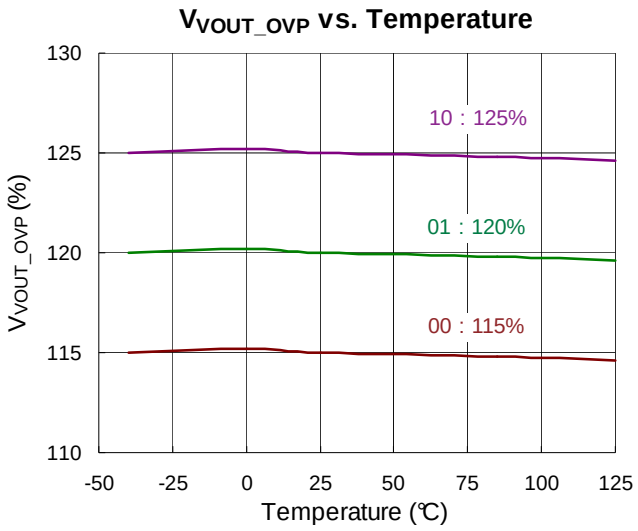


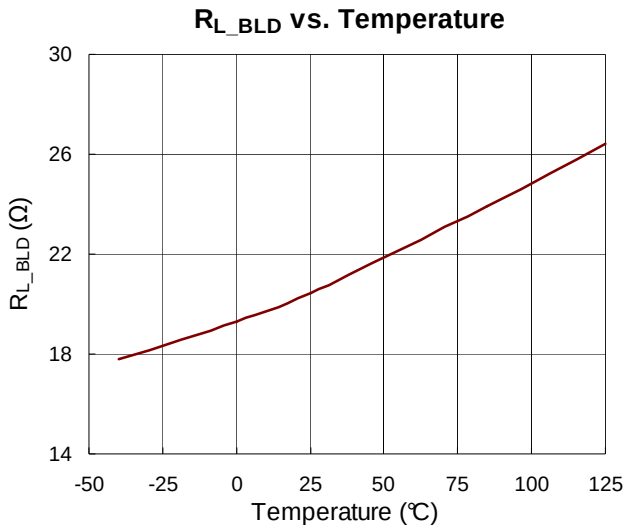


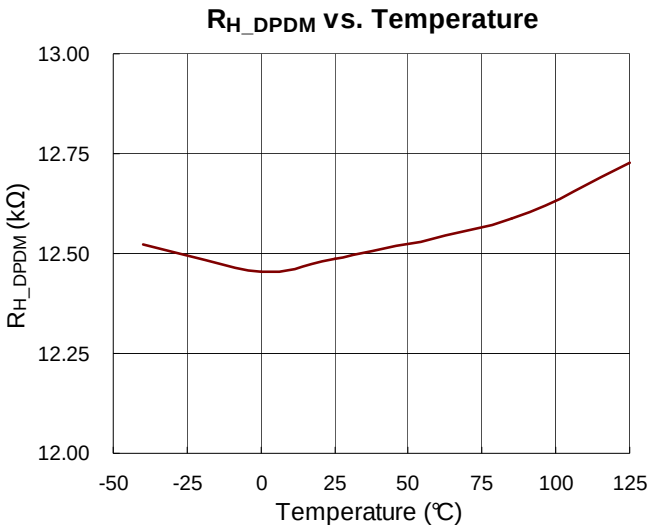


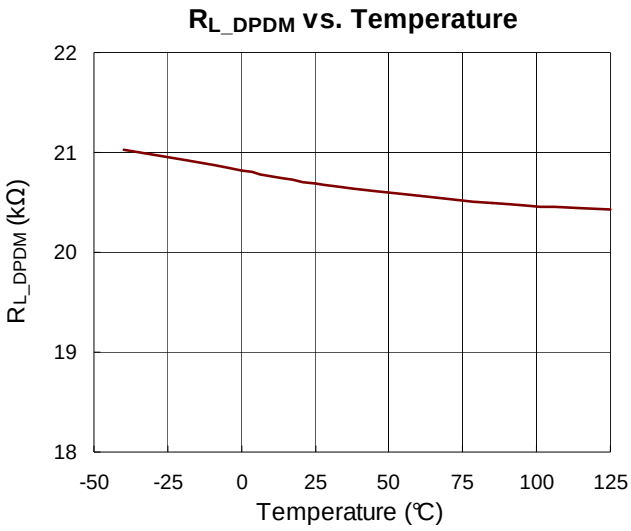


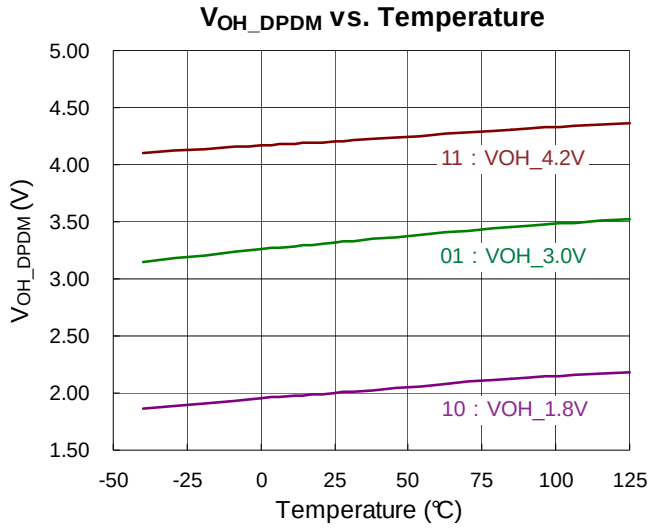
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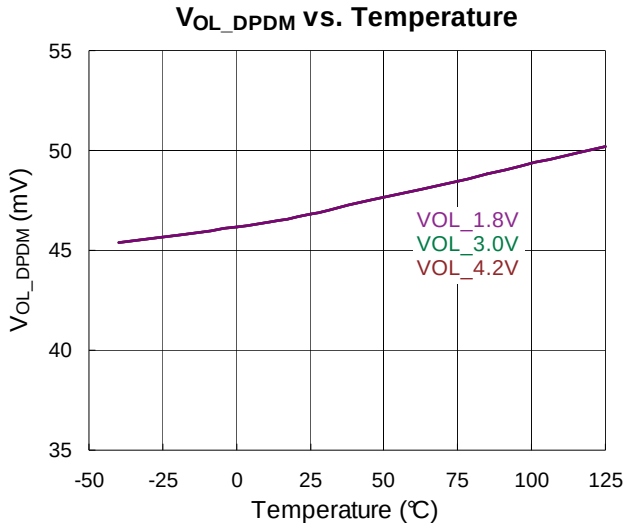




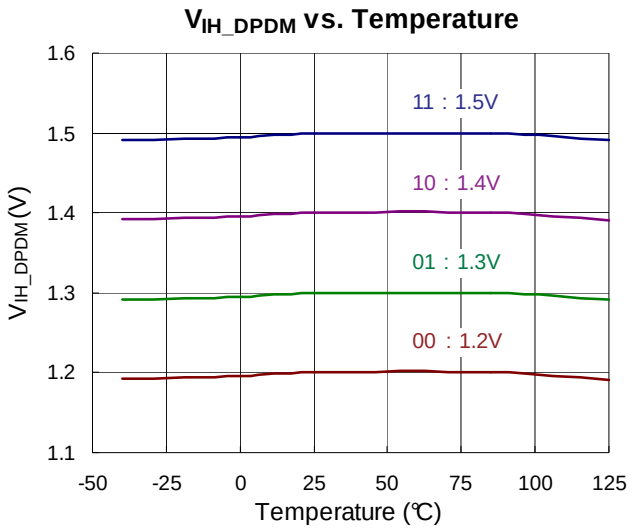


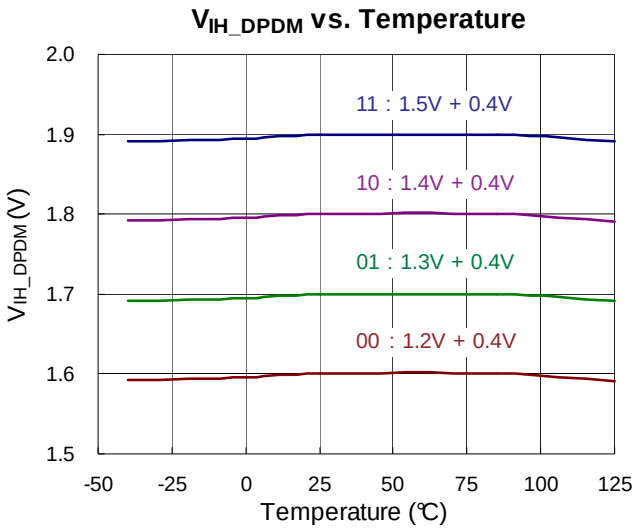


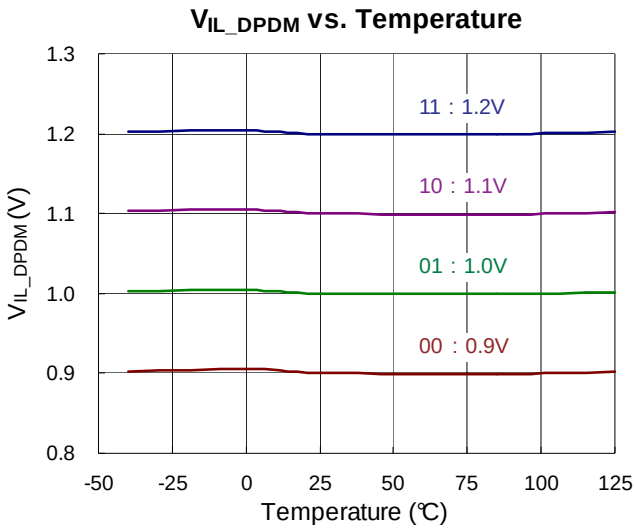


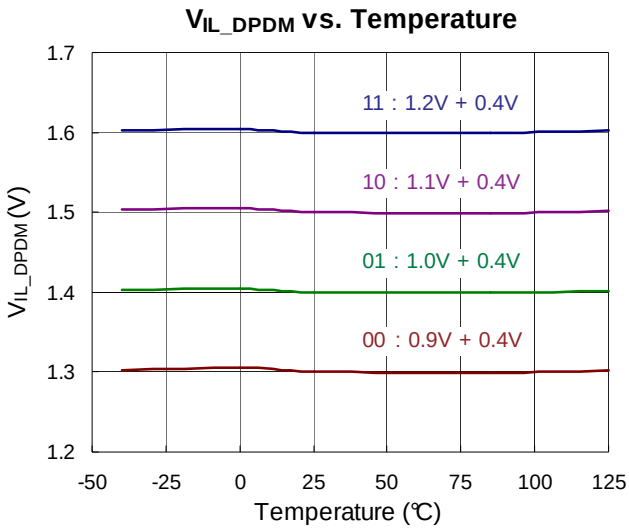


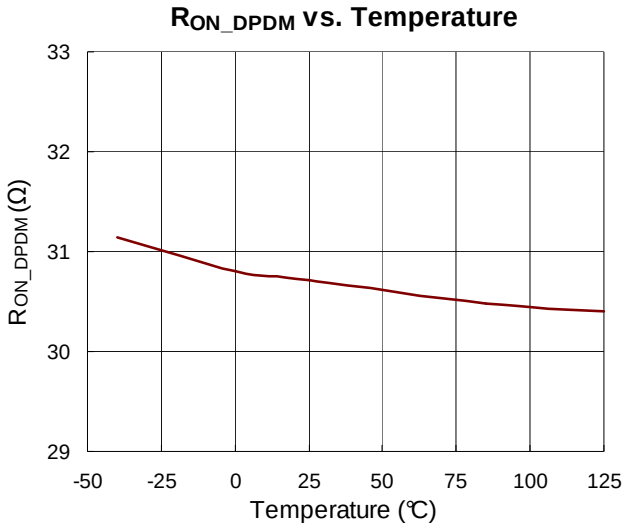
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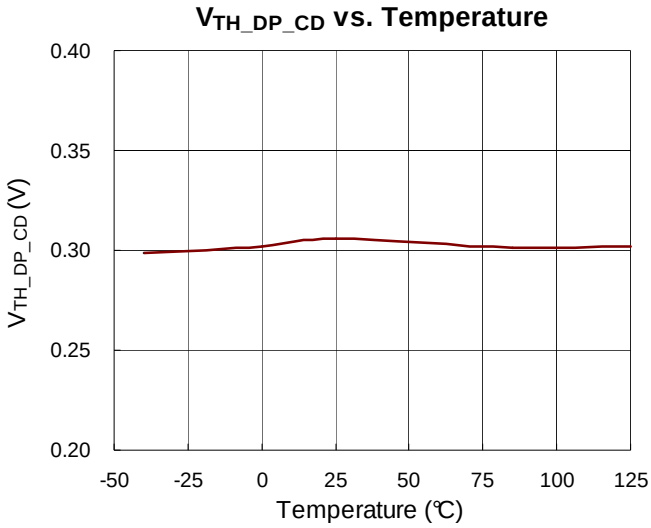




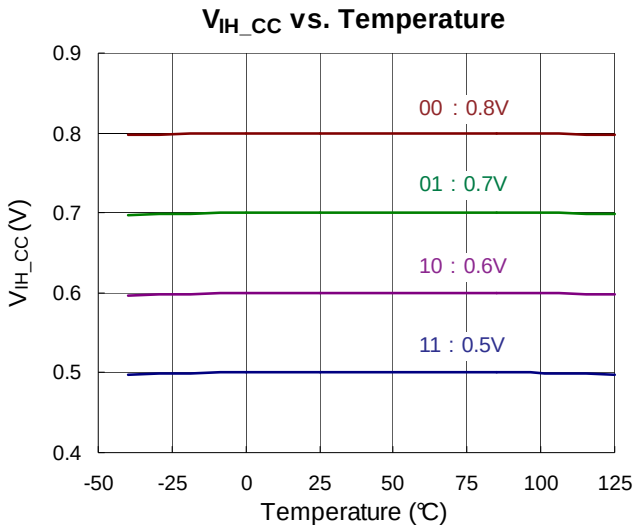


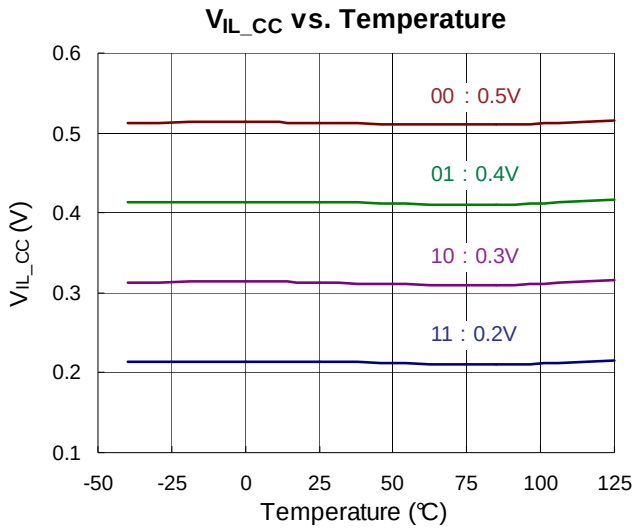


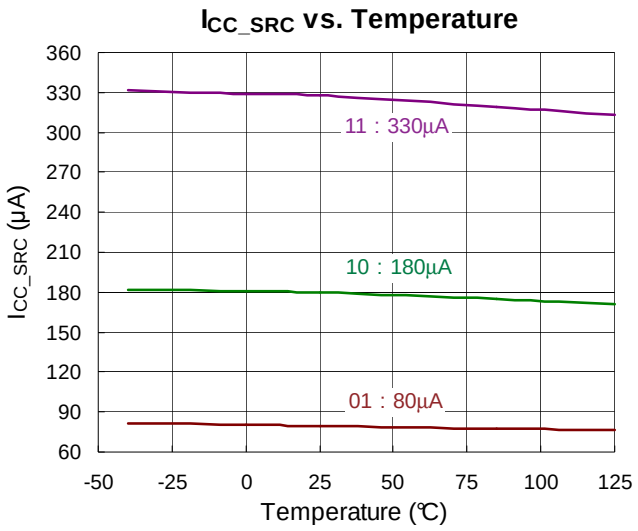


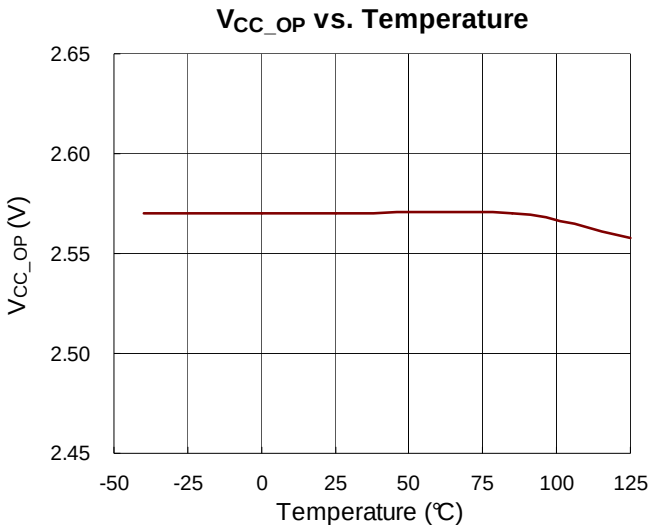


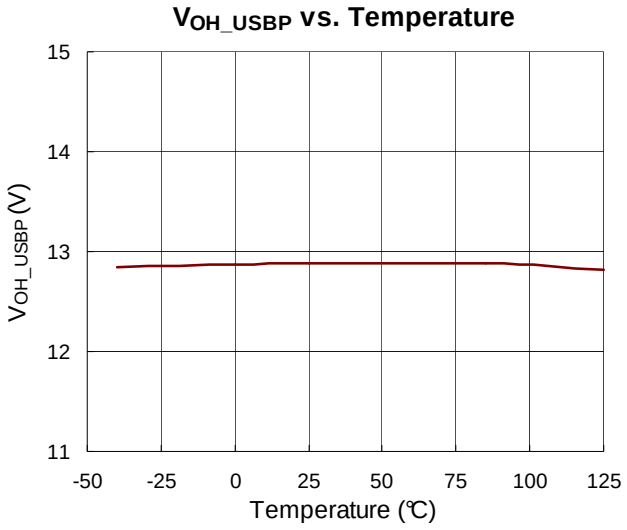
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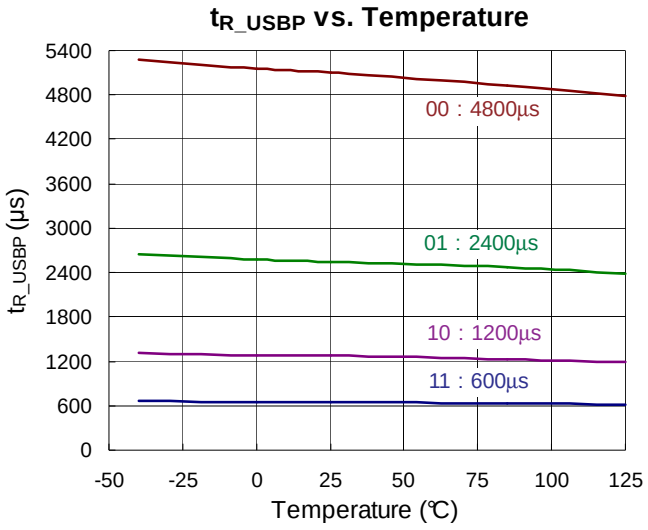




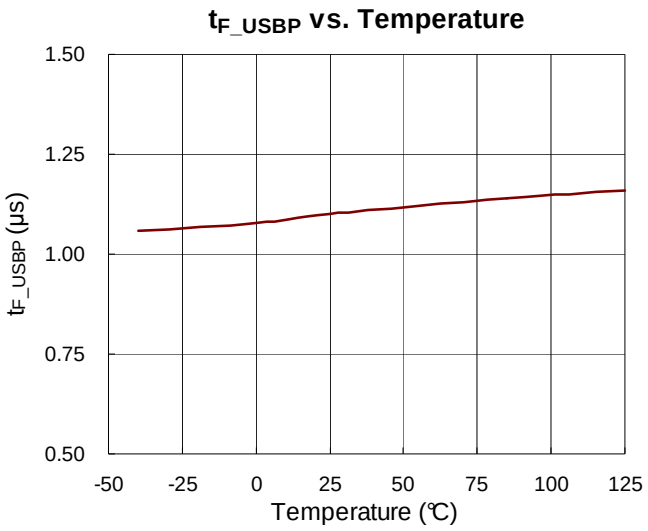


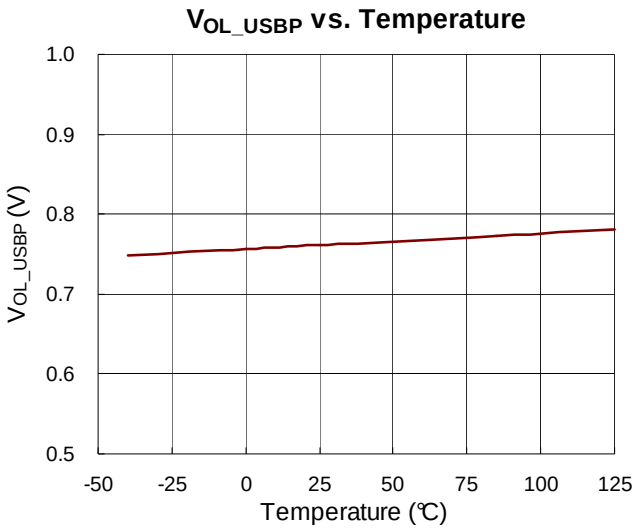


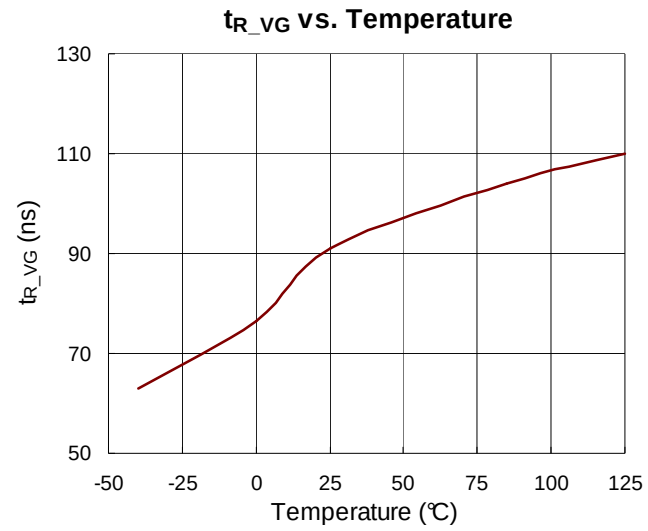


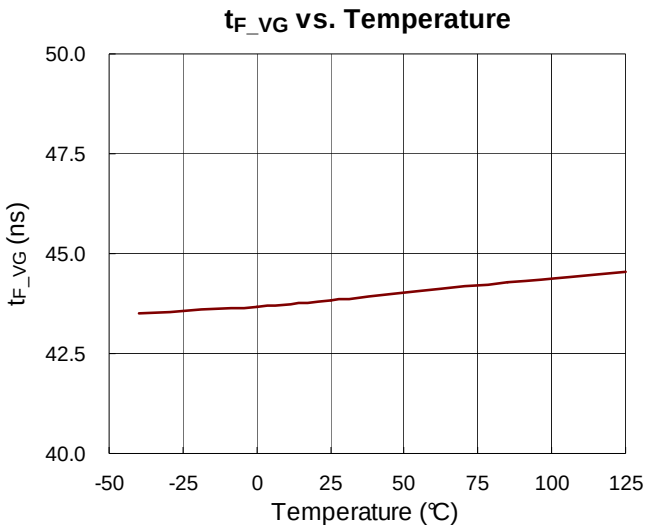


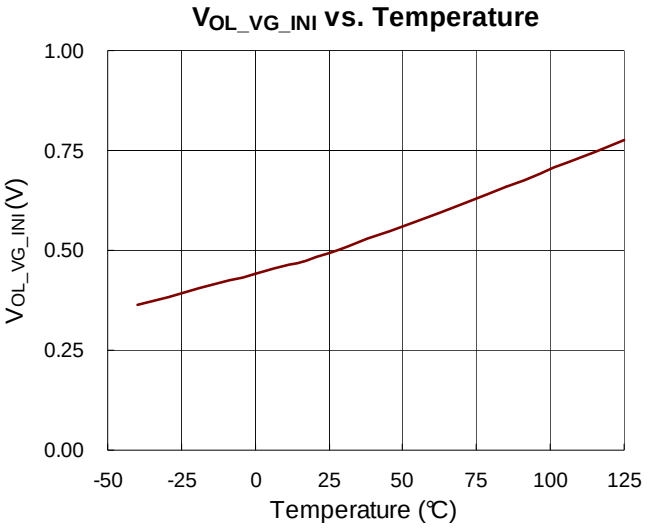
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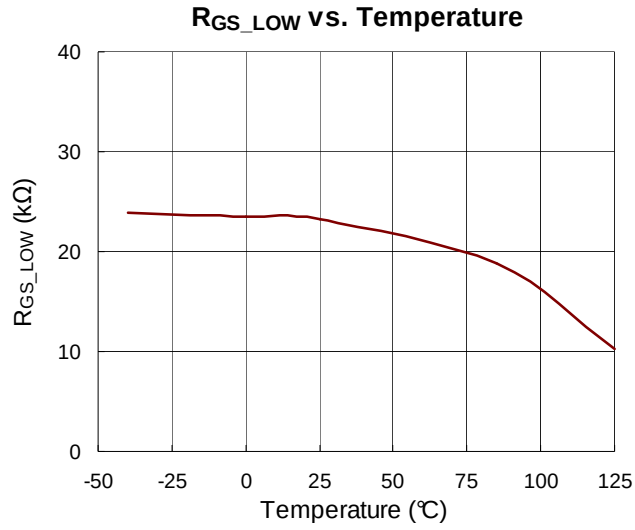




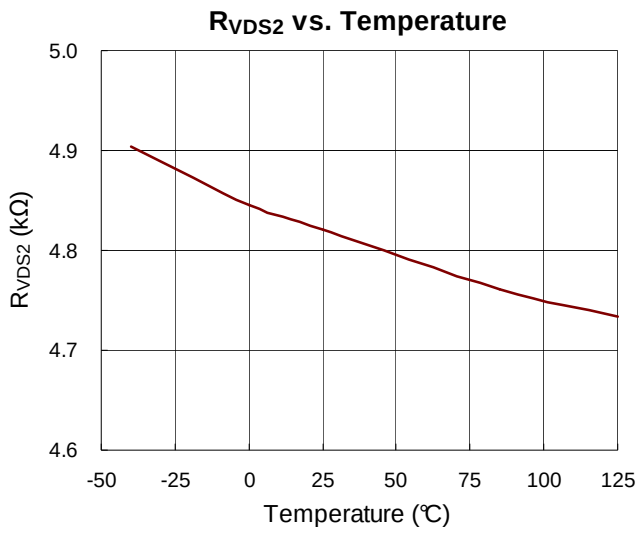


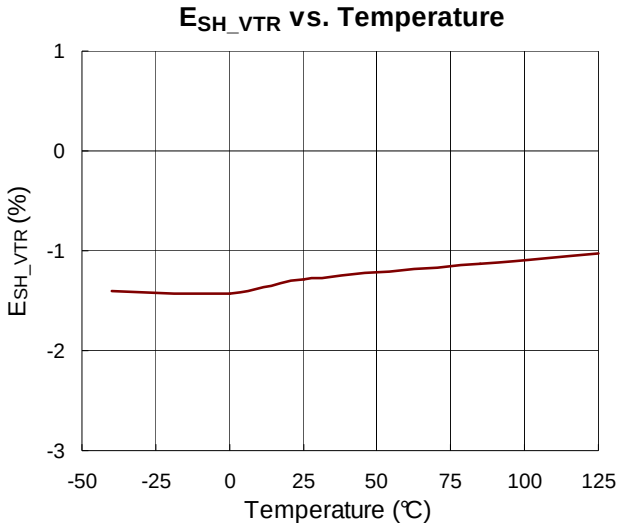


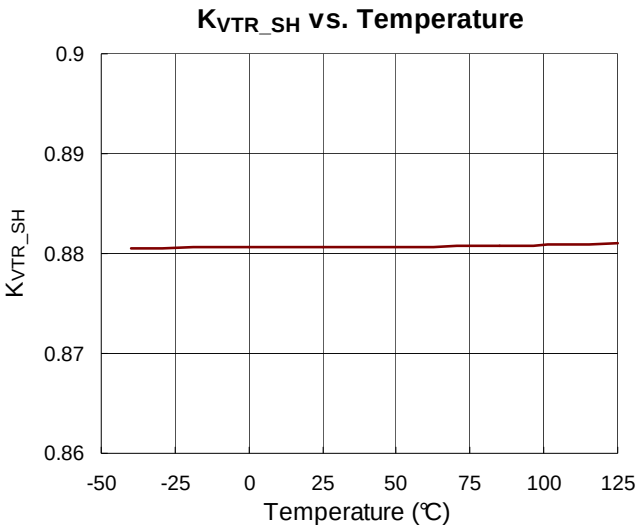


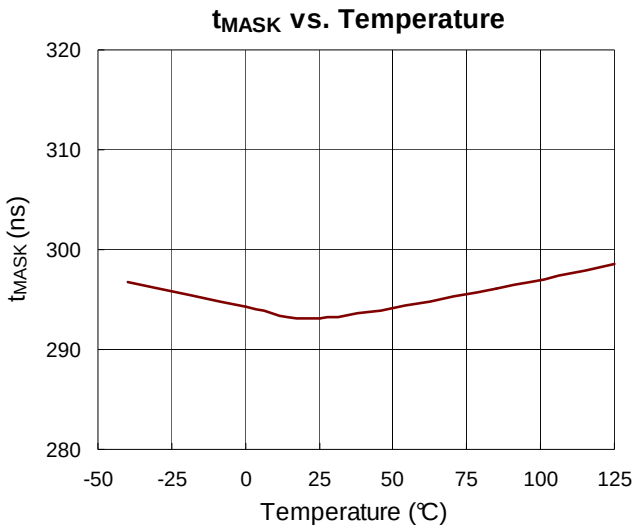


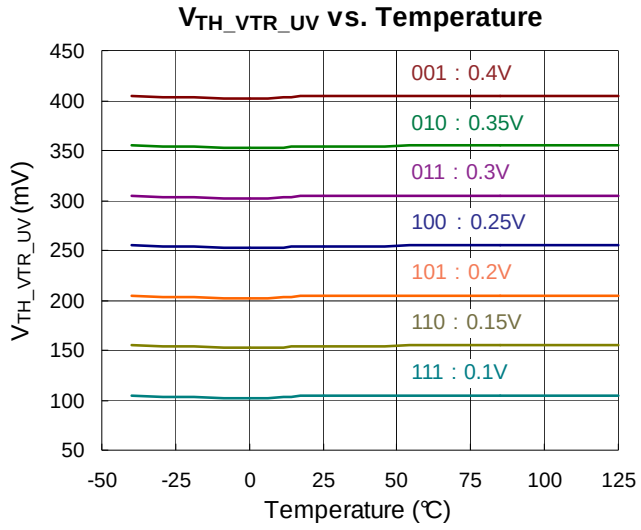
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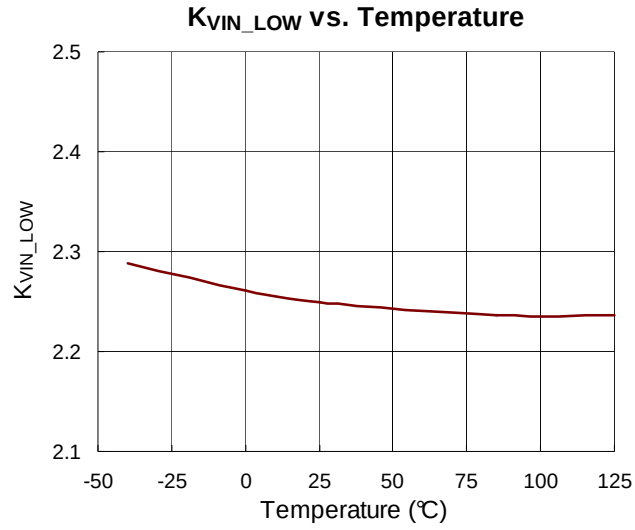




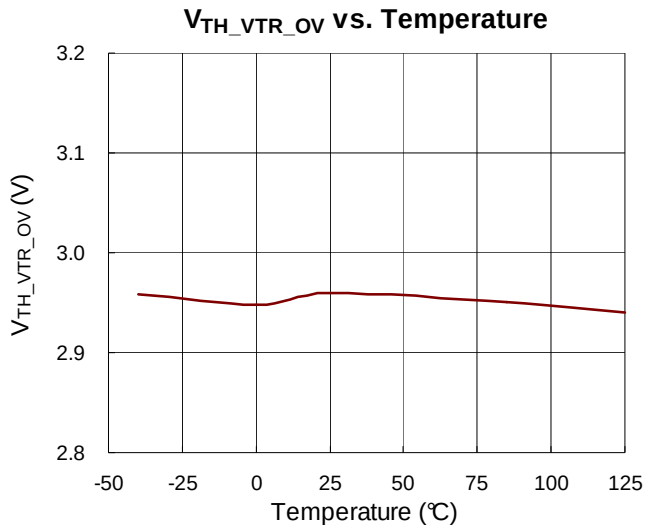


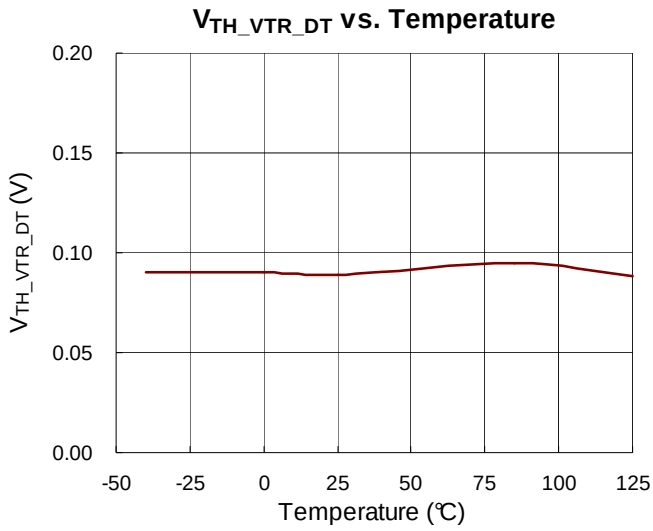


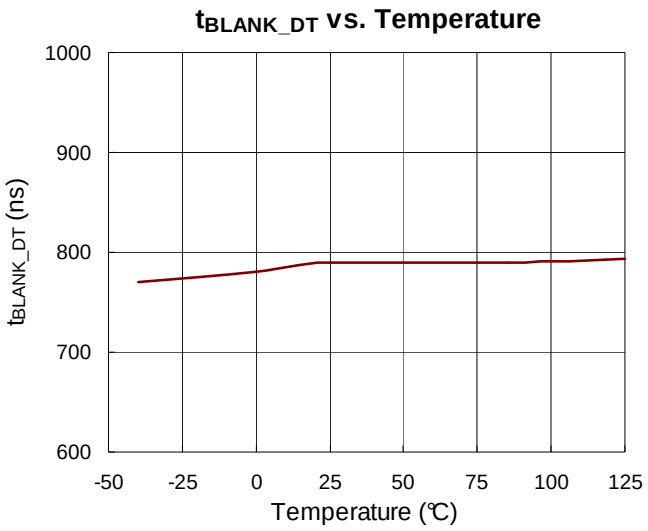


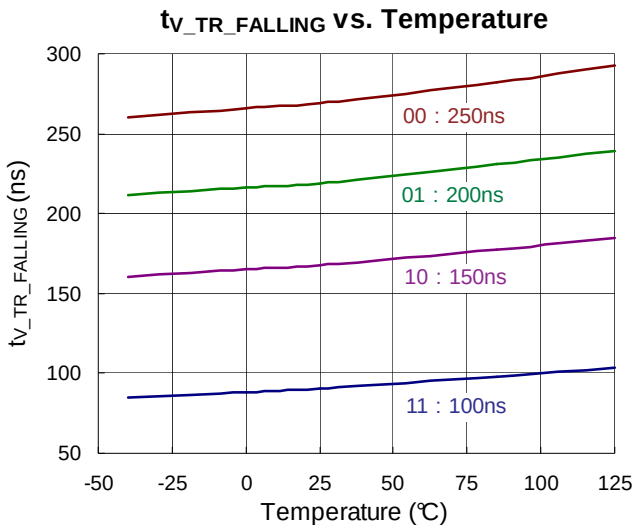


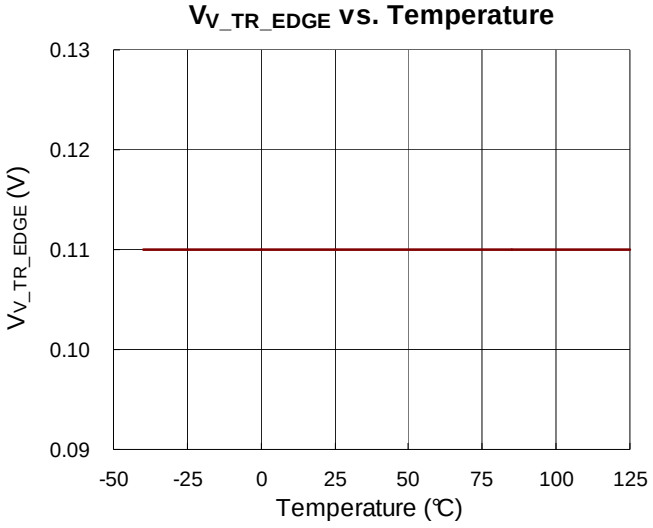
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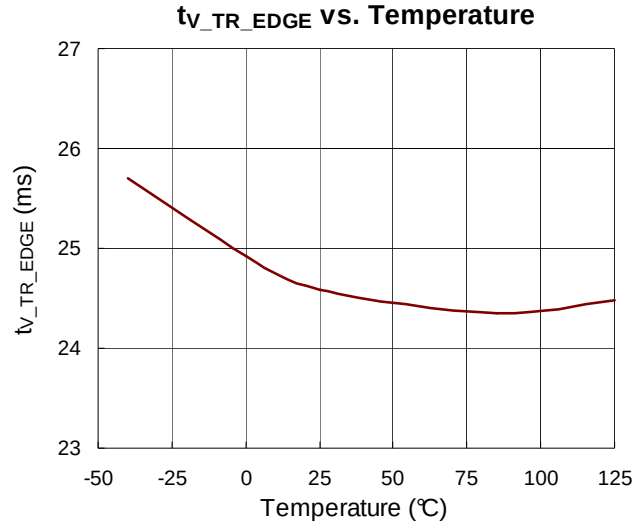




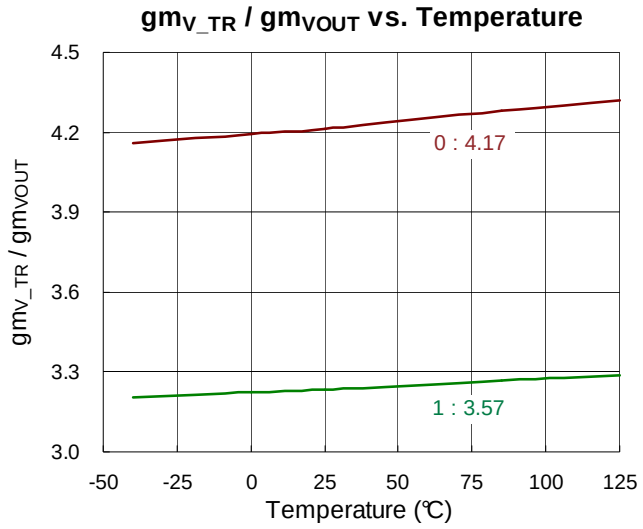


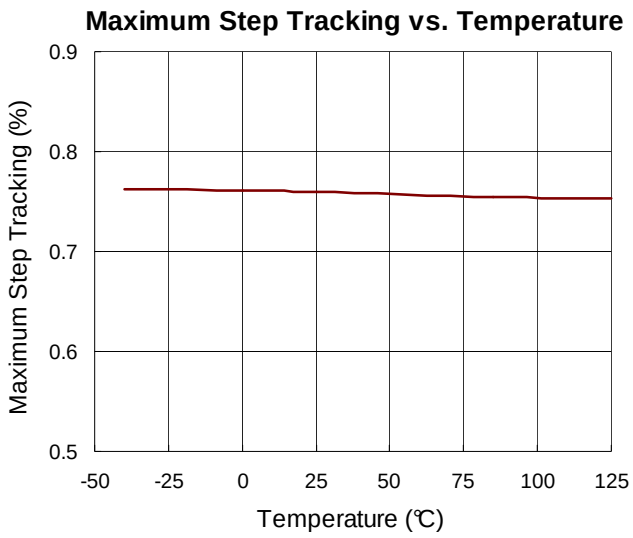






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Application Information

Constant-Voltage (CV) Loop

The RT7205A incorporates 2 error amplifiers (EA) to regulate output voltage and current, respectively. The output voltage is determined as :

$V_{OUT} = K_{VOUT} \times V_{REF_CV}$

Where

For the RT7205A, $K_{VOUT} = (R_{FB1} + R_{FB2}) / R_{FB2} = 5$ (typ)

For the RT7205AL, $K_{VOUT} = (R_{FB1} + R_{FB2}) / R_{FB2} = 2.5$ (typ)

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, and its digital counterpart, which is controlled by the MCU, as shown in Functional Block Diagram.

Constant-Current (CC) Loop and Current-Sense Amplifier

The RT7205A integrates a virtually-zero input-offset-voltage current-sense amplifier with differential-mode inputs to minimize noise interference. The amplified output current sense signal, sent to an ADC for A/D conversion, is monitored and processed by the MCU, and is also sent to the CC loop. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed by chargers' requirements.

Both the constant-voltage and constant-current compensation loops are connected together at the OPTO pin. The OPTO driver sinks current through an optocoupler and an external resistor R_D from output voltage, and the optocoupler isolates the secondary side from the primary side and also provide the feedback compensation signal for the primary side. Note that for better linearity of the loop compensation range, R_D should be designed to cover for operation at the minimum output voltage.

$$\frac{V_{OUT_MIN} - V_F - 0.3V}{R_D} \times CTR \geq I_{COMP_MAX}$$

CTR : Current transfer ratio of the optocoupler

V_F : Forward voltage of the optocoupler

0.3V : The minimum OPTO voltage for the OPTO driver to sink 2mA.

I_{COMP_MAX} : The maximum COMP sourcing current of a traditional PWM controller in the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected the COMP pin in the PWM controller.

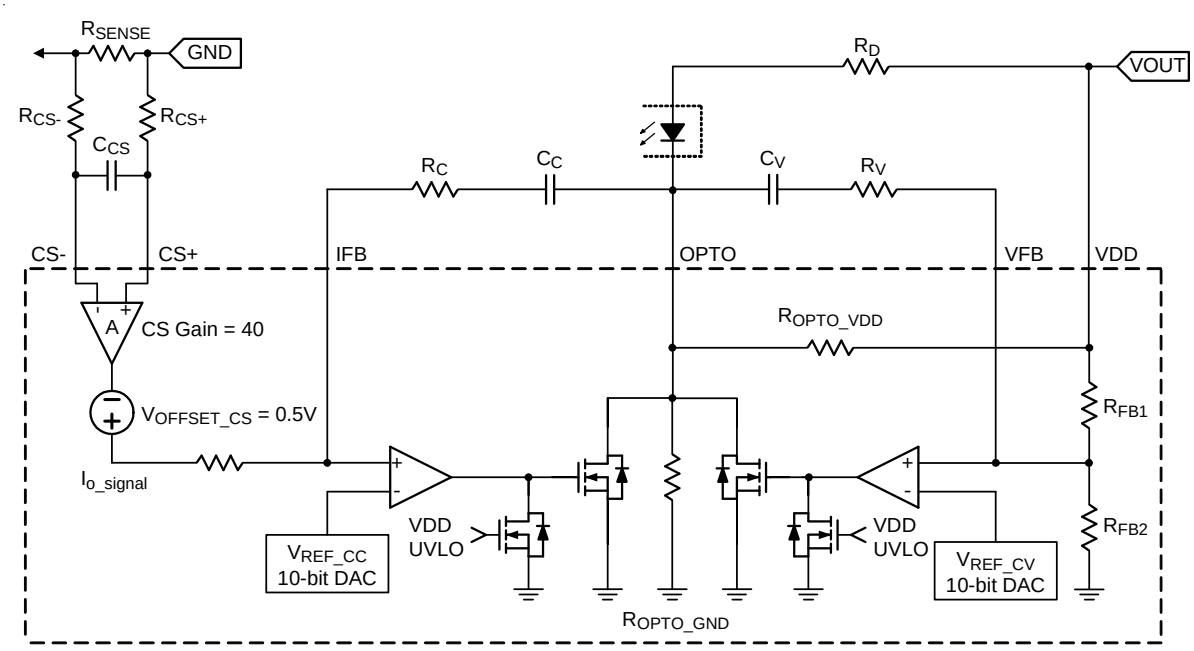


Figure 6. CV Loop and Current-Sense Amplifier

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Power-Up Sequence

Once a Type-C cable is attached, the UFP will deliver voltage and current settings to the RT7205A for the MCU to decode and to program reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, the RT7205A will enter power-saving mode, under which the RT7205A operates at ultra-low operating current and thus the total input power can be saved. If the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7205A will exit power-saving mode.

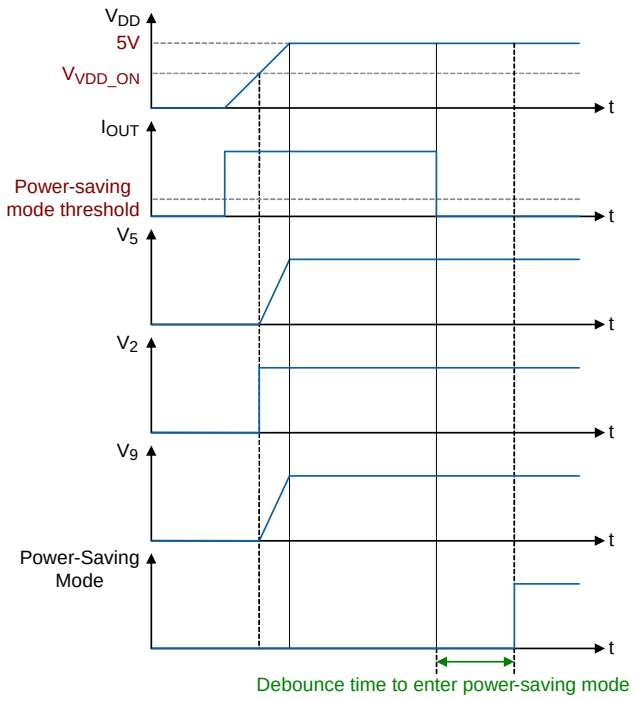


Figure 7. The Bias Voltages Sequence during Start-Up

Internal Biases and Charge Pump

The RT7205A provides three regulated bias voltages, V_5, V_2, and V_9. The V_5 bias voltage is the output of a linear regulator powered by V_{DD}, and supplies the internal analog circuit and the charge pump driver. The V_2 bias voltage is the output of a linear regulator powered by V_5, and supplies the MCU. As shown in Figure 8, the RT7205A also integrates a charge pump circuit to generate V_9 to supply for the SR driver when V_{DD} is at lower levels, such as 3V to 5V. If the RT7205A enters power-saving mode, the charge pump driver will be disabled.

The minimum source/sink capability of the charge pump driver is around 10mA at 170kHz of charge pump operating frequency f_{CP}. Bypass capacitors on the V5, V2 and V9 pins are required to minimize output ripples of the biases.

$$V_9 = V_5 \times 2 - V_{F_DCP1} - V_{F_DCP2} - I_{V9} \times R_{OUT_CP}$$

When output voltage is set at lower levels (< 5V), V_5 will be lower, following V_{DD} by a voltage drop of a dropout voltage of the LDO. For higher V_9, a lower forward voltage for the Schottky diodes, D_{CP1} and D_{CP2}, is required.

The RT7205A provides V5 short-circuit protection against the condition that the V5, V2, or VCP pin is shorted to GND, and also provides under-voltage protection for V9. If the V9 voltage is below V_{V9_SRON} (typical 4.5V), the SR driver will be turned off by firmware, that is, VG will be inactivated.

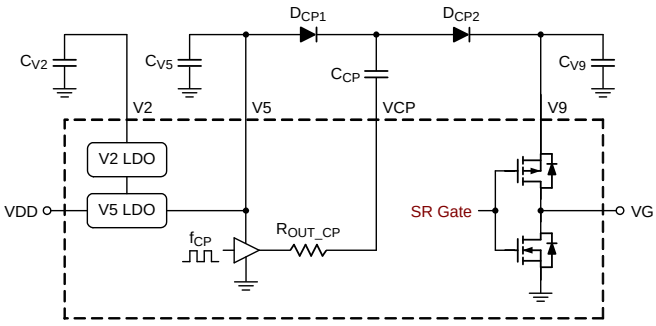
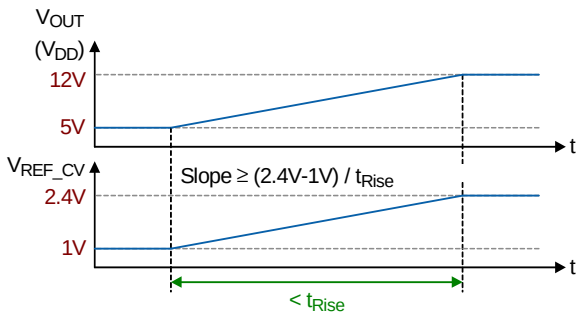


Figure 8. Charge Pump Circuit

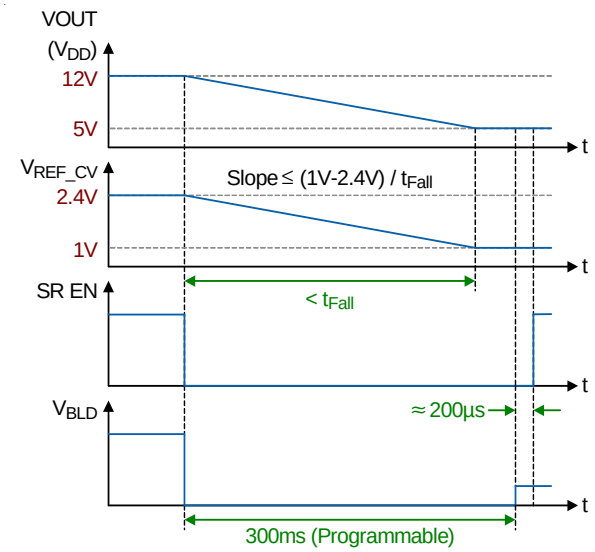
Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and fall time of output voltages should be less than define specification, as shown in Figure 9.



(a) Output Voltage Rising

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(b) Output Voltage Falling

Figure 9. Output Voltage Transient Waveforms

During the time of V_{OUT} falling, as shown in Figure 10, the BLD driver will be turned on as a dummy load to provide an extra discharging path for the output capacitor so that V_{OUT} can be settled in a shorter duration. The resistance of R_{DUMMY} can be calculated as below :

$2 \times C_{OUT} \times (R_{DUMMY} + R_{L_BLD}) < t_{Fall}$

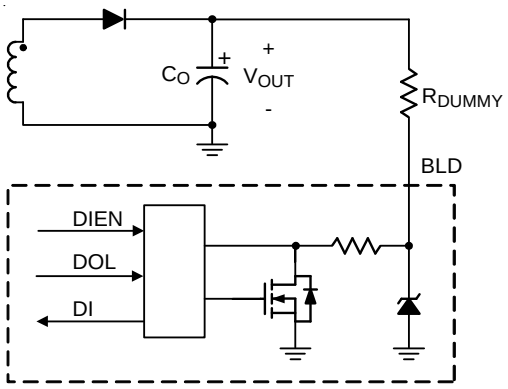


Figure 10. Application Circuit of an Active Dummy Load

During the time of V_{OUT} rising or falling, the SR driver will be turned off. After a firmware programmable delay time 300ms, the RT7205A will sense the load condition and may reactivate the SR driver.

Temperature Sensing and Thermal Protection

The RT7205A provides the RT pin for over-temperature protection or thermal monitoring. As shown in Figure 2, the RT pin sources a constant bias current for a remote thermal sensor of an NTC thermistor, connected from the RT pin to GND, for temperature sensing. If the RT voltage is below a programmable threshold voltage and the condition sustains for a programmable deglitch time, over-temperature protection will be triggered.

The bias current through the RT pin can be programmed as 100µA, 20µA, or 4µA by setting the internal register. With the appropriate bias current setting, linearity of temperature sensing over the temperature range of 25°C to 100°C can be improved. The RT7205A can deliver the sensed RT voltage data back to the UFP via the protocol (Vendor Defined Message), if necessary. Figure 11 shows the RT voltages vary with temperature at three different bias currents with an NTC thermistor TTC104 as an example.

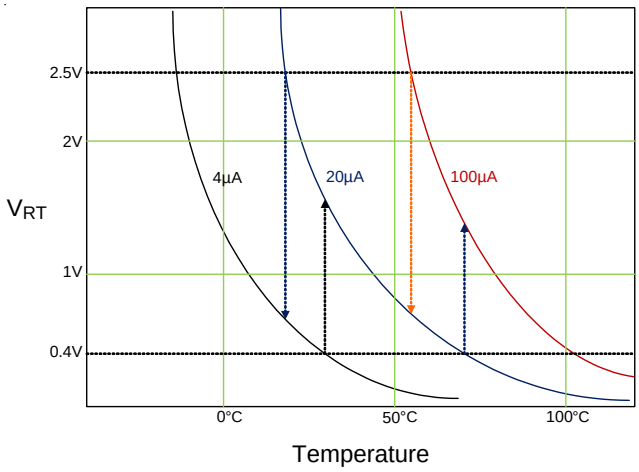


Figure 11. The RT Voltages vs. Temperature at Three Bias Currents

Blocking N-MOSFET Control (USBP)

RT7205A provides a push-pull driver for controlling external blocking N-MOSFET as shown in the Figure 12. The push-pull driver not only can control N-MOSFET smooth turn-on to avoid VOUT drops in the capacitive load condition but also provide quickly turn-off in any fault condition.

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Once the communication is set up with an UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector of the UFP is detected, the N-MOSFET will be turned on. If V_{OUT} over-voltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged by the V_{OUT} over-voltage condition. If V_{OUT} is shorted to GND, the N-MOSFET will also be turned off automatically so that output power can be limited.

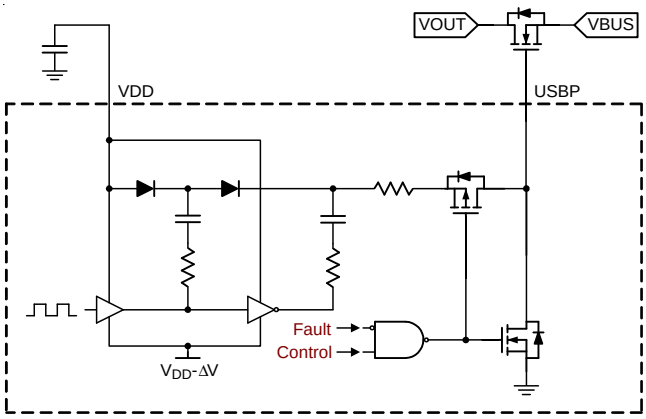


Figure 12. Blocking N-MOSFET Control

Output Over-Voltage Protection

As shown in the Figure 13 and Figure 14, the RT7205A provides the OVP pin as a backup V_{OUT} over-voltage protection, in case the optocoupler of the feedback loop is malfunction due to aging. If the internal voltage related to VDD is higher by the programmable threshold V_{VOUT_OVP}, the OVP pin will be pulled low. The OVP pin voltage will be latched low until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

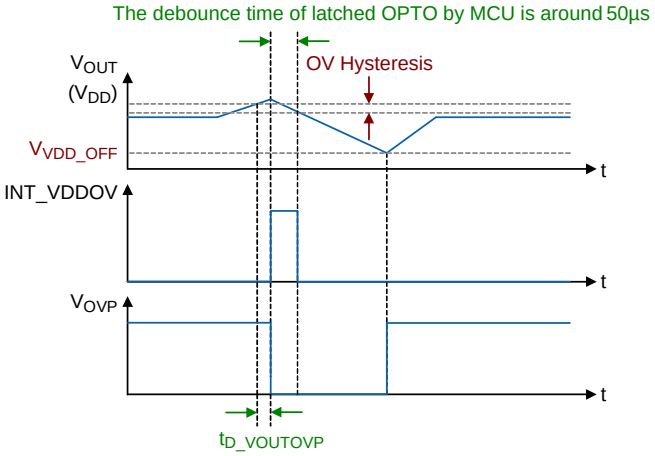


Figure 13. Timing Sequence of the OVP Function

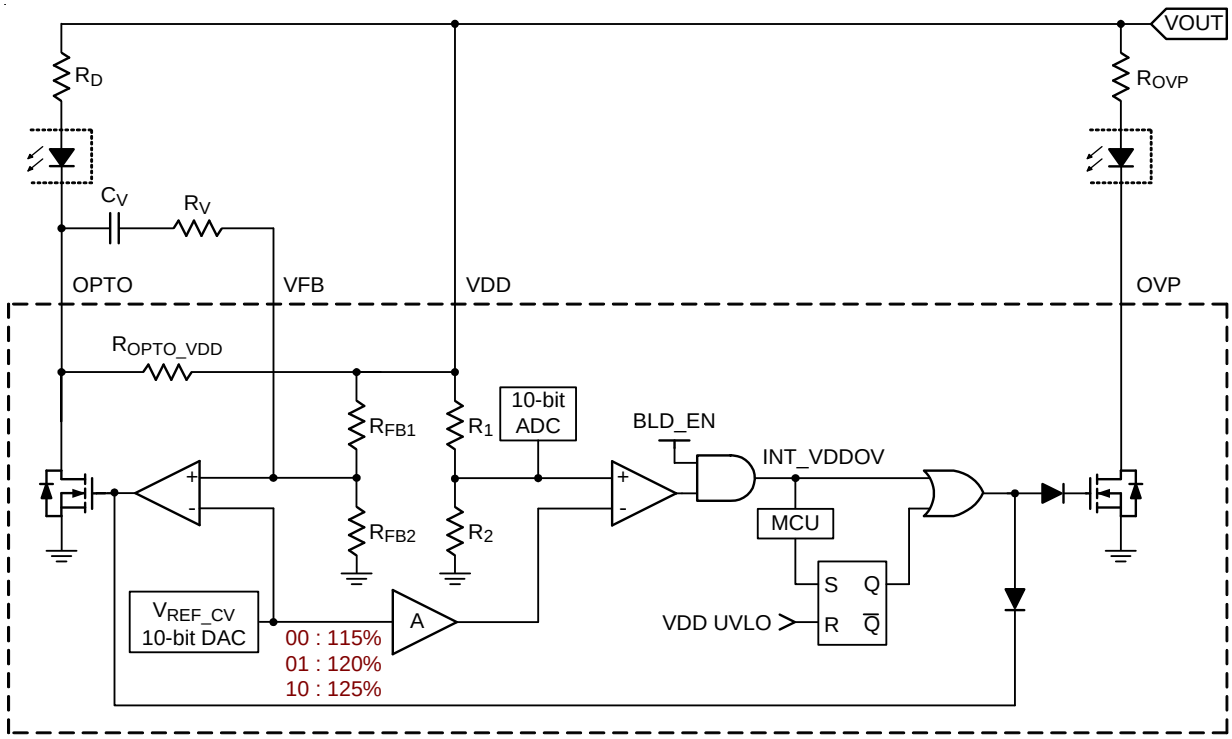


Figure 14. OVP Pin Block Diagram

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Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 14 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

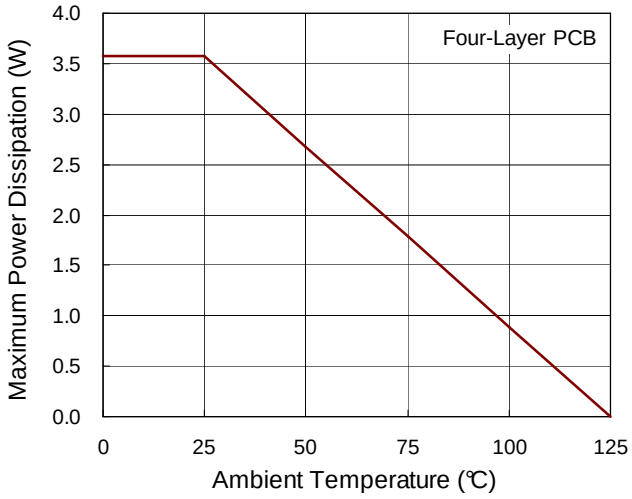
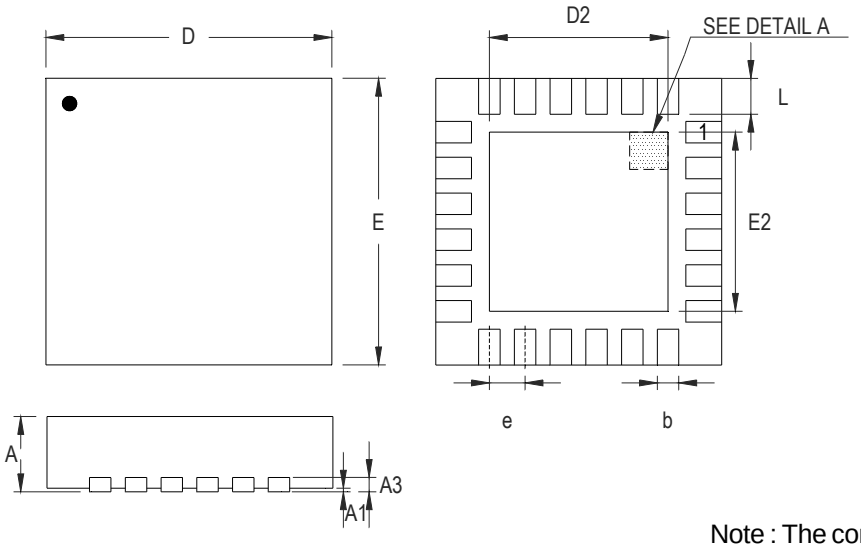
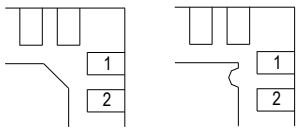


Figure 14. Derating Curve of Maximum Power Dissipation

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

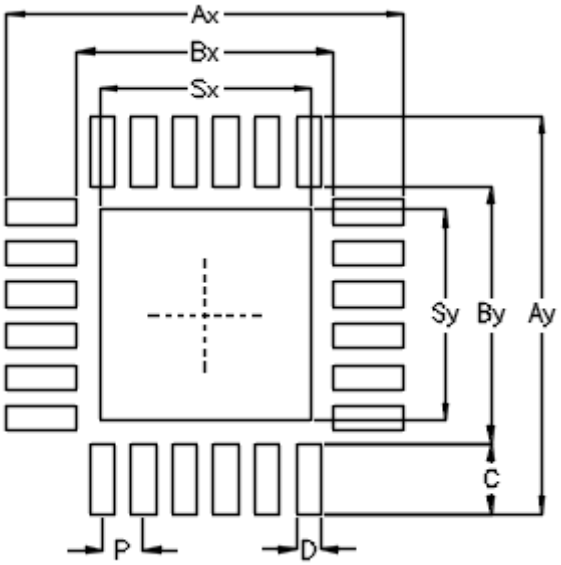
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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