

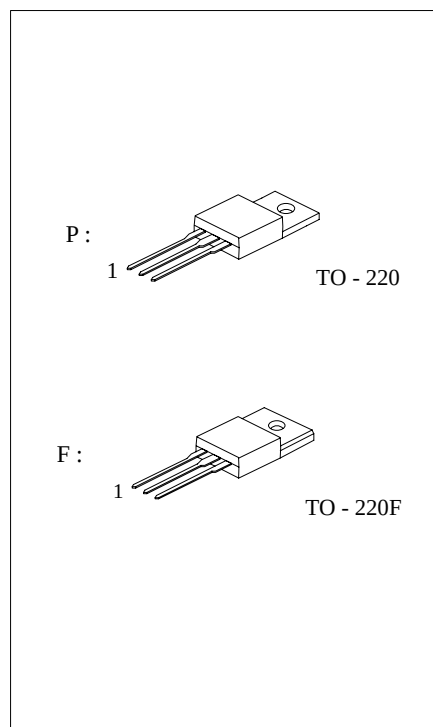
6.0A, 400V, 1.0Ω

N-CHANNEL POWER MOSFET

DESCRIPTION

- IRF730 is 400V High voltage N-Channel enhancement mode power MOS-FET chip fabricated in advanced silicon epitaxial planar technology;
- Advanced termination scheme to provide enhanced voltage-blocking capability;
- Avalanche Energy Specified;
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode;
- IRF730 product is widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

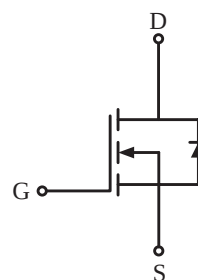
Power MOS FET



FEATURES

- * 6.0A, 400V, $R_{DS(ON)}=1.0\Omega$
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL



ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
IRF730	TO-220	G	D	S	Tube
IRF730F	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (T _J = 25°C ~ 125°C)		V _{DS}	400	V
Drain to Gate Voltage (R _{GS} = 20kΩ) (T _J = 25°C ~ 125°C)		V _{DGR}	400	V
Gate to Source Voltage		I _{GS}	±20	V
Drain Current	Continuous	I _D	5.5	A
	T _C = 100°C	I _D	3.5	A
	Pulsed	I _{DM}	22	A
Maximum Power Dissipation Derating above 25°C		P _D	74	W
			0.6	W/°C
Single Pulse Avalanche Energy Rating (V _{DD} =50V, starting T _J =25°C, L=16mH, R _G =25Ω, peak I _{AS} = 5.5A)		E _{AS}	290	mJ
Junction Temperature		T _J	-55~ +150	°C
Storage Temperature		T _{STG}	-55~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ _{JA}	62	°C / W
Thermal Resistance Junction-Case	θ _{Jc}	1.7	

■ ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V	400			V
Gate to Threshold Voltage	V _{GS(THR)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V	5.5			A
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			25	μA
		V _{DS} = 0.8 × Rated BV _{DSS} , V _{GS} = 0V, T _J = 125°C			250	μA
Gate to Source Leakage Current	I _{GSS}	V _{DS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	R _{DS(ON)}	I _D = 3.3A, V _{GS} = 10V		0.85	1.0	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} ≥ 10V, I _D = 3.3A	2.9	4.4		S
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 200V, I _D ≈ 3.5A, R _{GS} = 12Ω, R _L = 57Ω MOSFET Switching Times are Essentially Independent of Operating Temperature		10		ns
Rise Time	t _r			15		ns
Turn-Off Delay Time	t _{DLY(OFF)}			38		ns
Fall Time	t _f			14		ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{G(TOT)}	V _{GS} = 10V, I _D = 3.5A, V _{DS} = 0.8 × Rated BV _{DSS} I _{G(REF)} = 1.5mA			38	nC
Gate to Source Charge	Q _{GS}	Gate Charge is Essentially Independent of Operating Temperature			5.7	nC
Gate to Drain "Miller" Charge	Q _{GD}				22	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		700		pF
Output Capacitance	C _{OSS}			170		pF
Reverse - Transfer Capacitance	C _{RSS}			64		pF



■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 5.5\text{A}$, $V_{GS} = 0\text{V}$			1.6	V
Continuous Source to Drain Current	I_S				5.5	A
Pulse Source to Drain Current(Note 2)	I_{SM}				22	A
Reverse Recovery Time	t_{RR}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 3.5\text{A}$, $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$		270		ns
Reverse Recovery Charge	Q_{RR}			1.8		μC

Note:

1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
2. Repetitive rating: Pulse width limited by maximum junction temperature.

■ TEST CIRCUITS AND WAVEFORMS

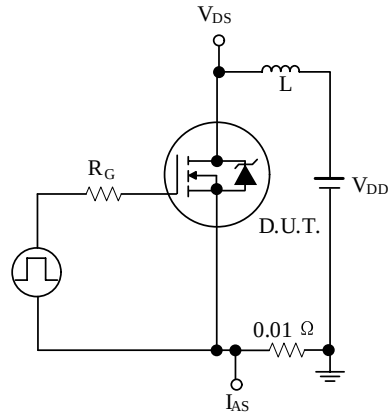


Figure 1A. Unclamped Energy Test Circuit

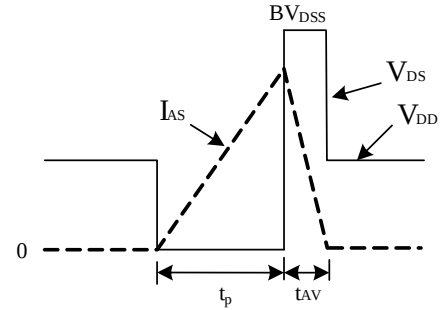


Figure 1B. Unclamped Energy Waveforms

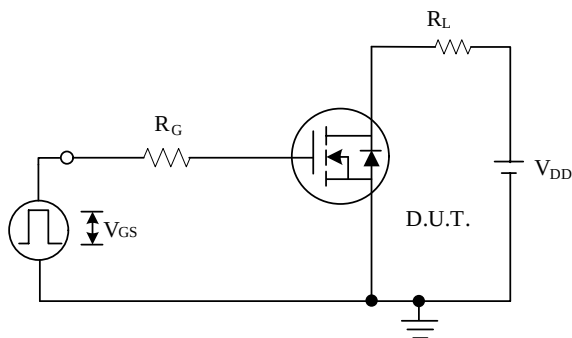


Figure 2A. Switching Time Test Circuit

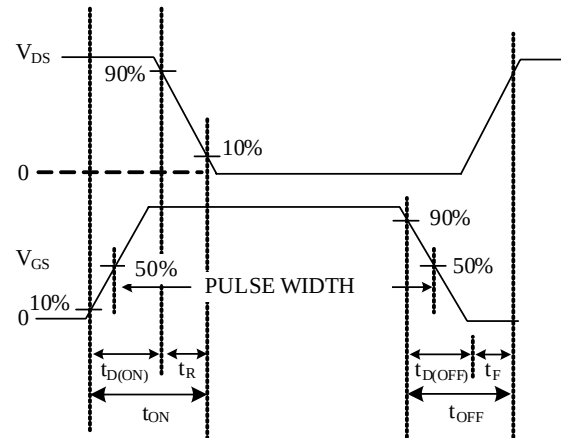


Figure 2B. Resistive Switching Waveforms

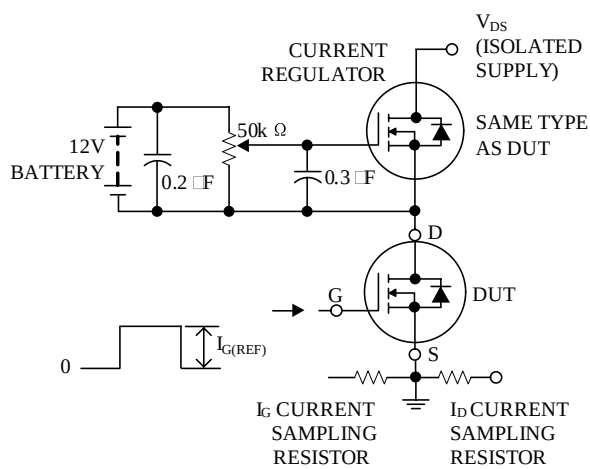


Figure 3A. Gate Charge Test Circuit

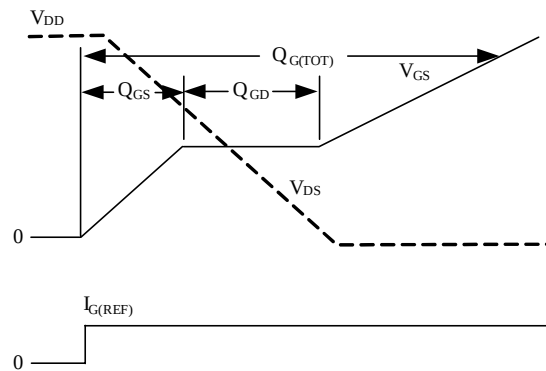
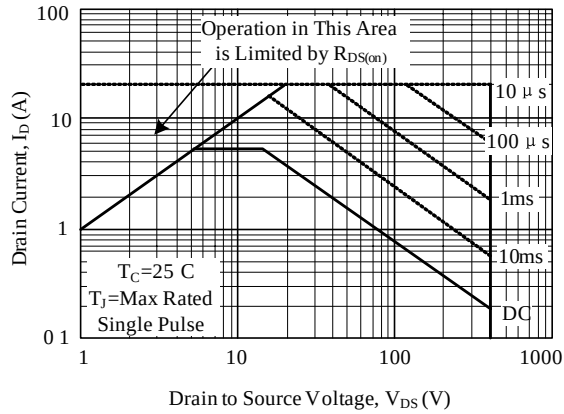


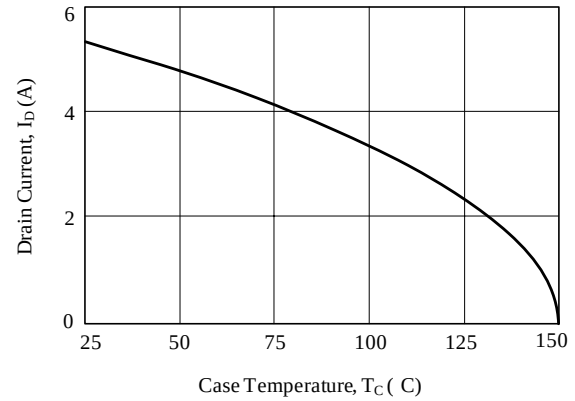
Figure 3B. Gate Charge Waveforms

■ TYPICAL PERFORMANCE CUVES (Unless Otherwise Specified)

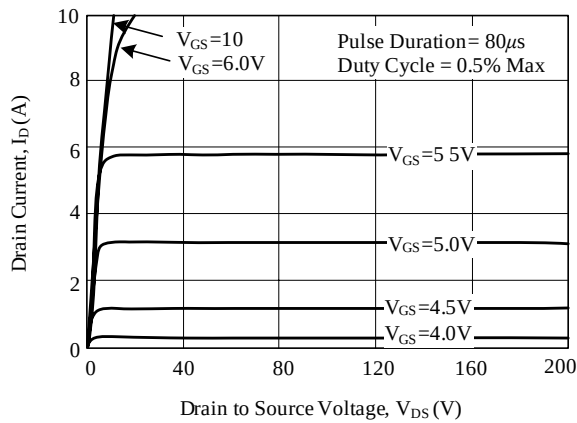
Forward Bias Safe Operating Area



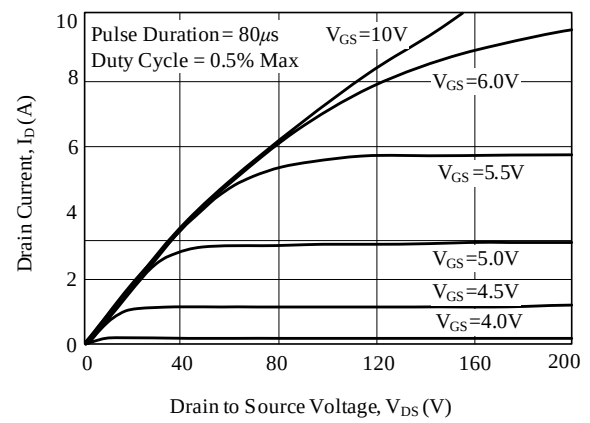
Maximum Contionuous Drain Current vs. Case Temperature



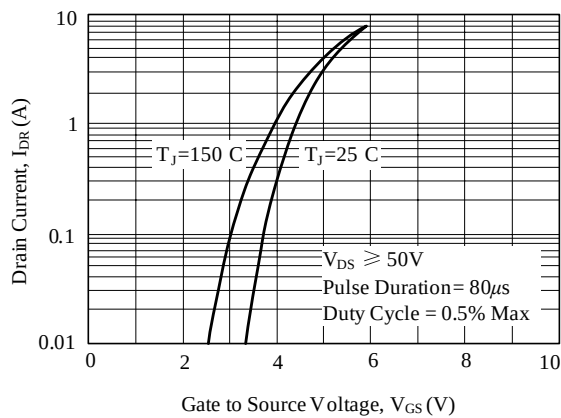
Output Characteristics



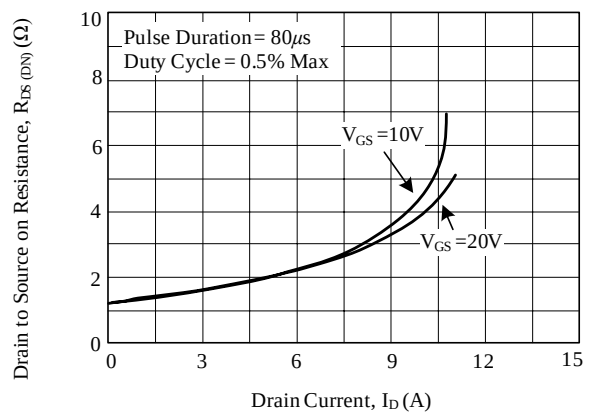
Sturation Characteristics



Transfer Characteristics

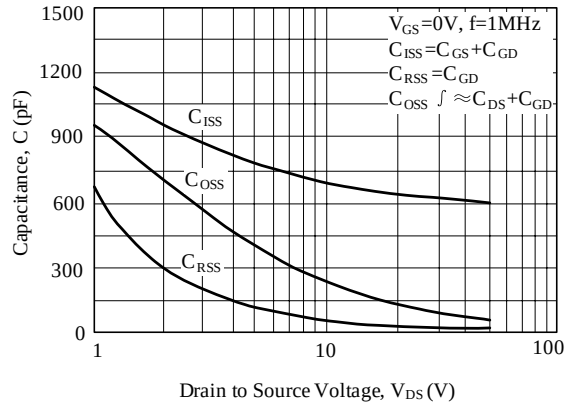


Drain to Source on Resistance vs. Gate Voltage and Drain Current

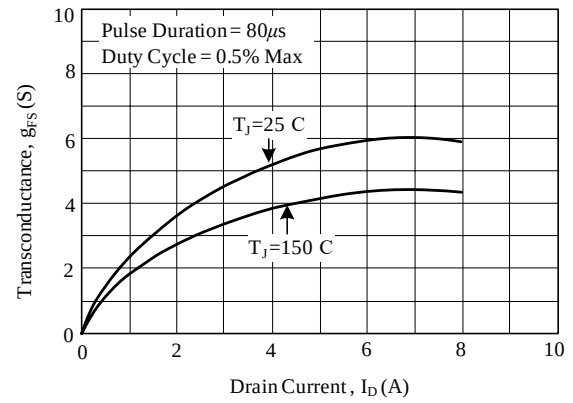


■ TYPICAL PERFORMANCE CUVES

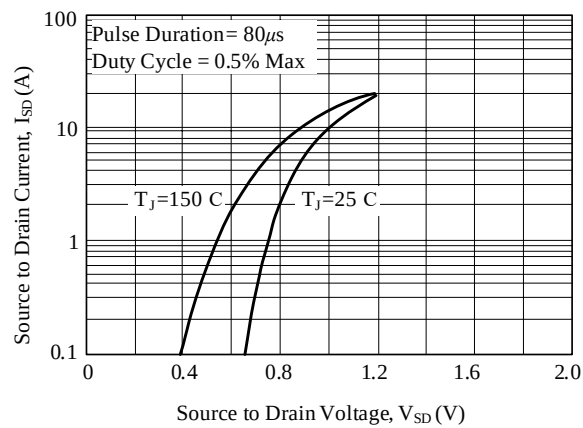
Capacitance vs. Drain to Source Voltage



Transconductance vs. Drain Current



Source to Drain Diode Voltage



Gate to Source Voltage vs. Gate Charge

