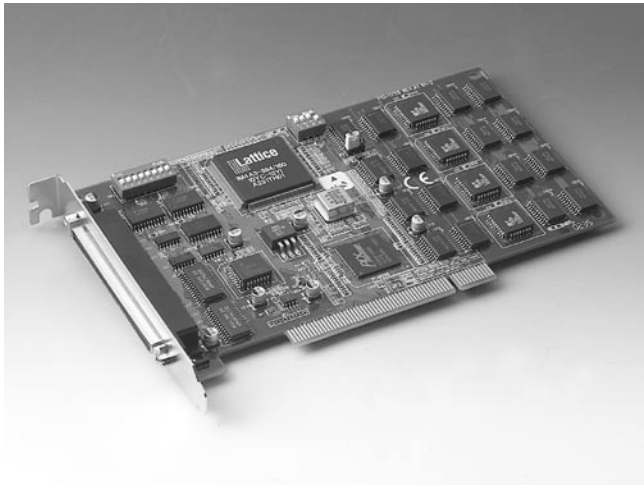


PCI-1755

80 MB/s, 32-ch Digital I/O PCI Card



FCC CE

Features

- Bus-mastering DMA data transfer with scatter gather technology
- 32/16/8-bit Pattern I/O with start and stop trigger function, 2 modes Handshaking I/O Interrupt handling capability
- Onboard active terminators for high speed and long distance transfer
- Pattern match and Change state detection interrupt function
- General-purpose 8-ch DI/O

Introduction

The PCI-1755 supports PCI-bus mastering DMA for high-speed data transfer. By setting aside a block of memory in the PC, the PCI-1755 performs bus-mastering data transfers without CPU intervention, setting the CPU free to perform other more urgent tasks such as data analysis and graphic manipulation. The function allows users to run all I/O unctons simultaneously at full speed without losing data.

Specifications

| | | | |
|----------------------------------|---|--|---|
| Channels | 32 TTL compatible | | |
| Number of Ports | Port A, Port B, Port C and Port D (8 bits/port) | | |
| I/O Configuration | 32DI (PA ~ PD) (default); 32DO (PA ~ PD); 16DI (PA ~ PB) & 16DO (PC ~ PD); 8DI (PA) & 8DO (PC) (Programmable) | | |
| Onboard FIFO | 16 KB for DI & 16 KB DO channels | | |
| Transfer Characteristics | Data Transfer Mode | Bus Mastering DMA with Scatter-Gather | |
| | Data Transfer Bus Width | 8/16/32 bits (programmable) | |
| | Max. Transfer Rate | DI: 80 M bytes/sec, 32-bit @ 20 MHz 120 M bytes/sec, 32-bit @ 40 MHz external pacer when data length is less than FIFO size DO: 80 MBytes/sec, 32-bit @ 20 MHz | |
| | Operation Mode | Handshaking | |
| Handshaking Mode | Direction | I/O | Samples No. Finite transfer, Continuous I/O |
| | Asynchronous | 8255 Emulation | Synchronous Burst Handshaking |
| | Clock source for Burst Handshaking | Internal: 30 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, Timer#0 for DI & Timer#1 for DO External: EXT_CLKIN for DI & EXT_CLKOUT for DO | |
| Normal Mode | Input | Data Acquisition at a predetermined rate by internal/external clock | |
| | Output | Waveform Generation at a predetermined rate by internal/external clock | |
| | Clock Source for DI | Internal: 30 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, Timer#0 External: EXT_CLKIN | |
| | Clock Source for DO | Internal: 30 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, Timer#1 External: EXT_CLKOUT | |
| | Start Mode | Software command/Trigger signal occurred from DI_STR or DO_STR/Pattern DI | |
| | Stop Mode | Software command/Trigger signal occurred from DI_STP (for DI) or DO_STR (for DO)/Pattern DI/Finite transfers | |
| Chang Detection (DI only) | Monitor the selected input channel and capture data whenever there is a transition on one of the channels, and then issue a IRQ | | |
| | Clock Source for DI | Internal: 30 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, Timer#0 External: EXT_CLKIN | |
| | Start Mode | Software command/Trigger signal occurred from DI_STP/Pattern DI | |
| | Stop Mode | Software command/Trigger signal occurred from DI_STP/Pattern DI/Finite transfers | |
| Trigger Capability | DI trigger signal | DI_STR, DI_STP | DO trigger signal DO_STR, DO_STP |
| | Low | 0.8 V max. | High 2.0 V min. |
| | Trigger Type | Rising or falling edge, or digital pattern (for DI only) | |
| | Pulse width for edge triggers | 10 ns min. | |
| | Pattern trigger detection capabilities | Detect pattern match or mismatch on user-selected data lines | |
| Terminator | Onboard Schottky diode termination | | |
| Messaging | The messages can be generated when 1. A specified number of bytes have been transferred, 2. When a specified input pattern is matched, 3. When a measurement operation completes. | | |
| Input Voltage | Low | 0 V min.; 0.8 V max. | High 2.0 V min.; 5 V max. |

| | | | |
|-----------------------------|--|------------------------------------|-----------------------------------|
| Input Load | Terminator OFF: TTL compatible | | |
| | Low | +0.5 V @ ±20 mA | High +2.7 V @ ±1 mA max. |
| | Terminator ON | | |
| | Terminator Resistor | 110 Ω | Termination Voltage 2.9 V |
| Output Voltage | Low | +0.5 V @ ±22.4 mA | High +2.7 V @ ±1 mA max. |
| | High | 2.7 V min. | |
| Driving Capacity | Low | 0.5 V max. @ +48 mA (sink) | High 2.4 V min. @ -15 mA (source) |
| | High | +4.65 ~ +5.25 V _{cc} @ 1A | |
| Hysteresis | 500 mV | Power Available at I/O connector | |
| | +4.65 ~ +5.25 V _{cc} @ 1A | | |
| General-purpose DI/O | DI Channels | DI0 ~ DI7 (TTL compatible) | |
| | DO Channels | DO0 ~ DO7 (TTL compatible) | |
| Interrupt Source | DI0 ~ 7 and Timer#2, Pattern match and Change detection, DI FIFO overflow and DO FIFO underflow, DI_STP and DO_STP | | |

Pacer

- **Channels** Timer#0, Timer#1 and Timer#2
- **Timer#0** Timer pacer for digital input
- **Timer#1** Timer pacer for digital output
- **Timer#2** Interrupt source
- **Resolution** 16-bit
- **Base Clock** 10 MHz

General

| | | | |
|---------------------------|---|----------------------------|-----------------------------------|
| I/O Connector Type | 100-pin SCSI-II female | | |
| Dimensions (L x H) | 175 x 100 mm (6.9" x 3.9") | | |
| Power Consumption | Typical | Terminator OFF: +5 V @ 1 A | Max. Terminator OFF: +5 V @ 1 A |
| | | Terminator ON: +5 V @ 1 A | |
| Temperature | Operating | 0 ~ 60° C (32 ~ 140° F) | Storage -20 ~ 85° C (-4 ~ 185° F) |
| | | (refer to IEC 68-2-1, 2) | |
| Relative Humidity | 5 ~ 95% RH non-condensing (refer to IEC 68-2-3) | Cert. | FCC, CE certified |

Ordering Information

- **PCI-1755** Ultra-speed 32-ch Digital I/O Card
- **ADAM-39100** PCI-1755 Wiring Terminal for DIN-rail Mounting
- **PCL-101100-1** 100-pin SCSI-II cable with male connectors on both ends and special shielding for noise reduction, 1 m