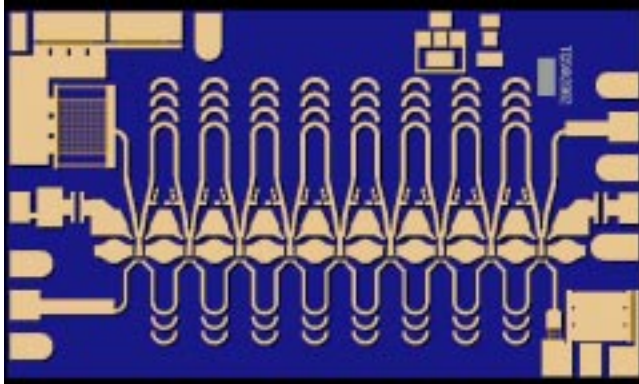


12.5Gb/s Modulator Driver Amplifier
Metro and Long Haul Applications

TGA4802-EPU



Key Features and Performance

- Frequency Range: DC - 25 GHz
- Single-ended Input / Output
- 15 dB Small Signal Gain
- 18 GHz Small Signal Bandwidth
- Wide Drive Range (3V to 7V)
- 15ps Edge Rates (20/80)
- Power Dissipation 1.2 Watts
- 0.25um pHEMT 2MI Technology
- Die Size: 3.3 x 2.0 x 0.1 mm
 (0.131 x 0.79 x 0.004 inches)

Description

The TriQuint TGA4802 is part of a series of optical driver amplifiers suitable for a variety of driver applications.

The TGA4802 is a medium power wideband AGC amplifier MMIC die that typically provides 15dB small signal gain with 10dB AGC range. RF ports are DC coupled enabling the user to customize system corner frequencies.

The TGA4802 is an excellent choice for 12.5Gb/s optical modulator driver applications. The TGA4802 has demonstrated capability to amplify a 2V input signal to 7Vpp saturated.

The TGA4802 requires off-chip decoupling, a DC block and a bias tee. The TGA4802 is available in die form.

Primary Applications

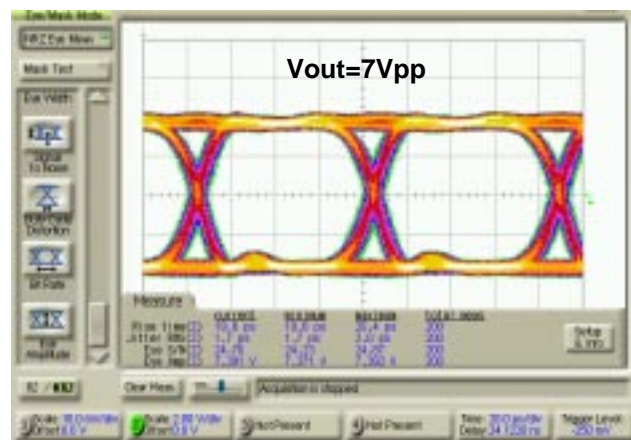
- Mach-Zehnder Modulator Driver for Metro and Long Haul

Measured Performance

TGA4802 Fixtured Data
 Vd(Rfout)=6V, Id=170mA, (Pdc=1.2W)
 Vout=7Vpp, Vin = 2Vpp
 Scale: 2V/div, 20ps/div

12.5Gb/s

Vin=2V



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V _d	POSITIVE SUPPLY VOLTAGE Drain Voltage at RF output	7 V	2/
I _d	POSITIVE SUPPLY CURRENT Drain Current	200 mA	2/
P _d	POWER DISSIPATION	1.4 W	2/, 3/
V _g I _g	NEGATIVE GATE Voltage Gate Current	0 V to -3 V 5 mA	
V _{ctrl} I _{ctrl}	CONTROL GATE Voltage Gate Current	V _d /2 to -3 V 5 mA	4/
P _{IN}	RF INPUT Sinusoidal Continuous Wave Power	23 dBm	
T _{CH}	OPERATING CHANNEL TEMPERATURE	150 °C	5/, 6/
T _M	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T _{STG}	STORAGE TEMPERATURE	-65 to 150 °C	

Notes:

- 1/ These ratings represent the maximum operable values for the device.
- 2/ Assure the combination of V_d and I_d does not exceed maximum power dissipation rating.
- 3/ Assure V_{ctrl} never exceeds V_d during bias on and off sequences, and normal operation.
- 4/ When operated at this bias condition with a base plate temperature of 70°C, the median life is reduced.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TEST
(T_A = 25 °C, nominal)

NOTES	SYMBOL	LIMITS		UNITS
		MIN	MAX	
1/	V _{BVGS}	11	30	V
1/	V _{BVGD}	11	30	V

Notes:

- 1 V_{BVGS} and V_{BVDS} are negative.

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TABLE III
RF SPECIFICATIONS

(T_A = 25°C Nominal)

Bias Conditions: V_d = 7V I_d = 170 mA

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			18		GHz
<u>1/</u>	SMALL-SIGNAL GAIN MAGNITUDE	2 - 10 GHz 12 - 18 GHz	14 10			dB
<u>1/</u>	INPUT RETURN LOSS MAGNITUDE	2 - 14 GHz		10		dB
<u>1/</u>	OUTPUT RETURN LOSS MAGNITUDE	2 - 14 GHz		12		dB
<u>2/ 3/</u>	SATURATED OUTPUT POWER	2 - 12 GHz	22			dBm
<u>2/, 3/</u>	EYE AMPLITUDE	V _d (RF _{out}) = 6V V _d (RF _{out}) = 5V V _d (RF _{out}) = 4V	7.0 6.0 5.0			V _{pp}
<u>2/, 4/</u>	ADDITIVE JITTER			5		ps
<u>2/, 4/</u>	RISE TIME (20/80)			15		ps

Notes:

1/ RF Probe Bias: V⁺ = 8 V, adjust V_{g1} to achieve I_d = 80 mA, V_{ctrl} = +1.5 V

2/ Verified by design, TGA4802 assembled onto an evaluation platform as shown on page 9 then tested using the application circuit and bias procedure detailed on pages 7 and 8.

3/ V_{in} = 2 V, Data Rate = 12.5 Gb/s, V_{ctrl} and V_g are adjusted for maximum output.

4/ Computed using RSS Method where J_{pp_additive} = SQRT(J_{pp_out}² - J_{pp_in}²)

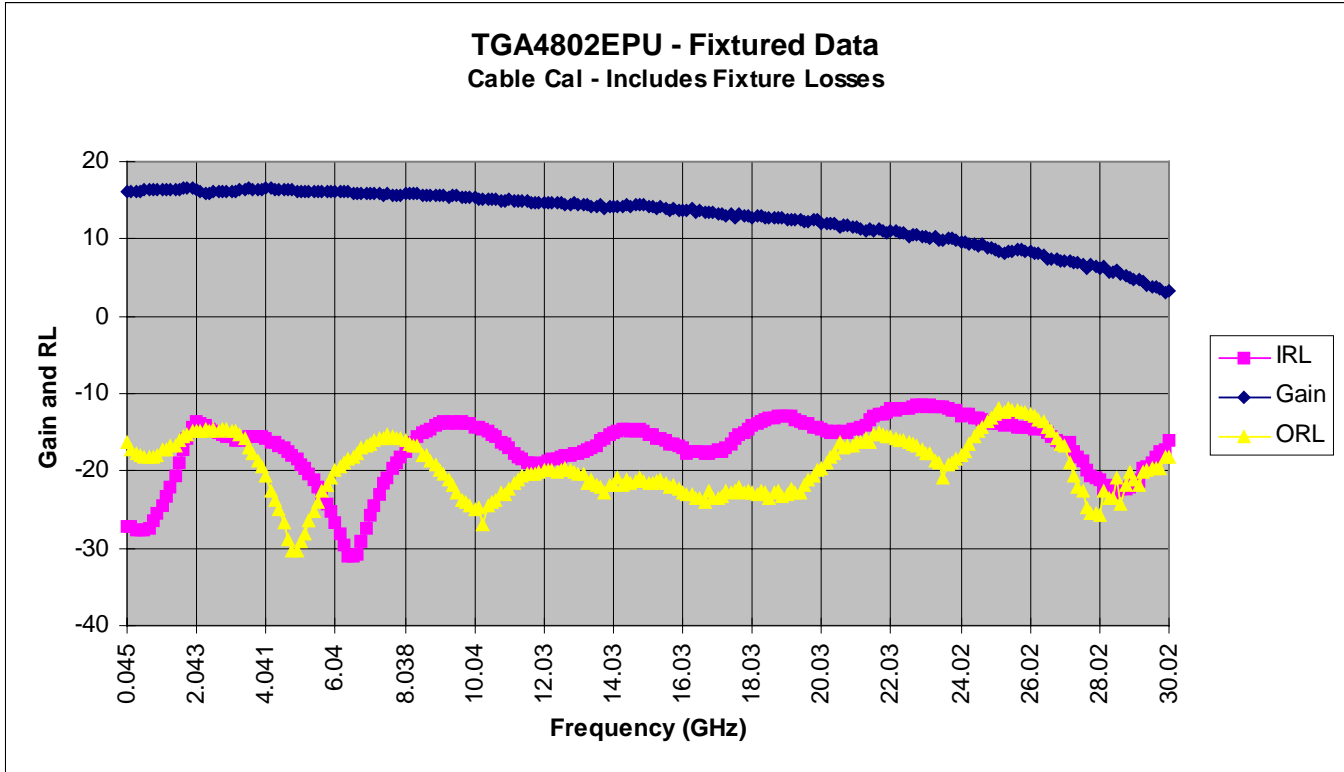
**TABLE IV
THERMAL INFORMATION***

PARAMETER	TEST CONDITIONS	T _{CH} (°C)	R _{θJC} (°C/W)	T _M (HRS)
R _{θJC} Thermal Resistance (channel to backside of carrier)	V _d (RF out) = 7 V I _D = 170 mA P _{diss} = 1.2 W	110	32.7	4.2 E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated. Thermal transfer is conducted thru the bottom of the TGA4802 into the mounting carrier. Design the mounting interface to assure adequate thermal transfer to the base plate.

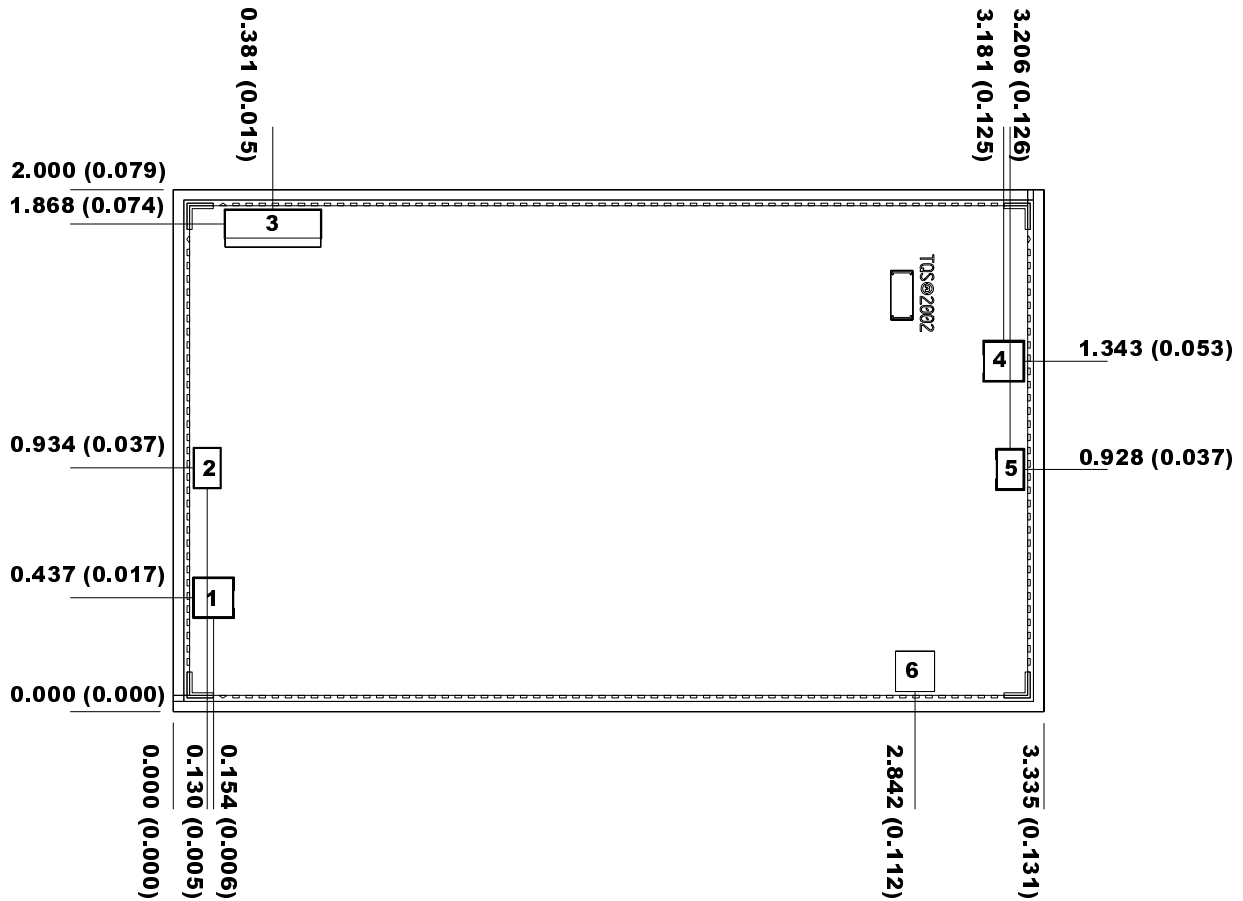
Measured Fixtured Data

Bias Conditions: $V_d = 7V$, $I_d = 170mA$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

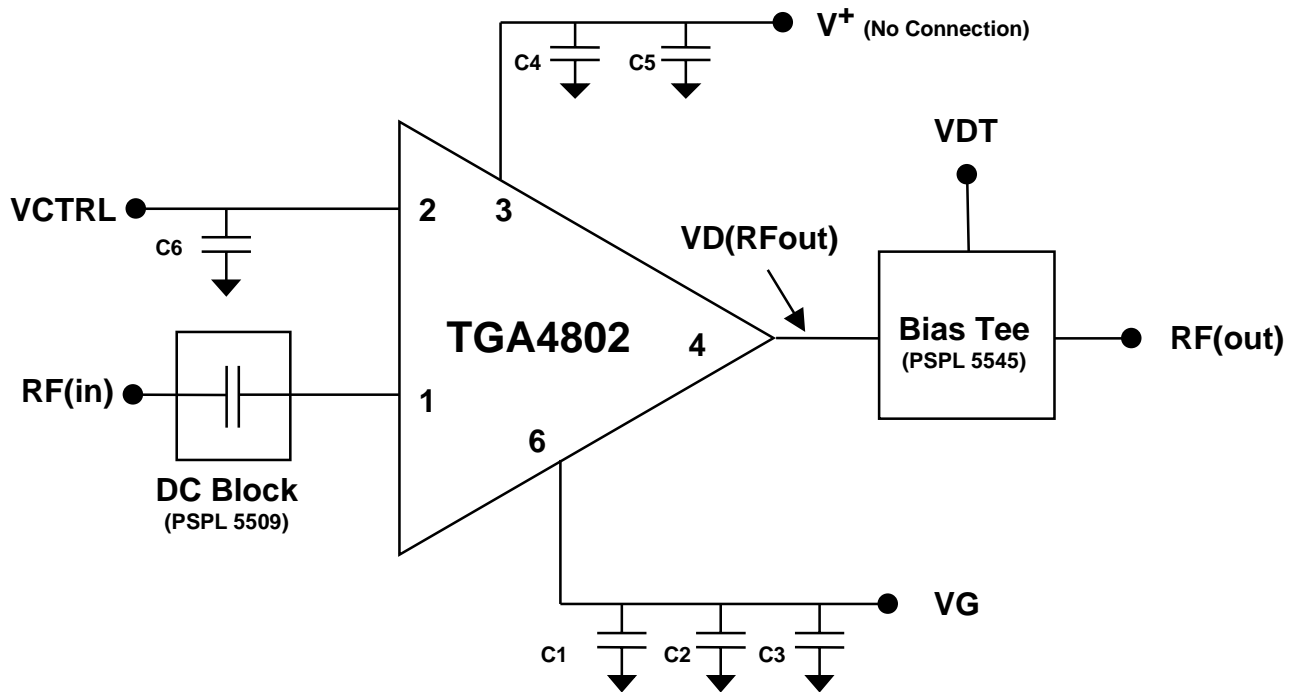
Chip size tolerance: +/- 0.051 (0.002)

Bond pad #1	(RF In)	0.150 x 0.150 (0.006 x 0.006)
Bond pad #2	(Vctrl)	0.100 x 0.150 (0.004 x 0.006)
Bond pad #3	(V+)	0.366 x 0.108 (0.014 x 0.004)
Bond pad #4	(RF Out)	0.155 x 0.155 (0.006 x 0.006)
Bond pad #5	(Vctrl aux)	0.100 x 0.150 (0.004 x 0.006)
Bond pad #6	(Vg)	0.150 x 0.150 (0.006 x 0.006)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TGA4802 Application Circuit



Notes:

Recommended Components are detailed on page 9.

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Bias Procedure for 7V Output

Bias ON

1. Disable the RF source (PPG)
2. Set $V_{dT}=0V$ $V_{ctrl}=0V$ and $V_g=0V$
3. Set $V_g=-1.5V$
4. Increase V_{dT} to 7V observing I_d .
 - Assure $I_d=0mA$
5. Set $V_{ctrl}=+1.0V$
 - I_d should still be 0mA
6. Make V_g more positive until $I_{dd}=170mA$.
 - Typical value for V_g is -0.2V
7. Measure V^+ , adjust V_{dT} such that V^+ is 6V.
 - This will set $V_d(RF_{out})$ to approximately 6V.
 - I_{dd} will increase slightly
8. Adjust V_g such that $I_{dd}=170mA$.
9. Enable the RF source (PPG)
 - Set $V_{in}=2V$
10. Output Swing Adjust: Adjust V_{ctrl} slightly positive to increase output swing or adjust V_{ctrl} slightly negative to decrease the output swing.
 - Typical value for V_{ctrl} is +1.0V for $V_o=7V$.
11. Crossover Adjust: Adjust V_g slightly positive to push the crossover down or adjust V_g slightly negative to push the crossover up.
 - Typical value for V_g is -0.2V to center crossover with $V_o=7V$.

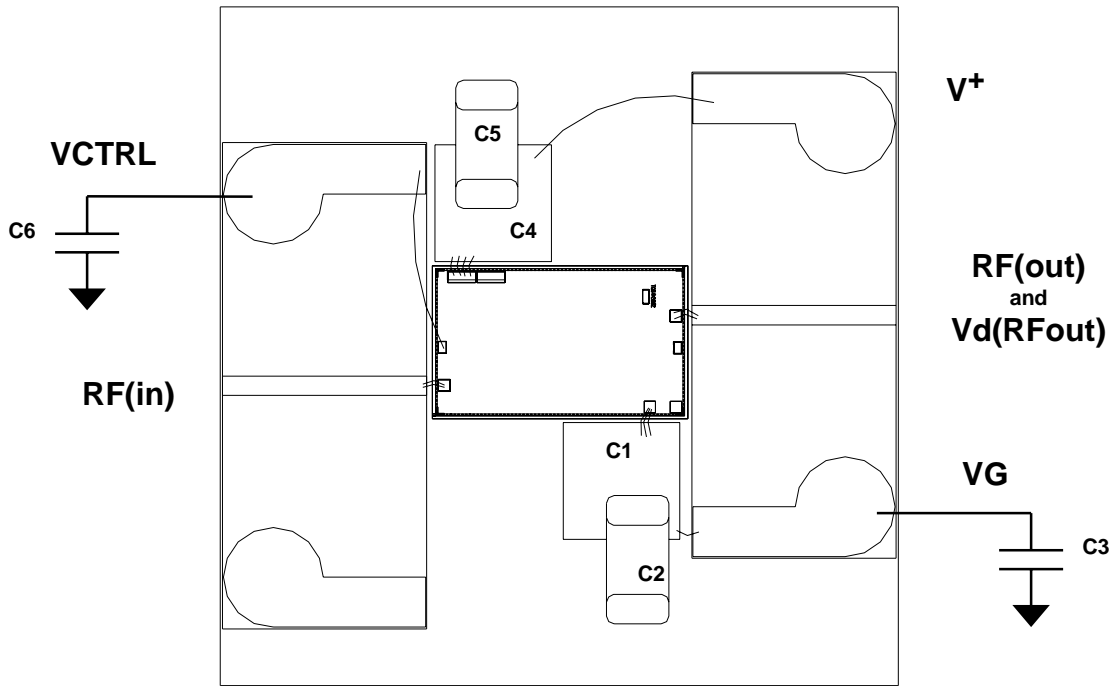
Bias OFF

1. Disable the output of the PPG
2. Set $V_{ctrl}=0V$
3. Set $V_{dT}=0V$
4. Set $V_g=0V$

Notes:

1. Assure V_{ctrl} never exceeds V_d during Bias ON and Bias OFF sequences and during normal operation.

Evaluation Platform Assembly Diagram



Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C4	1500pF Capacitor SLC	Presidio	SL5050X7R1522H5
C2, C5	0.1uF Capacitor MLC Ceramic	AVX	0603YC104KAT
C3	10uF Capacitor MLC Ceramic	AVX	0603YC102KAT
C6	0.01 uF Capacitor MLC	AVX	0603YC103KAT

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Evaluation Platform Assembly Notes

Assembly Notes:

Reflow Attachment:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- Use alloy station or conveyor furnace with reducing atmosphere
- No fluxes should be utilized
- Coefficient of thermal expansion matching is critical for long-term reliability
- Storage in dry nitrogen atmosphere

Adhesive Attachment:

- Organic attachment can be used in low-power applications
- Curing should be done in a convection oven; proper exhaust is a safety concern
- Microwave or radiant curing should not be used because of differential heating
- Coefficient of thermal expansion matching is critical

Component Pickup and Placement:

- Vacuum pencil and/or vacuum collet preferred method of pick up
- Avoidance of air bridges during placement
- Force impact critical during auto placement

Interconnect:

- Thermosonic ball bonding is the preferred interconnect technique
- Force, time, and ultrasonics are critical parameters
- Aluminum wire should not be used
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- Maximum stage temperature: 200°C