# ATA663431/ATA663454

## LIN SBC(1) including LIN Transceiver, Voltage Regulator, Window Watchdog and High-side Switch

**DATASHEET**

## Features

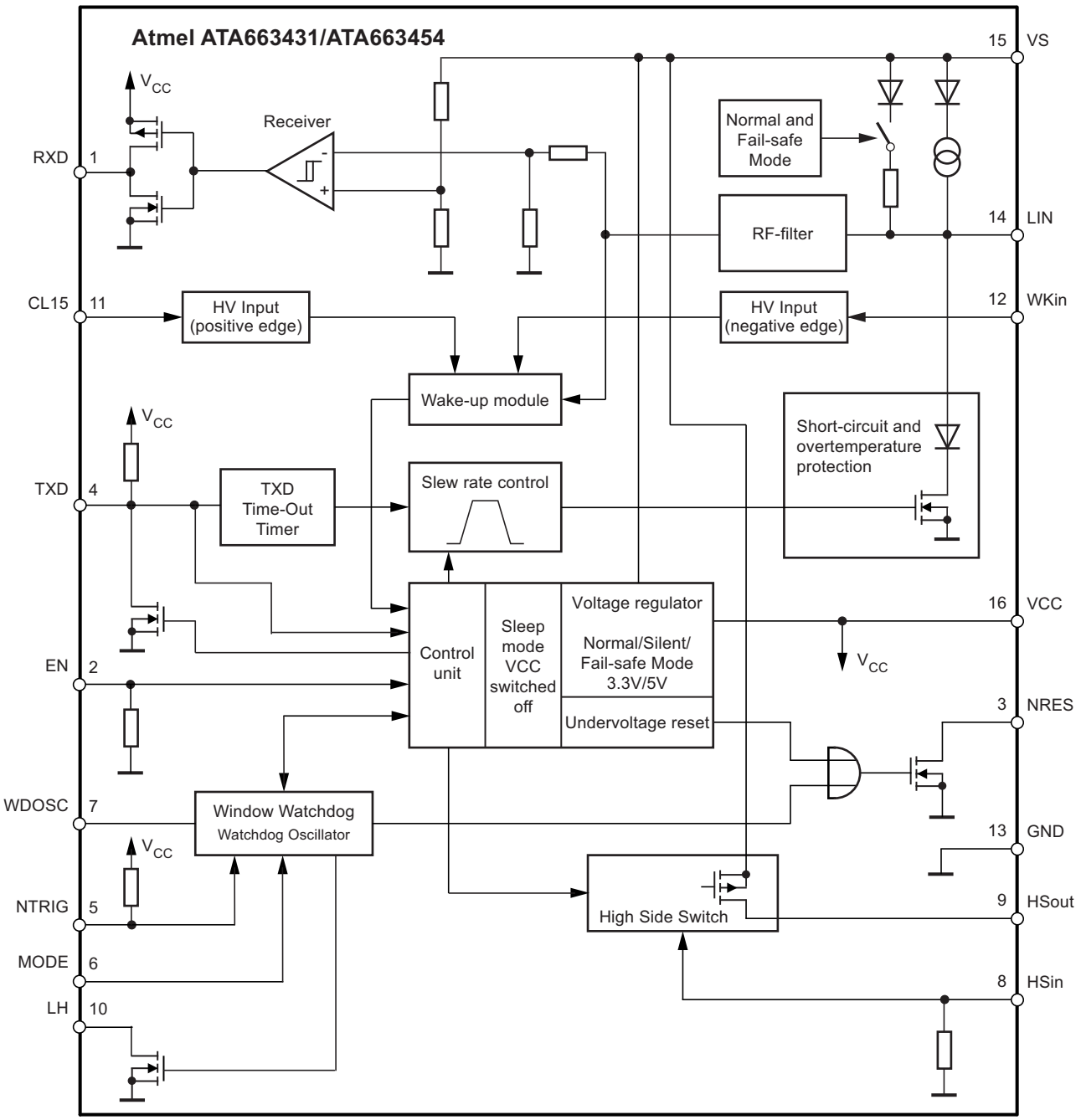
- Supply voltage up to 40V
- Operating voltage $V_{VS}$ = 5V to 28V
- Supply current
  - Sleep mode: typically 10µA
  - Silent mode: typically 47µA
  - Very low current consumption at low supply voltages (2V < $V_{VS}$ < 5.5V): typically 150µA
- Linear low-drop voltage regulator, 85mA current capability:
  - MLC (multi-layer ceramic) capacitor with 0Ω ESR
  - Normal, fail-safe, and silent mode
    - Atmel ATA663454: $V_{CC}$ = 5.0V ±2%
    - Atmel ATA663431: $V_{CC}$ = 3.3V ±2%
  - Sleep mode: VCC is switched off
- VCC undervoltage detection with open drain reset output (NRES, 4ms reset time)
- Voltage regulator is short-circuit and over-temperature protected
- Adjustable watchdog time via external resistor
- Negative trigger input for watchdog
- Limp Home watchdog failure output
- LIN physical layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Bus pin is overtemperature and short-circuit protected versus GND and battery
- High-side switch
- Wake-up capability via LIN Bus (100µs dominant), WKin pin and CL15 pin
- Wake-up source recognition
- TXD time-out timer
- Advanced EMC and ESD performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and damage protection according to ISO7637
- Qualified according to AEC-Q100
- Package: DFN16 with wettable flanks (Moisture Sensitivity Level 1)

Note: 1. LIN SBC: LIN system basis chip

# 1. Description

Designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, the Atmel® ATA663431/ATA663454 is a new generation of system basis chips with a fully integrated LIN transceiver, a low-drop voltage regulator (3.3V/5V/85mA), a window watchdog, and a high-side switch. This combination makes it possible to develop simple, but powerful, slave nodes in LIN-bus systems. Atmel ATA663431/ATA663454 is designed to handle low-speed data communication in vehicles (such as in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20Kbaud. The bus output is designed to withstand high voltage. Sleep mode and silent mode guarantee a minimized current consumption even in the case of a floating or short-circuited LIN bus.

**Figure 1-1. Block Diagram**



# 2. Pin Configuration

**Figure 2-1. Pinning DFN16**

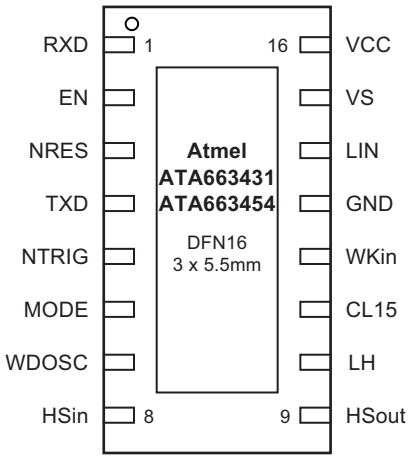



**Table 2-1. Pin Description**

| Pin | Symbol | Function |
|---|---|---|
| 1 | RXD | Receive data output |
| 2 | EN | Enable normal mode if the input is high |
| 3 | NRES | VCC undervoltage output, open drain, low at reset |
| 4 | TXD | Transmit data input |
| 5 | NTRIG | Low-level watchdog trigger input from microcontroller; if not needed, connect to VCC |
| 6 | MODE | Control input for watchdog. Low: watchdog is on. High: watchdog is off |
| 7 | WDOSC | Connection for external resistor to set the watchdog frequency |
| 8 | HSin | High-side control input |
| 9 | HSout | High-side switch output |
| 10 | LH | Failure output of the watchdog (Limp Home), open drain |
| 11 | CL15 | Ignition detection (edge sensitive); if not needed, connect to GND |
| 12 | WKin | High-voltage input for local wake-up request; if not needed, connect directly to VS |
| 13 | GND | Ground |
| 14 | LIN | LIN bus line input/output |
| 15 | VS | Supply voltage |
| 16 | VCC | Output voltage regulator 3.3V/5V/85mA |
| Backside | | Heat slug, internally connected to GND |

# 3. Pin Description

## 3.1 Supply Pin (VS)

LIN operating voltage is $V_{VS}$ = 5V to 28V. In order to avoid false bus messages, undervoltage detection is implemented to disable transmission if $V_{VS}$ falls below $V_{VS_th_N_F_down}$. After switching on $V_{VS}$, the IC starts in fail-safe mode and the voltage regulator is switched on.

The supply current in sleep mode is typically 10µA and 47µA in silent mode.

## 3.2 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It can handle ground shifts of up to 11.5% with respect to $V_{VS}$.

## 3.3 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other ICs on the PCB, and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC_th_uv_down}$.

## 3.4 Undervoltage Reset Output Pin (NRES)

If the $V_{VCC}$ voltage falls below the undervoltage detection threshold $V_{VCC_th_uv_down}$, NRES switches to low after $t_{res_f}$. Even if $V_{VCC}$ = 0V, the NRES stays low because it is internally driven from the VS voltage. If VS voltage ramps down, NRES stays low until $V_{VS}$ < 1.5V and then becomes high-impedant.

The undervoltage delay implemented keeps NRES low for $t_{Reset}$ = 4ms after $V_{VCC}$ reaches its nominal value.

## 3.5 Bus Pin (LIN)

A low-side driver is implemented with internal current limitation and thermal shutdown as well as an internal pull-up resistor in compliance with LIN specification 2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or supply disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (transition from recessive to dominant state) and the rise time (transition from dominant to recessive state) are slope-controlled.

During a short-circuit at the LIN pin to VBAT the output limits the output current to $I_{BUS_LIM}$. Due to the power dissipation, the chip temperature exceeds $T_{LINoff}$ and the LIN output is switched off. The chip cools down and, after a hysteresis of $T_{hys}$, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the VCC regulator works independently.

During a short circuit from LIN to GND the IC can be switched into sleep or silent mode and even in this case the current consumption is lower than 100µA in sleep mode and lower than 120µA in silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2µA at pin LIN during loss of $V_{Bat}$. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

## 3.6 Bus Data Input/Output (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into normal mode, it must be pulled to high longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being driven unintentionally to dominant state after normal mode has been activated (also in the case of a short circuit at TXD to GND). If TXD is short-circuited to GND, it is possible to switch to sleep mode via the EN pin after $t > t_{dom}$.

In fail-safe mode this pin is used as an output and signals the fail-safe source.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than $t_{dom}$ > 20ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, TXD needs to be set high for at least $t_{DTOrel}$ (min 10µs).

## 3.7 Bus Data Output Pin (RXD)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD. The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured with an external load capacitor of 20pF.

In silent mode the RXD output switches to high.

## 3.8 Enable Input Pin (EN)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in normal mode, with the TXD to LIN and the LIN to RXD the transmission paths both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced into silent mode. No data transmission is possible and the current consumption is reduced to $I_{VSsilent}$ typ. 47µA. The VCC regulator maintains full functionality.

If EN is switched to low while TXD is low, the device is forced into sleep mode. This disables data transmission and the voltage regulator is switched off.

Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

## 3.9 Wake Input Pin (WKin)

The WKin pin is a high-voltage input used for waking up the device from sleep mode or silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10µA is implemented. The voltage threshold for a wake-up signal is typically 2V below $V_{VS}$. If the WKin pin is not needed in the application, it can be connected directly to the VS pin.

## 3.10 CL15 Pin

The CL15 pin is a high-voltage input that can be used to wake up the device from sleep mode or silent mode. It is an edge-sensitive pin (low to-high transition). Thus, even if the CL15 pin is at high voltage ($V_{CL15} > V_{CL15H}$), it is possible to switch the IC into sleep mode or silent mode. It is usually connected to the ignition for generating a local wake-up in the application if the ignition is switched on. The CL15 pin should be tied directly to ground if not needed. A debounce timer with a value $t_{dbCL15}$ of typically 100µs is implemented. To protect this pin against transients, a serial resistor with 10kΩ and a ceramic capacitor with 47nF are recommended. With this RC combination you can increase the CL15 wake-up time.

## 3.11 WDOSC Output Pin

The WDOSC output pin provides a typical voltage of 1.23V intended to supply an external resistor with values between 34kΩ and 120kΩ. The value of the resistor adjusts the watchdog oscillator frequency to provide a certain range of time windows.

If the watchdog is disabled, the output voltage is switched off and the pin can either be tied to VCC or left open.

## 3.12 NTRIG Input Pin

The NTRIG input pin is the trigger input for the window watchdog. A pull-up resistor is implemented. A falling edge triggers the watchdog. The trigger signal (low) must exceed a minimum time of $t_{trigmin}$ to generate a watchdog trigger and avoid false triggers caused by transients.

## 3.13 Mode Input Pin (MODE)

Connect the MODE pin directly or via an external resistor to GND for normal watchdog operation. To debug the software of the connected microcontroller, connect the MODE pin to VCC and the watchdog is switched off. For fail-safe reasons, the MODE pin has a self-holding function, pulling the input to ground (i.e., watchdog enabled) in case of an open connection.

Note: If you do not use the watchdog, connect the mode pin directly to VCC.

## 3.14 Limp Home Watchdog Failure Output (LH)

The LH output pin indicates a failure of the watchdog. It is realized as a high-voltage open drain NMOS structure. During power up or after a wake-up from sleep mode the LH output is switched off. As the watchdog is only working in normal and fail-safe mode, the state of the LH output transistor can change only in these two modes. In silent mode the LH output remains in the same state as it was before switching into silent mode.

If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin.

## 3.15 High-side Switch Pins (HSout, HSin)

This high-side switch is designed for low-power loads such as LEDs, sensors or a voltage divider for measuring the supply voltage. It is functional in all operating modes of the chip except for sleep mode. Its structure is connected to the VS supply pin. This pin is short-circuit protected and also protected against overheating, whereas the protective shutdown is debounced and latched. In other words, after a protective shutdown of the output switch, the control line HSin has to go to low level first before the output can be restarted again.

The high-side switch is controlled via the low-voltage input pin HSin. If the input is high, the output is switched on. For fail-safe reasons, the HSin input is equipped with a pull-down resistor to GND. This keeps the high-side switch off in case of a missing connection from the controller.

Please note that in case of a disconnected system ground, the module can be supplied via the connected load on the high-side output and an internal ESD structure. This is the case if the load has a different ground connection than the PCB. See also the “Absolute Maximum Ratings” section for current limits in such cases.

# 4. Functional Description

## 4.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (such as the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes found in older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

## 4.2 Operating Modes

**Figure 4-1. Operating Modes**

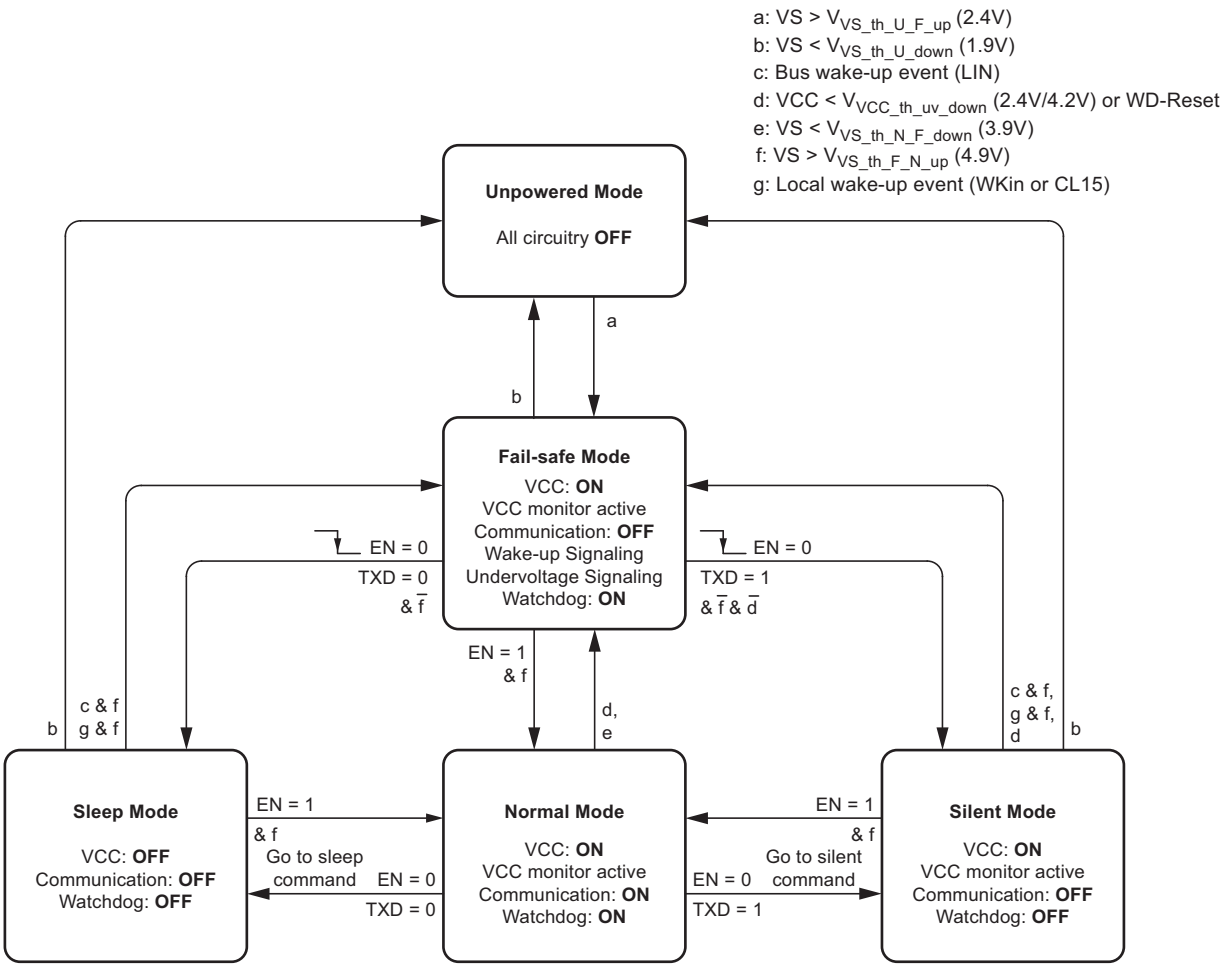



**Table 4-1. Operating Modes (Mode Pin Is Always Low)**

| Operating Modes | Transceiver | Voltage Regulator | Watchdog | LH | High-Side Output | LIN | TXD | RXD |
|---|---|---|---|---|---|---|---|---|
| Fail-safe | OFF | ON | ON | WD dependent | HSin-dependent | Recessive | Signaling fail-safe sources (see Table 4-2) | |
| Normal | ON | ON | ON | WD dependent | HSin-dependent | TXD dependent | Follows data transmission | |
| Silent | OFF | ON | OFF | Remains in previous state | HSin-dependent | Recessive | High | High |
| Sleep/Unpowered | OFF | OFF | OFF | OFF | OFF | Recessive | Low | Low |

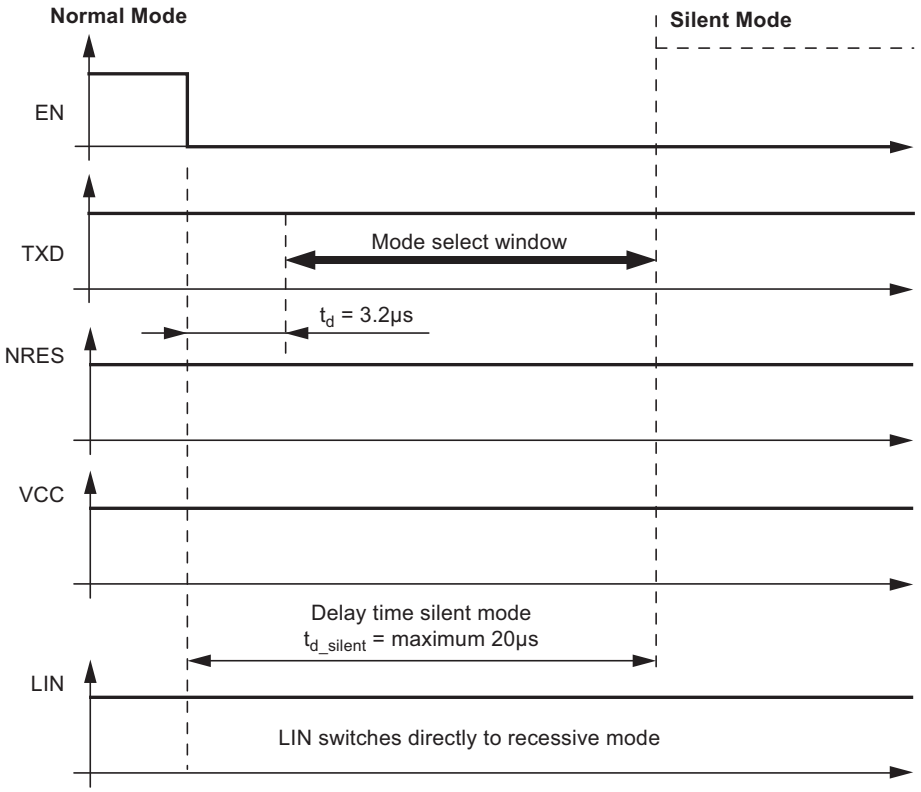
### 4.2.1 Normal Mode

This is the normal transmission and receiving mode of the LIN interface. The VCC voltage regulator works with 3.3V/5V output voltage. The watchdog needs a trigger signal from NTRIG to avoid resets at NRES. If NRES switches to low, the IC changes its state to fail-safe mode.

### 4.2.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into silent mode. The TXD signal has to be logic high during the mode select window. The transmission path is disabled in silent mode. The voltage regulator is active. The overall supply current from VBAT is a combination of the $I_{VSsilent}$ of typ. 47µA plus the VCC regulator output current $I_{VCC}$.

**Figure 4-2. Switching to Silent Mode**



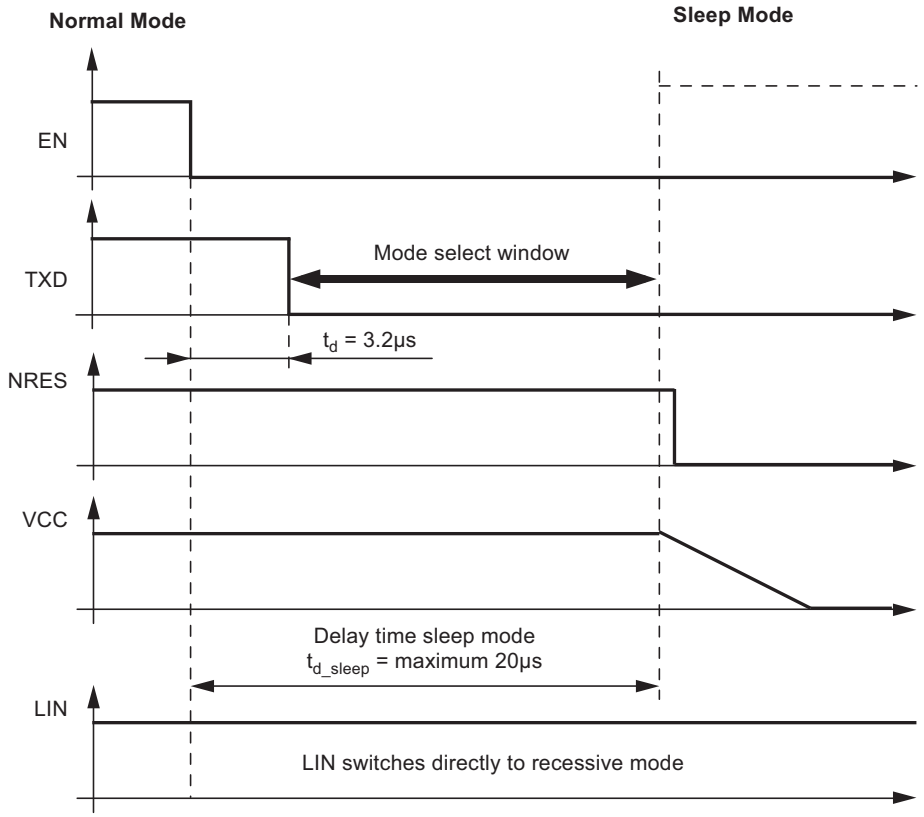

In silent mode, the internal slave termination between the LIN pin and VS pin is disabled to minimize current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) is present between the LIN pin and the VS pin. Silent mode can be activated regardless of the current level on the LIN pin or WKin pin.

If an undervoltage condition occurs, NRES is switched to low and the Atmel ATA663431/ATA663454 changes its state to fail-safe mode.

### 4.2.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC to sleep mode. The TXD signal has to be logic low during the mode select window.

**Figure 4-3. Switching to Sleep Mode**




In order to avoid any influence on the LIN pin while switching into sleep mode, it is possible to switch the EN to low up to 3.2µs earlier than the TXD. The best and easiest way is to generate two simultaneous falling edges at TXD and EN.

The transmission path is disabled in sleep mode. Supply current from VBAT is typically $I_{VSsleep}$ = 10µA. The VCC regulator is switched off; NRES and RXD are low. The internal slave termination between the LIN and VS pins is disabled to minimize current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) between the LIN pin and VS pin is present. Sleep mode can be activated independently from the current level on the LIN pin. A voltage less than the LIN pre-wake detection $V_{LINL}$ at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

If TXD is short-circuited to GND, it is possible to switch to sleep mode via EN after $t > t_{dom}$.

### 4.2.4 Fail-Safe Mode

The device automatically switches to fail-safe mode at system power-up. The voltage regulator and the watchdog are switched on. The NRES output remains low for $t_{res}$ = 4ms and resets the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. A low at NRES switches the IC directly into fail-safe mode. During fail-safe mode the TXD pin is an output and together with the RXD output pin transmits a signal indicating the fail-safe source.

If the device enters fail-safe mode coming from normal mode (EN=1) due to a $V_{VS}$ undervoltage condition ($V_{VS} < V_{VS_th_N_F_down}$), it is possible to switch to sleep mode or silent mode through a falling edge at the EN input. The current consumption can be reduced further with this feature.

A wake-up event from either silent mode or sleep mode is indicated to the microcontroller using the two pins RXD and TXD. A $V_{VS}$ undervoltage condition is also indicated at these two pins. The coding is shown in Table 4-2.

A wake-up event switches the IC to fail-safe mode.

**Table 4-2. Signaling in Fail-safe Mode**

| Fail-Safe Sources | TXD | RXD |
|---|---|---|
| LIN wake-up (LIN pin) | Low | Low |
| Local wake-up (WKin pin or CL15 pin) | Low | High |
| $V_{VS_th_N_F_down}$ (battery) undervoltage detection ($V_{VS}$ < 3.9V) | High | Low |

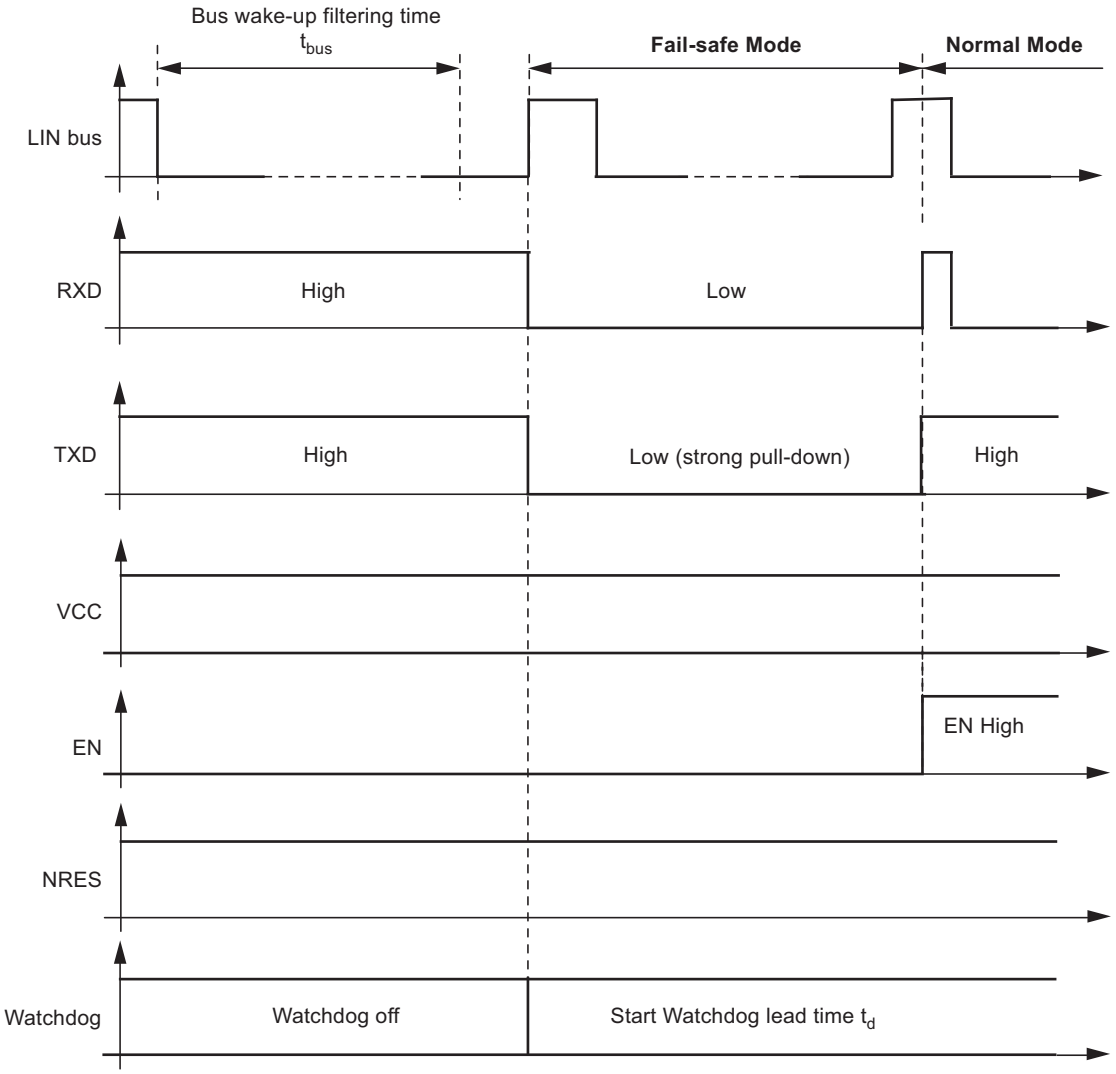
## 4.3 Wake-up Scenarios from Silent Mode or Sleep Mode

### 4.3.1 Remote Wake-up via LIN Bus

#### 4.3.1.1 Remote Wake-up from Silent Mode

A remote wake-up from silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection $V_{LINL}$ at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a given time period (> $t_{bus}$) and the following rising edge at the LIN pin (see Figure 4-4) result in a remote wake-up request. The device switches from silent mode to fail-safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD and TXD pins (strong pull-down at TXD). EN high can be used to switch directly to normal mode.

**Figure 4-4. LIN Wake-up from Silent Mode**



### 4.3.1.2 Remote Wake-up from Sleep Mode

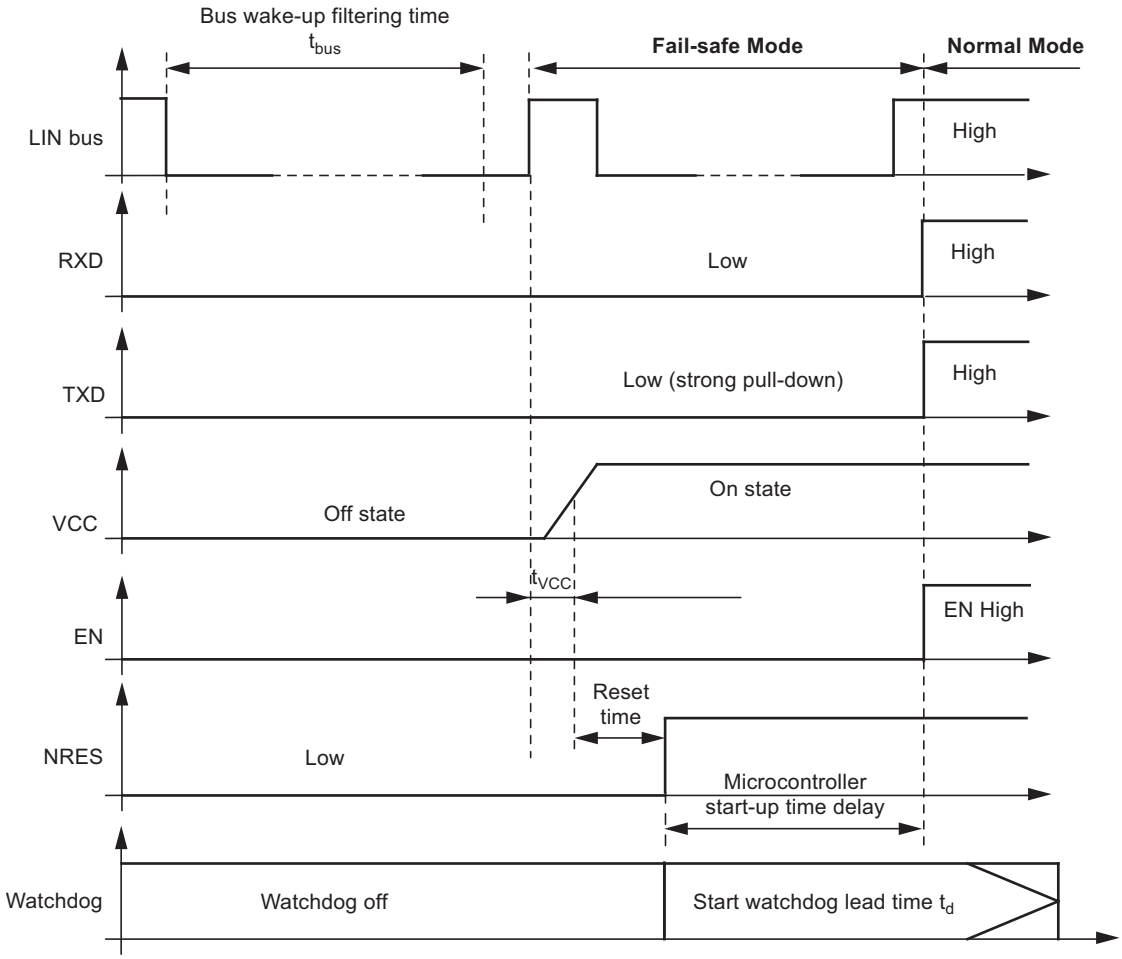
A voltage less than the LIN pre-wake detection $V_{LINL}$ at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a given time period (> $t_{bus}$) and a subsequent rising edge at the LIN pin results in a remote wake-up request. The device switches from sleep mode to fail-safe mode.

The VCC regulator is activated, and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull-down at TXD).

EN high can be used to switch directly from sleep/silent to fail-safe mode. If EN is still high after $V_{CC}$ ramp-up and the undervoltage reset time, the IC switches to normal mode.

**Figure 4-5. LIN Wake-up from Sleep Mode**



### 4.3.2 Local Wake-up via WKin Pin

A falling edge at the WKin pin followed by a low level maintained for a given time period (> $t_{WKin}$) results in a local wake-up request. The device switches to fail-safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the WKin pin is low, it is possible to switch to silent mode or sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10µs before the negative edge at WKin starts a new local wake-up request.

**Figure 4-6. Local Wake-up via WKin pin from Sleep Mode**

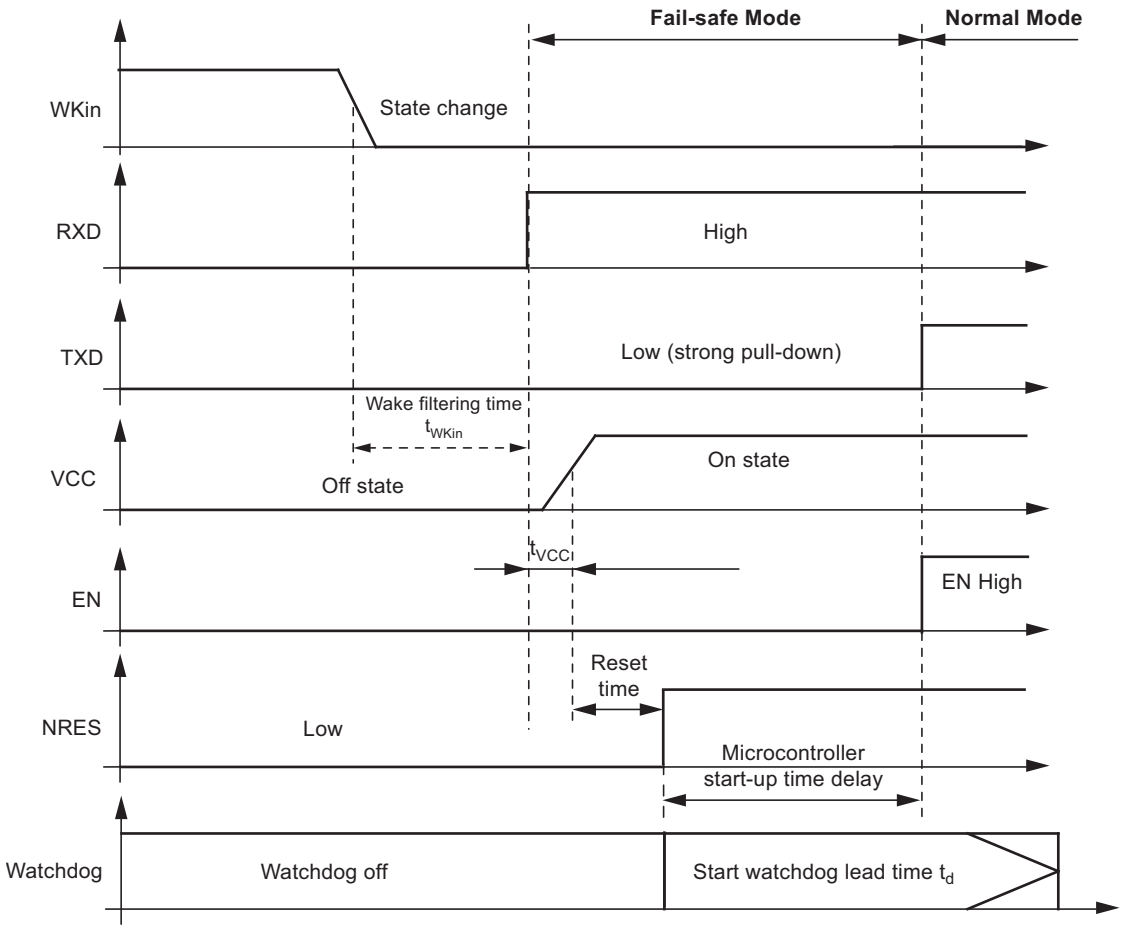
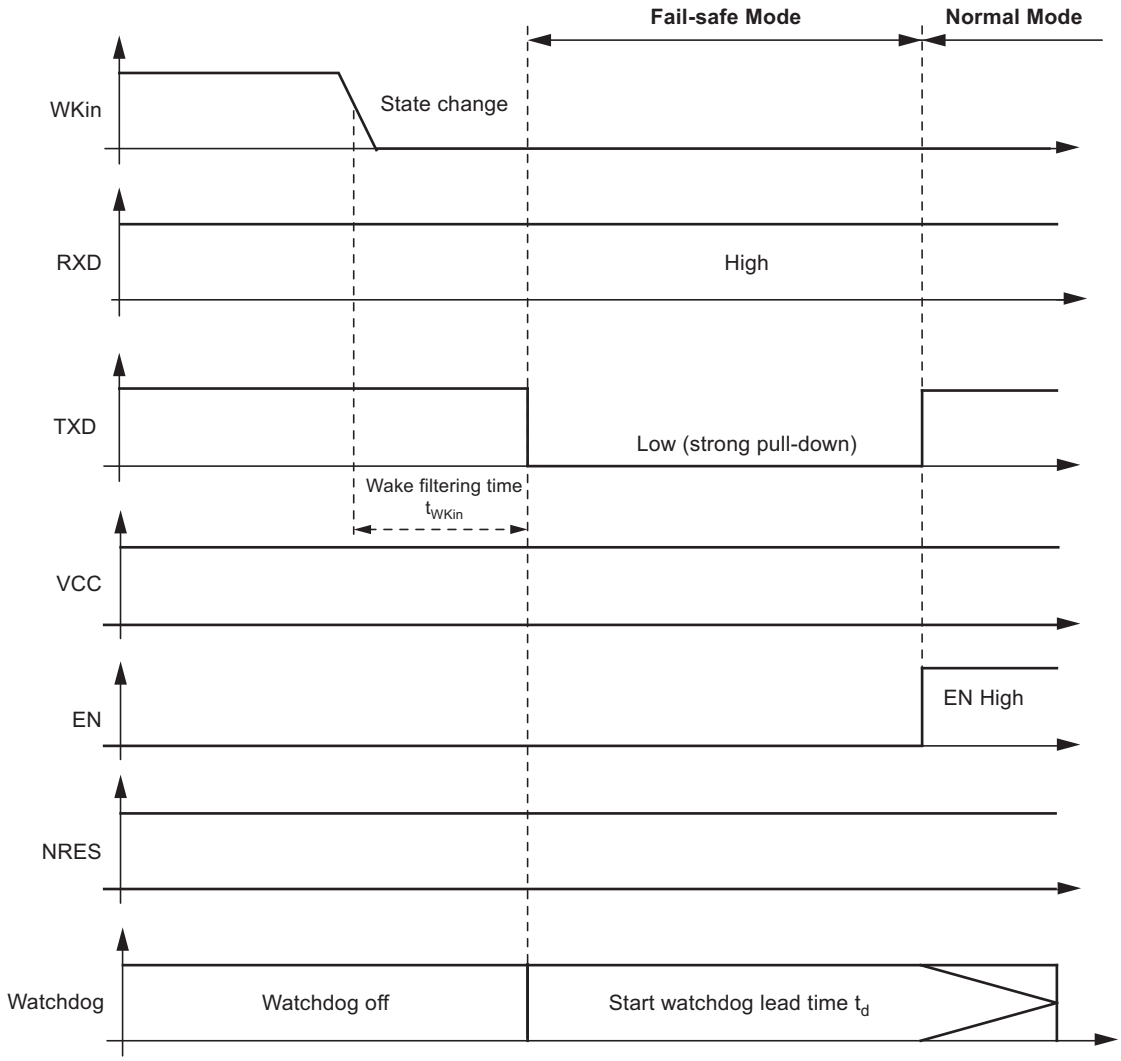


**Figure 4-7. Local Wake-up via WKin pin from Silent Mode**




### 4.3.3 Local Wake-up via CL15

A voltage on pin CL15 above $V_{CL15H}$ for at least $t_{dbCL15}$ results in a local wake-up request. The device switches to fail-safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. Even when the CL15 pin is high, it is possible to switch to silent mode or sleep mode via the EN pin. In this case, the wake-up signal at CL15 has to be switched to low > 10µs before the rising edge at CL15 starts a new local wake-up request.

### 4.3.4 Wake-up Source Recognition

The device can distinguish between different wake-up sources (see Table 4-3). The wake-up source can be read on the TXD and RXD pin in fail-safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in normal mode.

**Table 4-3. Signaling in Fail-safe Mode**

| Fail-Safe Sources | TXD | RXD |
|---|---|---|
| LIN wake-up (LIN pin) | Low | Low |
| Local wake-up (WKin pin or CL15 pin) | Low | High |
| $V_{VS_th_N_F_down}$ (battery) undervoltage detection ($V_{VS}$ < 3.9V) | High | Low |

## 4.4 Behavior under Low Supply Voltage Conditions

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 4-12 on page 17). If $V_{VS}$ is higher than the minimum $V_{VS}$ operation threshold $V_{VS_th_U_F_up}$ (typ. 2.25V), the IC mode changes from unpowered mode to fail-safe mode. As soon as $V_{VS}$ exceeds the undervoltage threshold $V_{VS_th_F_N_up}$ (typ. 4.6V), the LIN transceiver can be activated. The VCC output voltage reaches its nominal value after $t_{VCC}$. This parameter depends on the externally applied VCC capacitor and the load. The NRES output is low for the reset time delay $t_{reset}$. No mode change is possible during this time $t_{reset}$.

The behavior of VCC, NRES and VS is shown in following diagrams (ramp-up and ramp-down):

**Figure 4-8. VCC and NRES versus VS (Ramp-up) for ATA663431**

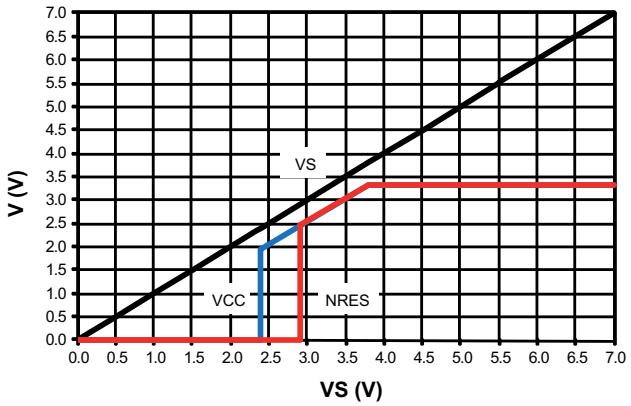



**Figure 4-9. VCC and NRES versus VS (Ramp-down) for ATA663431**

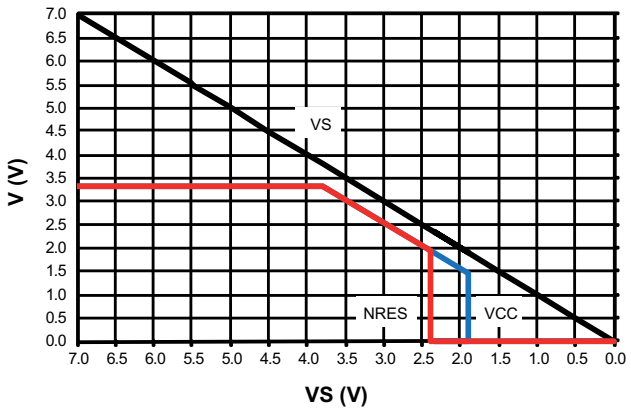


**Figure 4-10. VCC and NRES versus VS (Ramp-up) for ATA663454**

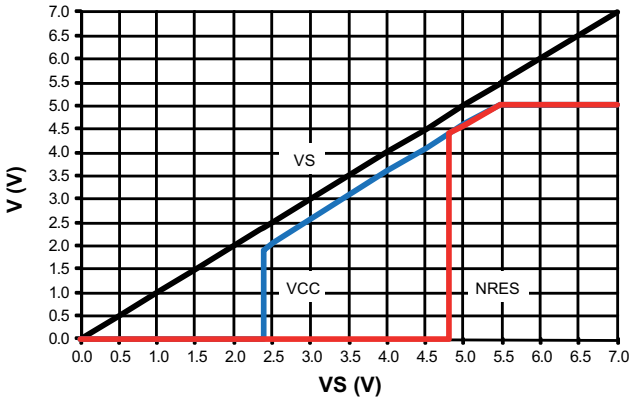
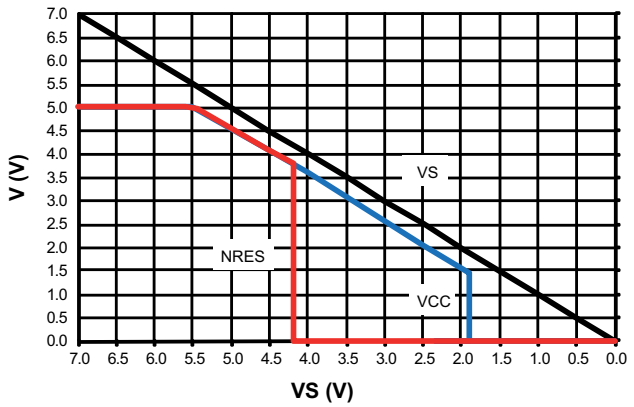



**Figure 4-11. VCC and NRES versus VS (Ramp-down) for ATA663454**




Please note that the upper graphs are only valid if the $V_{VS}$ ramp-up and ramp-down time is much slower than the VCC ramp-up time $t_{Vcc}$ and the NRES delay time $t_{reset}$.

If during **sleep mode** the voltage level of $V_{VS}$ drops below the undervoltage detection threshold $V_{VS_th_N_F_down}$ (typ. 4.3V), the operating mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the $V_{VS}$ operation threshold $V_{VS_th_U_down}$ (typ. 2.05V) does the IC switch to unpowered mode.

If during **silent mode** the VCC voltage drops below the VCC undervoltage threshold $V_{VCC_th_uv_down}$ the IC switches into fail-safe mode. If the supply voltage on pin VS drops below the $V_{VS}$ operation threshold $V_{VS_th_U_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

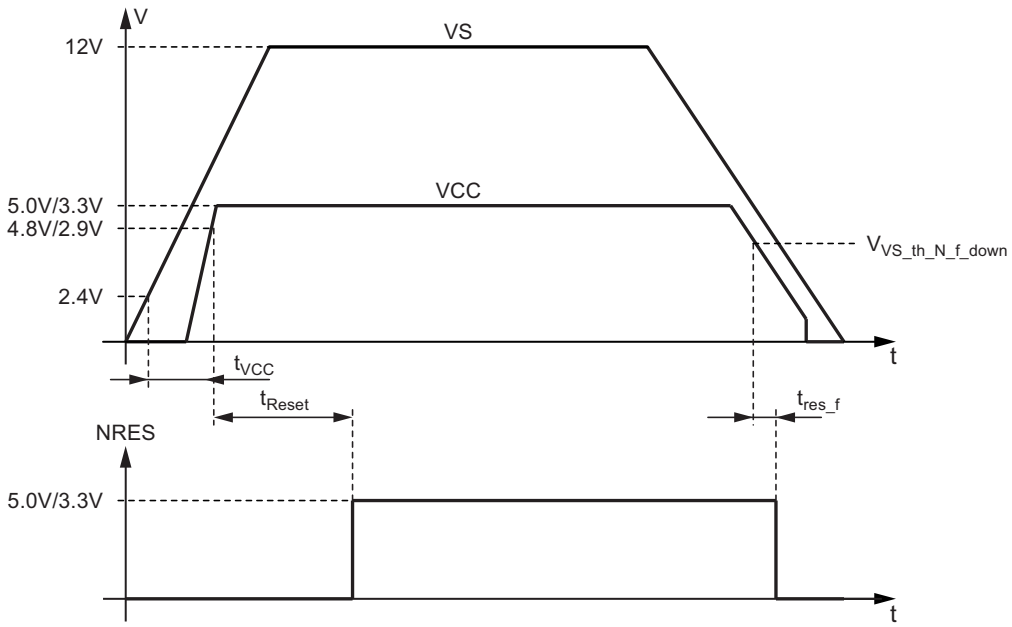
If during **normal mode** the voltage level on pin VS drops below the $V_{VS}$ undervoltage detection threshold $V_{VS_th_N_F_down}$ (typ. 4.3V), the IC switches to fail-safe mode. This means the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

> **For ATA663431**: In this undervoltage situation, it is possible to switch the device into sleep mode or silent mode through a falling edge at the EN input pin. This feature ensures that it is always possible to switch to these two current saving modes so that current consumption can be reduced even further.
>
> When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC_th_uv_down}$ (typ. 2.6V) the IC switches into fail-safe mode.
>
> **For ATA663454**: Because of the VCC undervoltage condition in this situation, the IC is in fail-safe mode and can be switched into sleep mode only.
>
> Only when the supply voltage $V_{VS}$ drops below the operation threshold $V_{VS_th_U_down}$ (typ. 2.05V) does the IC switch into unpowered mode.

The current consumption of the ATA663431/ATA663454 in silent mode is always below 200µA, even when the supply voltage $V_{VS}$ is lower than the regulator's nominal output voltage VCC.

## 4.5 Voltage Regulator

**Figure 4-12. VCC Voltage Regulator: Supply Voltage Ramp-up and Ramp-down**

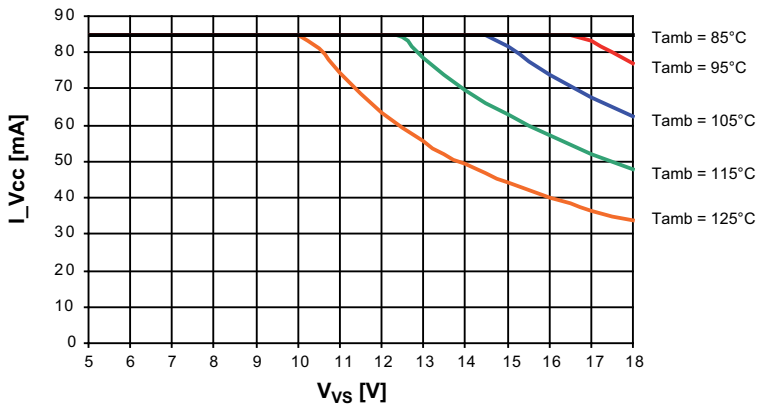



The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 1.8µF together with a 100nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

When the Atmel ATA663431/ATA663454 is being soldered onto the PCB, it is mandatory to connect the heat slug with a wide GND plate on the printed board to achieve a good heat sink.

The main power dissipation of the IC is created from the VCC regulator output current $I_{VCC}$, which is needed for the application. Figure 4-13 shows the safe operating area of the Atmel ATA663431/ATA663454 without considering any output current of the high-side output HSOUT.

**Figure 4-13. Power Dissipation: Safe Operating Area: Regulator's Output Current $I_{VCC}$ versus Supply Voltage $V_{VS}$ at Different Ambient Temperatures ($R_{thja}$ = 45K/W assumed)**



## 4.6 Watchdog

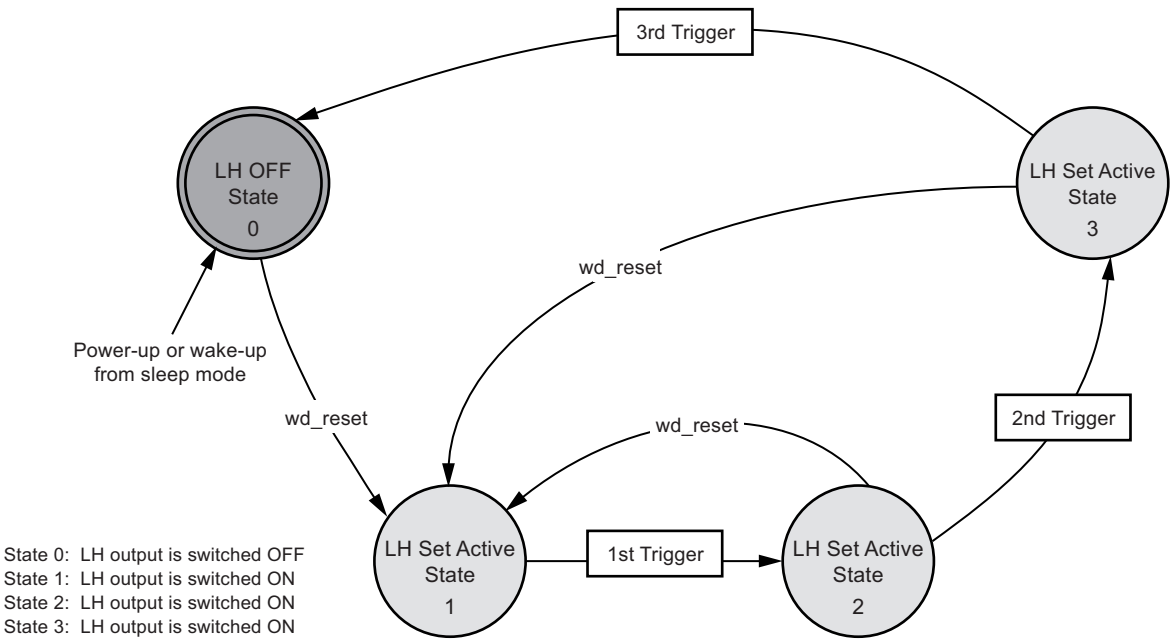
The watchdog anticipates a trigger signal from the microcontroller at the NTRIG (negative edge) input within a time window of $t_{wd}$. The trigger signal must exceed a minimum time of $t_{trigmin}$ > 200ns. If a trigger signal is not received, a reset signal is generated at output NRES and the LH output transistor switches on. The timing basis of the watchdog is provided by the internal oscillator. Its time period, $t_{osc}$, is adjustable via the external resistor $R_{WDOSC}$ (34kΩ to 120kΩ). During silent or sleep mode the watchdog is switched off to reduce current consumption. The minimum time for the first watchdog pulse is required after the undervoltage reset at NRES disappears, it is defined as lead time $t_d$. After wake-up from sleep mode, the lead time $t_d$ starts with the rising edge at the NRES output. After a wake-up from silent mode, the lead time $t_d$ starts with the falling edge at the TXD pin.

The Limp Home output LH is a high voltage NMOS open drain structure which is signaling watchdog failures. It works independently of the VCC voltage. So it is possible to switch on some external devices in the case of a watchdog failure independent from the microcontroller and the VCC voltage. During power up or after a wake-up from sleep mode the LH output is switched off. If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin.

As the watchdog is only working in normal and fail-safe mode, the state of the LH output transistor can change only in these two modes. In silent mode the LH output remains in the same state as it was before switching into silent mode. When the watchdog is disabled via a high level at the mode pin or during sleep or unpowered mode, the LH output is also disabled.

The behavior of the LH output when the watchdog is active during fail-safe and normal mode is depicted in Figure 4-14.

**Figure 4-14. Limp Home (LH) State Diagram**




In sleep mode and unpowered mode the watchdog and therefore the LH output are deactivated. In silent mode the LH output remains in the same state as it was before switching into silent mode

### 4.6.1 Typical Timing Sequence with $R_{WDOSC}$ = 51kΩ

The trigger signal $t_{wd}$ is adjustable between 20ms and 64ms using the external resistor $R_{WDOSC}$.

For example, with an external resistor of $R_{WDOSC}$ = 51kΩ ±1%, the typical parameters of the watchdog are as follows:

$t_{osc} = (0.405 \times R_{WDOSC} - 0.0004 \times (R_{WDOSC})^2) \times 2$ ($R_{WDOSC}$ in kΩ ; $t_{osc}$ in µs)

$t_{osc}$ = 39.3µs due to 51kΩ

$t_d$ = 3984 × 39.2µs = 154.8ms

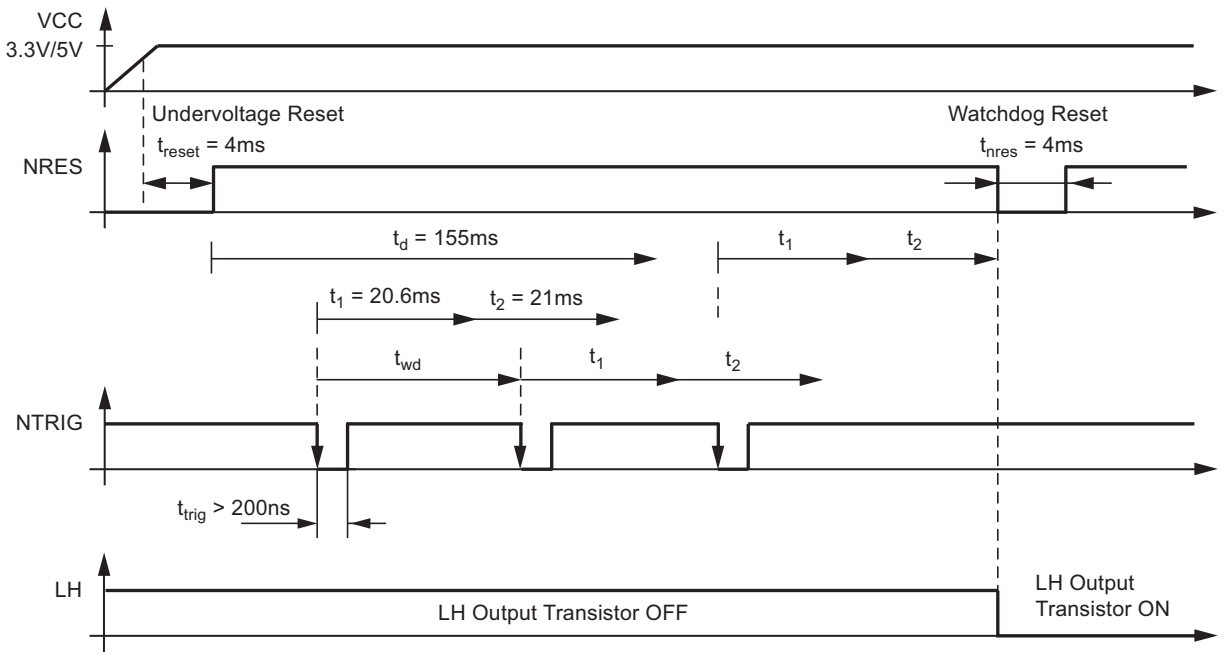
$t_1$ = 527 × 39.2µs = 20.6ms

$t_2$ = 553 × 39.3µs = 21.6ms

$t_{nres}$ = constant = 4ms

After ramping up the battery voltage, the 5V regulator is switched on. The reset output NRES stays low for the time $t_{reset}$ (typically 4ms), then it switches to high and the watchdog waits for the trigger sequence from the microcontroller. During power up or after a wake-up from sleep mode the LH output is switched off. If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin. The lead time, $t_d$, follows the reset and is $t_d$ = 155ms. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG occurs during this time, the time $t_1$ starts immediately. If no trigger signal occurs during the time $t_d$, a watchdog reset with $t_{NRES}$ = 4ms will reset the microcontroller after $t_d$ = 155ms and the LH output transistor switches on. The times $t_1$ and $t_2$ have a fixed relationship. A trigger signal from the microcontroller is anticipated within the time frame of $t_2$ = 21.6ms. To avoid false triggering from glitches, the trigger pulse must be longer than $t_{trigmin}$ > 200ns. This slope serves to restart the watchdog sequence. If the triggering signal fails in this open window $t_2$, the NRES output is drawn to ground as well as the LH output. A trigger signal during the closed window $t_1$ immediately switches NRES and LH to low.

**Figure 4-15. Timing Sequence with $R_{WDOSC}$ = 51kΩ**



### 4.6.2 Worst-Case Calculation with $R_{WDOSC}$ = 51kΩ

The internal oscillator has a tolerance of 20%. This means that $t_1$ and $t_2$ can also vary by 20%. The worst-case calculation for the watchdog period $t_{wd}$ is calculated as follows. The ideal watchdog time $t_{wd}$ is between the maximum $t_1$ and the minimum $t_1$ plus the minimum $t_2$.

$t_{1,min} = 0.8 \times t_1 = 16.5ms$, $t_{1,max} = 1.2 \times t_1 = 24.8ms$

$t_{2,min} = 0.8 \times t2 = 17.3ms$, $t_{2,max} = 1.2 \times t_2 = 26ms$

$t_{wdmax} = t_{1,min} + t_{2,min} = 16.5ms + 17.3ms = 33.8ms$

$t_{wdmin} = t_{1,max} = 24.8ms$

$t_{wd} = 29.3ms \pm 4.5ms (\pm 15\%)$

A microcontroller with an oscillator tolerance of ±15% is sufficient to supply the trigger inputs correctly.

**Table 4-4. Typical Watchdog Timings**

| $R_{WDOSC}$ kΩ | Oscillator Period $t_{osc}$/µs | Lead Time $t_d$/ms | Closed Window $t_1$/ms | Open Window $t_2$/ms | Trigger Period from Microcontroller $t_{wd}$/ms | Reset Time $t_{nres}$/ms |
|---|---|---|---|---|---|---|
| 34 | 13.3 × 2 | 105 | 14.0 | 14.7 | 19.9 | 4 |
| 51 | 19.61 × 2 | 154.8 | 20.64 | 21.67 | 29.32 | 4 |
| 91 | 3.54 × 2 | 264.80 | 35.32 | 37.06 | 50.14 | 4 |
| 120 | 42.84 × 2 | 338.22 | 45.11 | 47.34 | 64.05 | 4 |

If the WDOSC pin has a short circuit to GND or the external resistor at the WDOSC pin is disconnected, the watchdog runs with an internal oscillator and guarantees a reset and activation of the LH output.

# 5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage $V_{VS}$<br>- DC voltage<br>- $T_a$ = 25°C, $t_{Pulse}$ ≤ 500ms, $I_{VCC}$ ≤ 85mA<br>- $T_a$ = 25°C, $t_{Pulse}$ ≤ 2min, $I_{VCC}$ ≤ 85mA | $V_{VS}$ | –0.3 | | +40<br>+43.5<br>+28 | V |
| Logic pin voltage levels (TXD, RXD, EN, HSin, MODE, WDOSC, NRES, NTRIG) | $V_{LOGIC}$ | –0.3 | | +5.5 | V |
| Logic pin output DC currents | $I_{LOGIC}$ | –5 | | +5 | mA |
| LIN bus levels $V_{LIN}$<br>- DC voltage<br>- Pulse time ≤ 500ms | $V_{LIN}$ | –27 | | +40<br>+43.5 | V<br>V |
| $V_{CC}$<br>- DC voltage<br>- DC input current | $V_{VCC}$<br>$I_{VCC}$ | –0.3 | | +5.5<br>+200 | V<br>mA |
| Logic level pins injection currents<br>- DC currents<br>- $t_{Pulse}$ ≤ 2min | $I_{LOGIC}$ | –5<br>–5 | | 0.1<br>+5 | mA |
| LH voltage levels | $V_{LH}$ | –0.3 | | $V_{VS}$ + 0.3 | V |
| HSout<br>- DC voltage<br>- DC output current<br>- DC current injection levels<br>$V_{HSout}$ < 0V and $V_{HSout}$ > $V_{VS}$ | $V_{HSout}$<br>$I_{HSout}$<br>$I_{HSout}$ | –0.3<br>–50<br>–20 | | $V_{VS}$ + 0.3<br><br>+10 | V<br>mA<br>mA |
| CL15 voltage levels<br>- DC voltage | $V_{CL15}$ | –0.3 | | +40 | V |
| WKin voltage levels<br>- DC voltage<br>-Transient voltage according to ISO7637 (coupling 1nF), (with 2.7K serial resistor) | $V_{WKin}$ | –0.3<br><br>–150 | | +40<br><br>+100 | V |
| ESD according to IBEE LIN EMC<br>Test spec. 1.0 following IEC 61000-4-2<br>- Pin VS, WKin and LIN to GND<br>(CL15 and WKin with ext. circuitry according to applications diagram) | | ±6 | | | kV |
| ESD according to ISO10605, with 330pF/330Ω<br>- Pin HSout (100Ω series resistor, 22nF to GND) to GND | | ±6 | | | kV |
| ESD (HBM following STM5.1 with 1.5kΩ/100pF)<br>- Pin VS, LIN, WKin, HSout, CL15 to GND | | ±6 | | | kV |
| Component level ESD (HBM according to ANSI/ESD STM5.1)<br>JESD22-A114<br>AEC-Q100 (002) | | ±3 | | | kV |
| CDM ESD STM 5.3.1 | | ±750 | | | V |
| ESD machine model<br>AEC-Q100-RevF(003) | | ±100 | | | V |
| Junction temperature | $T_j$ | –40 | | +150 | °C |
| Storage temperature | $T_s$ | –55 | | +150 | °C |

## 6. Thermal Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Thermal resistance junction to heat slug | $R_{thjc}$ | | 8 | | K/W |
| Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC | $R_{thja}$ | | 45 | | K/W |
| Thermal shutdown of $V_{VCC}$ regulator | $T_{VCCoff}$ | 150 | 165 | 180 | °C |
| Thermal shutdown of LIN output | $T_{LINoff}$ | 150 | 165 | 180 | °C |
| Thermal shutdown of high-side driver | $T_{DSoff}$ | 150 | 165 | 180 | °C |
| Thermal shutdown hysteresis | $T_{hys}$ | | 10 | | °C |

## 7. Electrical Characteristics

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 1 | VS pin | | | | | | | | |
| 1.1 | Nominal DC voltage range | | VS | $V_{VS}$ | 5 | 13.5 | 28 | V | A |
| 1.2 | Supply current in sleep mode | Sleep mode<br>$V_{LIN}$ > $V_{VS}$ – 0.5V<br>$V_{VS}$ < 14V, T = 27°C | VS | $I_{VSsleep}$ | 5 | 10 | 15 | µA | B |
| | | Sleep mode<br>$V_{LIN}$ > $V_{VS}$ – 0.5V<br>$V_{VS}$ < 14V | VS | $I_{VSsleep}$ | 3 | 11 | 18 | µA | A |
| | | Sleep mode, $V_{LIN}$ = 0V<br>Bus shorted to GND<br>$V_{VS}$ < 14V | VS | $I_{VSsleep_short}$ | 20 | 50 | 100 | µA | A |
| 1.3 | Supply current in silent mode | Bus recessive<br>5.5V < $V_{VS}$ < 14V, HS-driver off<br>without load at VCC<br>T = 27°C | VS | $I_{VSsilent}$ | 30 | 47 | 58 | µA | B |
| | | Bus recessive<br>5.5V < $V_{VS}$ < 14V, HS-driver off<br>without load at VCC | VS | $I_{VSsilent}$ | 30 | 50 | 64 | µA | A |
| | | Bus recessive<br>$V_{VS}$ < 5.5V, $V_{VCC}$ > $V_{VCC_th_uv}$<br>HS-driver off<br>without load at VCC | VS | $I_{VSsilent}$ | 30 | 150 | 190 | µA | A |
| | | Silent mode<br>5.5V < $V_{VS}$ < 14V, HS-driver off<br>without load at VCC<br>Bus shorted to GND | VS | $I_{VSsilent_short}$ | 50 | 90 | 130 | µA | A |
| 1.4 | Supply current in normal mode | Bus recessive<br>$V_{VS}$ < 14V, HS-driver off<br>without load at VCC, watchdog<br>on, 51kΩ at WDOSC | VS | $I_{VSrec}$ | 300 | 400 | 500 | µA | A |
| | | Bus recessive<br>$V_{VS}$ < 14V, HS-driver off<br>without load at VCC, watchdog<br>off ($V_{MODE}$ = $V_{VCC}$) | VS | $I_{VSrec}$ | 150 | 250 | 350 | µA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 1.5 | Supply current in normal mode | Bus dominant (internal LIN pull-up resistor active) $V_{VS}$ < 14V, HS-driver off without load at VCC, watchdog on, 51kΩ at WDOSC | VS | $I_{VSdom}$ | 600 | 900 | 1150 | µA | A |
| | | Bus dominant (internal LIN pull-up resistor active) $V_{VS}$ < 14V, HS-driver off without load at VCC, watchdog off ($V_{MODE}$ = $V_{VCC}$) | VS | $I_{VSdom}$ | 500 | 750 | 1000 | µA | A |
| 1.6 | Supply current in fail-safe mode | Bus recessive 5.5V < $V_{VS}$ < 14V, HS-driver off without load at VCC, watchdog on, 51kΩ at WDOSC | VS | $I_{VSfail}$ | 100 | 200 | 300 | µA | A |
| | | Bus recessive 5.5V < $V_{VS}$ < 14V, HS-driver off without load at VCC, watchdog off ($V_{MODE}$ = $V_{VCC}$) | VS | $I_{VSfail}$ | 40 | 70 | 100 | µA | A |
| | | Bus recessive 2V < $V_{VS}$ < 5.5V, HS-driver off without load at VCC watchdog on, 51kΩ at WDOSC | VS | $I_{VSfail}$ | 150 | 280 | 320 | µA | A |
| | | Bus recessive 2V < $V_{VS}$ < 5.5V, HS-driver off without load at VCC watchdog off ($V_{MODE}$ = $V_{VCC}$) | VS | $I_{VSfail}$ | 50 | 150 | 200 | µA | A |
| 1.7 | VS undervoltage threshold (switching from normal mode to fail-safe mode) | Decreasing supply voltage | VS | $V_{VS_th_N_F_down}$ | 3.9 | 4.3 | 4.7 | V | A |
| | | Increasing supply voltage | VS | $V_{VS_th_F_N_up}$ | 4.1 | 4.6 | 4.9 | V | A |
| 1.8 | VS undervoltage hysteresis | | VS | $V_{VS_hys_F_N}$ | 0.1 | 0.25 | 0.4 | V | A |
| 1.9 | VS operation threshold (switching to unpowered mode) | Switch to unpowered mode | VS | $V_{VS_th_U_down}$ | 1.9 | 2.05 | 2.3 | V | A |
| | | Switch from unpowered mode to fail-safe mode | VS | $V_{VS_th_U_F_up}$ | 2.0 | 2.25 | 2.4 | V | A |
| 1.10 | VS undervoltage hysteresis | | VS | $V_{VS_hys_U}$ | 0.1 | 0.2 | 0.3 | V | A |
| 2 | RXD output pin | | | | | | | | |
| 2.1 | Low-level output sink capability | Normal mode, $V_{LIN}$ = 0V, $I_{RXD}$ = 2mA | RXD | $V_{RXDL}$ | | 0.2 | 0.4 | V | A |
| 2.2 | High-level output source capability | Normal mode $V_{LIN}$ = $V_S$, $I_{RXD}$ = –2mA | RXD | $V_{RXDH}$ | $V_{CC}$ – 0.4V | $V_{CC}$ – 0.2V | | V | A |
| 3 | TXD input/output pin | | | | | | | | |
| 3.1 | Low-level voltage input | | TXD | $V_{TXDL}$ | –0.3 | | +0.8 | V | A |
| 3.2 | High-level voltage input | | TXD | $V_{TXDH}$ | 2 | | $V_{CC}$ + 0.3V | V | A |
| 3.3 | Pull-up resistor | $V_{TXD}$ = 0V | TXD | $R_{TXD}$ | 40 | 70 | 100 | kΩ | A |
| 3.4 | High-level leakage current | $V_{TXD}$ = $V_{CC}$ | TXD | $I_{TXD}$ | –3 | | +3 | µA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 3.5 | Low-level output sink current at wake-up request | Fail-safe mode<br>$V_{LIN} = V_{VS}$<br>$V_{WKin} = 0V$<br>$V_{TXD} = 0.4V$ | TXD | $I_{TXD}$ | 2 | 2.5 | 8 | mA | A |
| 4 | EN input pin | | | | | | | | |
| 4.1 | Low-level voltage input | | EN | $V_{ENL}$ | –0.3 | | +0.8 | V | A |
| 4.2 | High-level voltage input | | EN | $V_{ENH}$ | 2 | | $V_{CC}$ + 0.3V | V | A |
| 4.3 | Pull-down resistor | $V_{EN} = V_{VCC}$ | EN | $R_{EN}$ | 50 | 125 | 200 | kΩ | A |
| 4.4 | Low-level input current | $V_{EN} = 0V$ | EN | $I_{EN}$ | –3 | | +3 | µA | A |
| 5 | NRES open drain output pin | | | | | | | | |
| 5.1 | Low-level output voltage | $V_{VS} \geq 5.5V$<br>$I_{NRES} = 2mA$ | NRES | $V_{NRESL}$ | | 0.2 | 0.4 | V | A |
| 5.2 | Undervoltage reset time | $V_{VS} \geq 5.5V$<br>$C_{NRES} = 20pF$ | NRES | $t_{Reset}$ | 2 | 4 | 6 | ms | A |
| 5.3 | Reset debounce time for falling edge | $V_{VS} \geq 5.5V$<br>$C_{NRES} = 20pF$ | NRES | $t_{res_f}$ | 0.5 | | 10 | µs | A |
| 5.4 | Switch-off leakage current | $V_{NRES} = 5.5V$ | NRES | $I_{NRES_L}$ | –3 | | +3 | µA | A |
| 6 | VCC voltage regulator ATA663431 | | | | | | | | |
| 6.1 | Output voltage VCC | 4V < $V_{VS}$ < 18V<br>(0mA to 50mA) | VCC | $V_{VCCnor}$ | 3.234 | | 3.366 | V | A |
| | | 4.5V < $V_{VS}$ < 18V<br>(0mA to 85mA) | VCC | $V_{VCCnor}$ | 3.234 | | 3.366 | V | C |
| 6.2 | Output voltage $V_{VCC}$ at low $V_{VS}$ | 3V < $V_{VS}$ < 4V | VCC | $V_{VCClow}$ | $V_{VS} - V_D$ | | 3.366 | V | A |
| 6.3 | Regulator drop voltage | $V_{VS}$ > 3V, $I_{VCC}$ = –15mA | VCC | $V_{D1}$ | | 200 | 250 | mV | A |
| 6.4 | Regulator drop voltage | $V_{VS}$ > 3V, $I_{VCC}$ = –50mA | VCC | $V_{D2}$ | | 300 | 500 | mV | A |
| 6.5 | Line regulation maximum | 4V < $V_{VS}$ < 18V | VCC | $VCC_{line}$ | | 0.1 | 0.2 | % | A |
| 6.6 | Load regulation maximum | 5mA < $I_{VCC}$ < 50mA | VCC | $VCC_{load}$ | | 0.1 | 0.5 | % | A |
| 6.7 | Output current limitation | $V_{VS}$ > 4V | VCC | $I_{VCClim}$ | | –180 | –120 | mA | A |
| 6.8 | Load capacity | MLC capacitor | VCC | $C_{load}$ | 1.8 | 2.2 | | µF | D |
| 6.9 | VCC undervoltage threshold (NRES ON) | Referred to VCC<br>$V_{VS}$ > 4V | VCC | $V_{VCC_th_uv_down}$ | 2.4 | 2.6 | 2.8 | V | A |
| | VCC undervoltage threshold (NRES OFF) | Referred to VCC<br>$V_{VS}$ > 4V | VCC | $V_{VCC_th_uv_up}$ | 2.5 | 2.7 | 2.9 | V | A |
| 6.10 | Hysteresis of VCC undervoltage threshold | Referred to VCC<br>$V_{VS}$ > 4V | VCC | $V_{VCC_hys_uv}$ | 100 | 200 | 300 | mV | A |
| 6.11 | Ramp-up time $V_{VS}$ > 4V to VCC = 3.3V | $C_{VCC} = 2.2µF$<br>$I_{load}$ = –5mA at VCC | VCC | $t_{VCC}$ | | 1 | 1.5 | ms | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 7 | VCC voltage regulator ATA663454 | | | | | | | | |
| 7.1 | Output voltage VCC | 5.5V < $V_{VS}$< 18V (0mA to 50mA) | VCC | $V_{VCCnor}$ | 4.9 | | 5.1 | V | A |
| | | 6V < $V_{VS}$ < 18V (0mA to 85mA) | VCC | $V_{VCCnor}$ | 4.9 | | 5.1 | V | C |
| 7.2 | Output voltage $V_{CC}$ at low $V_{VS}$ | 4V < $V_{VS}$ < 5.5V | VCC | $V_{VCClow}$ | $V_{VS} - V_D$ | | 5.1 | V | A |
| 7.3 | Regulator drop voltage | $V_{VS}$ > 4V, $I_{VCC}$ = –20mA | VCC | $V_{D1}$ | | 100 | 200 | mV | A |
| 7.4 | Regulator drop voltage | $V_{VS}$ > 4V, $I_{VCC}$ = –50mA | VCC | $V_{D2}$ | | 300 | 500 | mV | A |
| 7.5 | Regulator drop voltage | $V_{VS}$ > 3.3V, $I_{VCC}$ = –15mA | VCC | $V_{D3}$ | | | 150 | mV | A |
| 7.6 | Line regulation maximum | 5.5V < $V_{VS}$ < 18V | VCC | $VCC_{line}$ | | 0.1 | 0.2 | % | A |
| 7.7 | Load regulation maximum | 5mA < $I_{VCC}$ < 50mA | VCC | $VCC_{load}$ | | 0.1 | 0.5 | % | A |
| 7.8 | Output current limitation | $V_{VS}$ > 5.5V | VCC | $I_{VCClim}$ | | –180 | –120 | mA | A |
| 7.9 | Load capacity | MLC capacitor | VCC | $C_{load}$ | 1.8 | 2.2 | | µF | D |
| 7.10 | VCC undervoltage threshold (NRES ON) | Referred to VCC $V_{VS}$ > 4V | VCC | $V_{VCC_th_uv_down}$ | 4.2 | 4.4 | 4.6 | V | A |
| | VCC undervoltage threshold (NRES OFF) | Referred to VCC $V_{VS}$ > 4V | VCC | $V_{VCC_th_uv_up}$ | 4.3 | 4.6 | 4.8 | V | A |
| 7.11 | Hysteresis of undervoltage threshold | Referred to VCC $V_{VS}$ > 5.5V | VCC | $V_{VCC_hys_uv}$ | 100 | 200 | 300 | mV | A |
| 7.12 | Ramp-up time $V_{VS}$ > 5.5V to VCC = 5V | $C_{VCC}$ = 2.2µF $I_{load}$ = –5mA at VCC | VCC | $t_{VCC}$ | | 1 | 1.5 | ms | A |
| 8 | LIN bus driver: bus load conditions: Load 1 (Small): 1nF, 1kΩ; Load 2 (Large): 10nF, 500Ω; $C_{RXD}$ = 20pF, Load 3 (Medium): 6.8nF, 660Ω characterized on samples 10.7 and 10.8 specifies the timing parameters for proper operation at 20kb/s and 10.9kb/s and 10.10kb/s at 10.4kb/s | | | | | | | | |
| 8.1 | Driver recessive output voltage | Load1/Load2 | LIN | $V_{BUSrec}$ | $0.9 \times V_{VS}$ | | $V_{VS}$ | V | A |
| 8.2 | Driver-dominant voltage | $V_{VS}$ = 7V $R_{load}$ = 500Ω | LIN | $V_{_LoSUP}$ | | | 1.2 | V | A |
| 8.3 | Driver-dominant voltage | $V_{VS}$ = 18V $R_{load}$ = 500Ω | LIN | $V_{_HiSUP}$ | | | 2 | V | A |
| 8.4 | Driver-dominant voltage | $V_{VS}$ = 7V $R_{load}$ = 1000Ω | LIN | $V_{_LoSUP_1k}$ | 0.6 | | | V | A |
| 8.5 | Driver-dominant voltage | $V_{VS}$ = 18V $R_{load}$ = 1000Ω | LIN | $V_{_HiSUP_1k}$ | 0.8 | | | V | A |
| 8.6 | Pull-up resistor to $V_{VS}$ | The serial diode is mandatory | LIN | $R_{LIN}$ | 20 | 30 | 47 | kΩ | A |
| 8.7 | Voltage drop at the serial diodes | In pull-up path with $R_{slave}$ $I_{SerDiode}$ = 10mA | LIN | $V_{SerDiode}$ | 0.4 | | 1.0 | V | D |
| 8.8 | LIN current limitation $V_{BUS}$ = $V_{Bat_max}$ | | LIN | $I_{BUS_LIM}$ | 40 | 120 | 200 | mA | A |
| 8.9 | Input leakage current at the receiver including pull-up resistor as specified | Input leakage current Driver off $V_{BUS}$ = 0V $V_{VS}$ = 12V | LIN | $I_{BUS_PAS_dom}$ | –1 | –0.35 | | mA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 8.10 | Leakage current LIN recessive | Driver off<br>8V < $V_{VS}$ < 18V<br>8V < $V_{BUS}$ < 18V<br>$V_{BUS}$ ≥ $V_{Bat}$ | LIN | $I_{BUS_PAS_rec}$ | | 10 | 20 | µA | A |
| 8.11 | Leakage current when control unit disconnected from ground.<br>Loss of local ground must not affect communication in the residual network | $GND_{Device}$ = $V_{VS}$<br>$V_{VS}$ = 12V<br>0V < $V_{BUS}$ < 18V | LIN | $I_{BUS_NO_gnd}$ | –10 | +0.5 | +10 | µA | A |
| 8.12 | Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition. | $V_{VS}$ disconnected<br>$V_{SUP_Device}$ = GND<br>0V < $V_{BUS}$ < 18V | LIN | $I_{BUS_NO_bat}$ | | 0.1 | 2 | µA | A |
| 8.13 | Capacitance on the LIN pin to GND | | LIN | $C_{LIN}$ | | | 20 | pF | D |
| 9 | LIN bus receiver | | | | | | | | |
| 9.1 | Center of receiver threshold | $V_{BUS_CNT}$ = ($V_{th_dom}$ + $V_{th_rec}$)/2 | LIN | $V_{BUS_CNT}$ | 0.475 × $V_{VS}$ | 0.5 × $V_{VS}$ | 0.525 × $V_{VS}$ | V | A |
| 9.2 | Receiver dominant state | $V_{EN}$ = 5V/3.3V | LIN | $V_{BUSdom}$ | –27 | | 0.4 × $V_{VS}$ | V | A |
| 9.3 | Receiver recessive state | $V_{EN}$ = 5V/3.3V | LIN | $V_{BUSrec}$ | 0.6 × $V_{VS}$ | | 40 | V | A |
| 9.4 | Receiver input hysteresis | $V_{hys}$ = $V_{th_rec}$ – $V_{th_dom}$ | LIN | $V_{BUShys}$ | 0.028 × $V_{VS}$ | 0.1 × $V_{VS}$ | 0.175 × $V_{VS}$ | V | A |
| 9.5 | Pre-wake detection LIN High-level input voltage | | LIN | $V_{LINH}$ | $V_{VS}$ – 2V | | $V_{VS}$ + 0.3V | V | A |
| 9.6 | Pre-wake detection LIN Low-level input voltage | Activates the LIN receiver | LIN | $V_{LINL}$ | –27 | | $V_{VS}$ – 3.3V | V | A |
| 10 | Internal timers | | | | | | | | |
| 10.1 | Dominant time for wake-up via LIN bus | $V_{LIN}$ = 0V | LIN | $t_{bus}$ | 50 | 100 | 150 | µs | A |
| 10.2 | Time delay for mode change from fail-safe mode to normal mode via the EN pin | $V_{EN}$ = 5V/3.3V | EN | $t_{norm}$ | 5 | 15 | 20 | µs | A |
| 10.3 | Time delay for mode change from normal mode to Sleep Mode via the EN pin | $V_{EN}$ = 0V | EN | $t_{sleep}$ | 5 | 15 | 20 | µs | A |
| 10.4 | TXD-dominant time-out time | $V_{TXD}$ = 0V | TXD | $t_{dom}$ | 20 | 40 | 60 | ms | A |
| 10.6 | Time delay for mode change from silent mode to normal mode via the EN pin | $V_{EN}$ = 5V/3.3V | EN | $t_{s_n}$ | 5 | 15 | 40 | µs | A |
| 10.7 | Duty cycle 1 | $TH_{Rec(max)}$ = 0.744 × $V_{VS}$<br>$TH_{Dom(max)}$ = 0.581 × $V_{VS}$<br>$V_{VS}$ = 7.0V to 18V<br>$t_{Bit}$ = 50µs<br>D1 = $t_{bus_rec(min)}$/(2 × $t_{Bit}$) | LIN | D1 | 0.396 | | | | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 10.8 | Duty cycle 2 | $TH_{Rec(min)} = 0.422 \times V_{VS}$<br>$TH_{Dom(min)} = 0.284 \times V_{VS}$<br>$V_{VS}$ = 7.6V to 18V<br>$t_{Bit}$ = 50µs<br>D2 = $t_{bus_rec(max)}/(2 \times t_{Bit})$ | LIN | D2 | | | 0.581 | | A |
| 10.9 | Duty cycle 3 | $TH_{Rec(max)} = 0.778 \times V_{VS}$<br>$TH_{Dom(max)} = 0.616 \times V_{VS}$<br>$V_{VS}$ = 7.0V to 18V<br>$t_{Bit}$ = 96µs<br>D3 = $t_{bus_rec(min)}/(2 \times t_{Bit})$ | LIN | D3 | 0.417 | | | | A |
| 10.10 | Duty cycle 4 | $TH_{Rec(min)} = 0.389 \times V_{VS}$<br>$TH_{Dom(min)} = 0.251 \times V_{VS}$<br>$V_{VS}$ = 7.6V to 18V<br>$t_{Bit}$ = 96µs<br>D4 = $t_{bus_rec(max)}/(2 \times t_{Bit})$ | LIN | D4 | | | 0.590 | | A |
| 10.11 | Slope time falling and rising edge at LIN | $V_{VS}$ = 7.0V to 18V | LIN | $t_{SLOPE_fall}$<br>$t_{SLOPE_rise}$ | 3.5 | | 22.5 | µs | A |
| 10.12 | TXD release time after dominant time-out detection | | TXD | $t_{DTOrel}$ | 10 | | 20 | µs | B |
| 11 | Receiver electrical AC parameters of the LIN physical layer<br>LIN receiver, RXD load conditions: $C_{RXD}$ = 20pF | | | | | | | | |
| 11.1 | Propagation delay of receiver | $V_{VS}$ = 7.0V to 18V<br>$t_{rx_pd} = \max(t_{rx_pdr}, t_{rx_pdf})$ | RXD | $t_{rx_pd}$ | | | 6 | µs | A |
| 11.2 | Symmetry of receiver propagation delay rising edge minus falling edge | $V_{VS}$ = 7.0V to 18V<br>$t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}$ | RXD | $t_{rx_sym}$ | –2 | | +2 | µs | A |
| 12 | WKin pin | | | | | | | | |
| 12.1 | High-level input voltage | | WKin | $V_{WKinH}$ | $V_{VS}$ – 1V | | $V_{VS}$ + 0.3V | V | A |
| 12.2 | Low-level input voltage | Initializes a wake-up signal | WKin | $V_{WKinL}$ | –1 | | $V_{VS}$ – 3.3V | V | A |
| 12.3 | WKin pull-up current | $V_{VS}$ < 28V, $V_{WKin}$ = 0V | WKin | $I_{WKin}$ | –30 | –10 | | µA | A |
| 12.4 | High-level leakage current | $V_{VS}$ = 28V, $V_{WKin}$ = 28V | WKin | $I_{WKinL}$ | –5 | | +5 | µA | A |
| 12.5 | Debounce time of low pulse for wake-up via WKin pin | $V_{WKin}$ = 0V | WKin | $t_{WKin}$ | 50 | 100 | 150 | µs | A |
| 13 | Watchdog oscillator | | | | | | | | |
| 13.1 | Voltage at WDOSC in normal or fail-safe mode | $I_{WD_OSC}$ = –200µA<br>$V_{VS} \geq$ 4V | WDOSC | $V_{WDOSC}$ | 1.13 | 1.23 | 1.33 | V | A |
| 13.2 | Possible values of resistor | Resistor ±1% | WDOSC | $R_{WDOSC}$ | 34 | | 120 | kΩ | D |
| 13.3 | Oscillator period | $R_{WDOSC}$ = 34kΩ | | $t_{OSC}$ | 21.3 | 26.6 | 31.94 | µs | A |
| 13.6 | Oscillator period | $R_{WDOSC}$ = 120kΩ | | $t_{OSC}$ | 68.4 | 85.6 | 102.8 | µs | A |
| 13.7 | Watchdog lead time after reset | | | $t_d$ | | 3948 | | cycles | B |
| 13.8 | Watchdog closed window | | | $t_1$ | | 527 | | cycles | B |
| 13.9 | Watchdog open window | | | $t_2$ | | 553 | | cycles | B |
| 13.10 | Watchdog reset time NRES | | NRES | $t_{nres}$ | 2 | 4 | 6 | ms | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

# 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 14 | Watchdog trigger input Pin NTRIG | | | | | | | | |
| 14.1 | Low-level voltage input | | NTRIG | $V_{NTRIG_L}$ | –0.3 | | $0.3V_{VCC}$ | V | A |
| 14.2 | High-level voltage input | | NTRIG | $V_{NTRIG_H}$ | $0.7V_{VCC}$ | | $V_{VCC}$ + 0.3 | V | A |
| 14.3 | Pull-up resistor | $V_{NTRIG}$ = 0V | NTRIG | $R_{NTRIG}$ | 125 | 250 | 400 | K | A |
| 14.4 | Input leakage current | $V_{NTRIG}$ = $V_{VCC}$ | NTRIG | $I_{NTRIGleakH}$ | | | 1 | µA | A |
| 14.5 | Minimum trigger width | $V_{NTRIG}$ = $V_{VCC}$ | NTRIG | $t_{trig}$ | 200 | | | ns | D |
| 15 | MODE PIN | | | | | | | | |
| 15.1 | Low-level input voltage | | MODE | $V_{MODE_L}$ | –0.3 | | $0.3V_{VCC}$ | V | A |
| 15.2 | High-level input voltage | | MODE | $V_{MODE_H}$ | $0.7V_{VCC}$ | | $V_{VCC}$ + 0.3 | V | A |
| 15.4 | Leakage current | $V_{MODE}$ = 0V or $V_{MODE}$ = $V_{VCC}$ | MODE | $I_{MODE}$ | –3 | | +3 | µA | A |
| 15.5 | MODE pin pull-up current | $V_{MODE}$ = $0.7V_{VCC}$ | MODE | $I_{MODE_PU}$ | –75 | | –5 | µA | A |
| 15.6 | MODE pin pull-down current | $V_{MODE}$ = $0.3V_{VCC}$ | MODE | $I_{MODE_PD}$ | 5 | | 75 | µA | A |
| 16 | Limp Home open drain failure output pin LH | | | | | | | | |
| 16.1 | Output drain-to-source on resistance | Tj = 125°C | LH | $R_{DSon,LH}$ | | | 50 | Ω | A |
| 16.2 | Leakage current | $V_{LH}$ < 40V | LH | $I_{leak,LH}$ | | | 2 | µA | A |
| 17 | HSout pin | | | | | | | | |
| 17.1 | Output drain-to-source on resistance | $I_{HSout}$ = –20mA | HSout | $R_{DSon,HS}$ | | | 20 | Ω | A |
| 17.2 | Leakage current | –0.2V < $V_{HSout}$ < $V_{VS}$+ 0.2V | HSout | $I_{leak,HS}$ | | | 2 | µA | A |
| 17.5 | Switch-off slope (fall time) | $V_{VS}$ = 16V<br>$R_{load}$ = 560Ω<br>$C_{load}$ = 1nF<br>transition from 80% down to 20% of $V_{VS}$ | HSout | $t_{HSslope,fall}$ | 0.75 | | 5 | µs | A |
| 17.6 | Switch-on slope (rise time) | $V_{VS}$ = 16V<br>$R_{load}$ = 560Ω<br>$C_{load}$ = 1nF<br>transition from 20% to 80% of $V_{VS}$ | HSout | $t_{HSslope,rise}$ | 0.75 | | 5 | µs | A |
| 17.7 | Switch-on delay | $V_{VS}$ = 16V<br>$R_{load}$ = 560Ω<br>$C_{load}$ = 1nF<br>time from HSin=HIGH to $V_{HSout}$ = 50% of $V_{VS}$ | HSout | $t_{HSdel}$ | 3 | | 20 | µs | A |
| 17.8 | Switch-off delay | $V_{VS}$ = 16V<br>$R_{load}$ = 560Ω<br>$C_{load}$ = 1nF<br>time from HSin=LOW to $V_{HSout}$ = 50% of $V_{VS}$ | HSout | $t_{HSdel}$ | 3 | | 20 | µs | A |
| 17.9 | Short-circuit detection threshold | | HSout | $V_{SCth_HS}$ | $V_{VS}$ – 6V | | $V_{VS}$ – 2V | V | A |
| 17.10 | Short-circuit deb. time | | HSout | $t_{HS_deb}$ | 2 | | 10 | µs | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

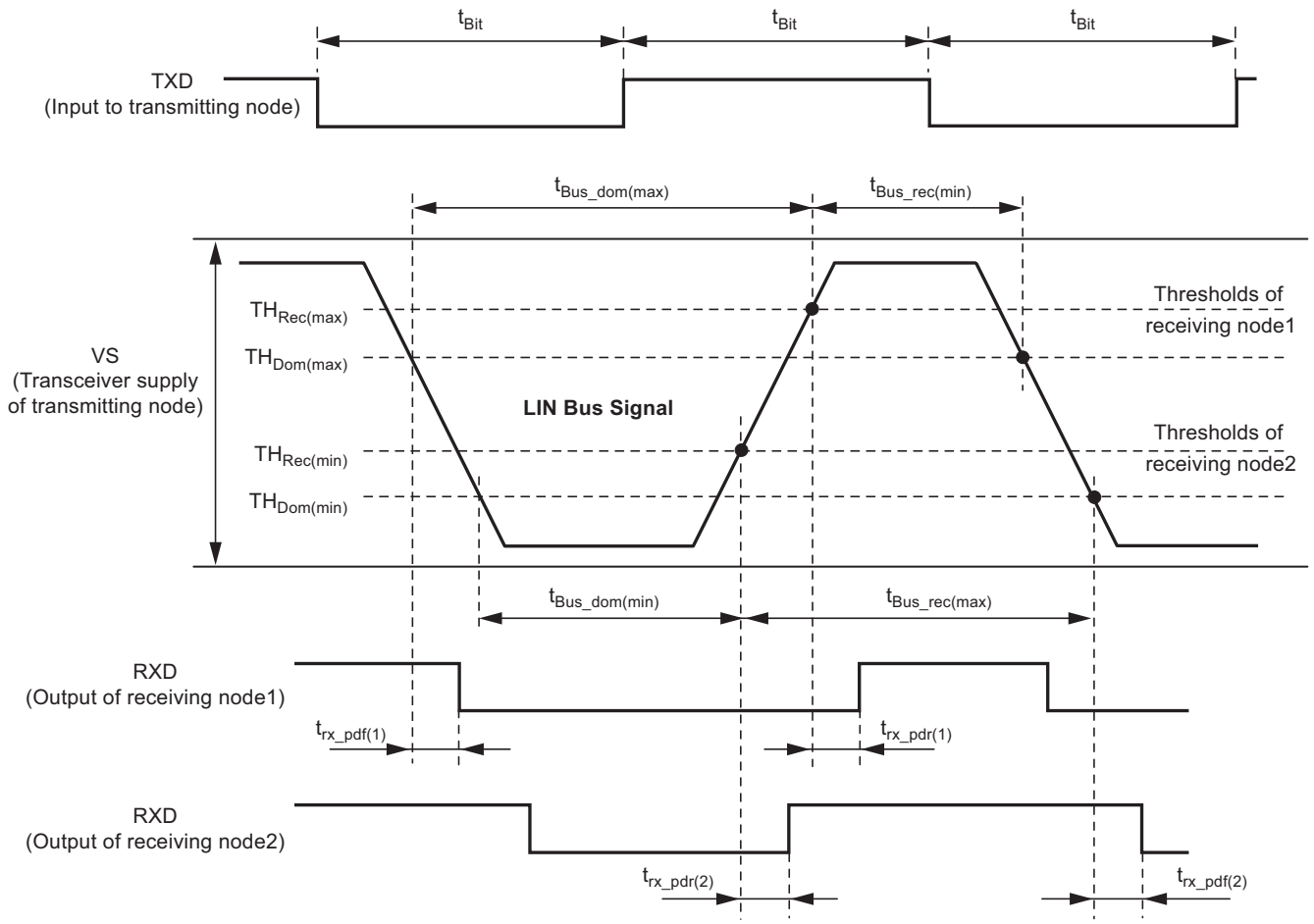
# 7. Electrical Characteristics (Continued)

5V < $V_{VS}$ < 28V, –40°C < $T_j$ < 150°C; unless otherwise specified all values refer to GND pins.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|
| 18 | HSin pin | | | | | | | | |
| 18.1 | Low-level voltage input | | HSin | $V_{HSin_L}$ | –0.3 | | $0.3V_{VCC}$ | V | A |
| 18.2 | High-level voltage input | | HSin | $V_{HSin_H}$ | $0.7V_{VCC}$ | | $V_{VCC}$ + 0.3 | V | A |
| 18.3 | Pull-down resistor | $V_{HSin} = V_{VCC}$ | HSin | $R_{HSin}$ | 50 | 100 | 150 | kΩ | A |
| 18.4 | Low-level input current | $V_{HSin}$ = 0V | HSin | $I_{HSin}$ | –1 | | +1 | µA | A |
| 18.5 | Maximum switching frequency | $R_{load}$ = 560Ω | HSin | $f_{HSin,max}$ | 5 | | | kHz | D |
| 19 | CL15 HV input pin | | | | | | | | |
| 19.1 | High Level input voltage | Positive edge initiates a local wake-up | CL15 | $V_{CL15H}$ | 4 | | | V | A |
| 19.2 | Low level input voltage | | CL15 | $V_{CL15L}$ | –1 | | +2 | V | A |
| 19.3 | Pull-down current | $V_{VS}$ < 28V, $V_{CL15}$ = 28V | CL15 | $I_{CL15}$ | | 50 | 60 | µA | A |
| 19.4 | Internal debounce time | Without external capacitor | CL15 | $t_{dbCL15}$ | 50 | 100 | 150 | µs | A |

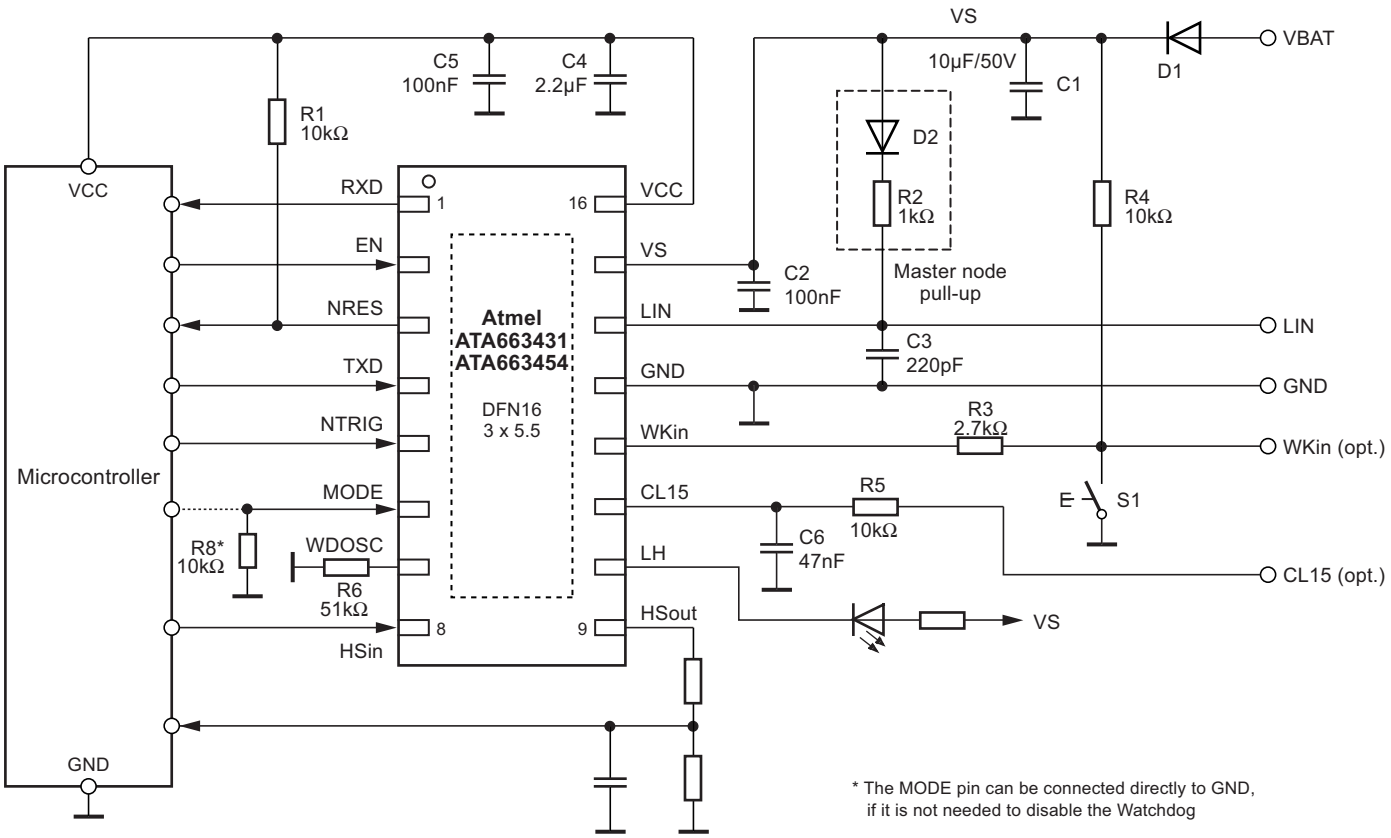
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

**Figure 7-1. Definition of Bus Timing Characteristics**



# 8. Application Circuits

**Figure 8-1. Typical Application Circuit**



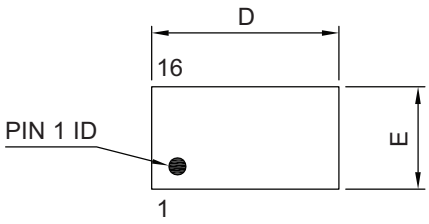

Note: Heat slug must always be connected to GND.

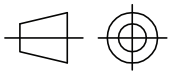
# 9. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| ATA663431-GDQW | DFN16 | 3.3V LIN system basis chip, Pb-free, 6k, taped and reeled |
| ATA663454-GDQW | DFN16 | 5V LIN system basis chip, Pb-free, 6k, taped and reeled |

# 10. Package Information

**Top View**



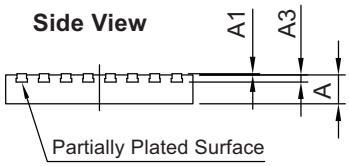



technical drawings
according to DIN
specifications

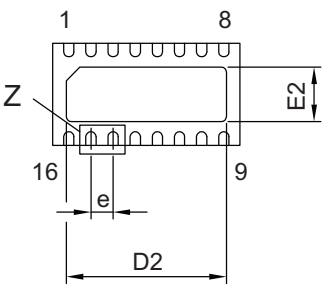
Dimensions in mm

Two Step Singulation process

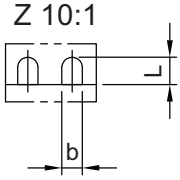
**Side View**




**Bottom View**




Z 10:1




| COMMON DIMENSIONS (Unit of Measure = mm) | | | | |
|---|---|---|---|---|
| **Symbol** | **MIN** | **NOM** | **MAX** | **NOTE** |
| A | 0.8 | 0.85 | 0.9 | |
| A1 | 0.0 | 0.035 | 0.05 | |
| A3 | 0.16 | 0.21 | 0.26 | |
| D | 5.4 | 5.5 | 5.6 | |
| D2 | 4.6 | 4.7 | 4.8 | |
| E | 2.9 | 3 | 3.1 | |
| E2 | 1.5 | 1.6 | 1.7 | |
| L | 0.35 | 0.4 | 0.45 | |
| b | 0.25 | 0.3 | 0.35 | |
| e | | 0.65 | | |

10/11/13

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Atmel **Package Drawing Contact:** packagedrawings@atmel.com | **Package: VDFN_5.5x3_16L**<br>Exposed pad 4.7x1.6 | | 6.543-5168.01-4 | 1 |

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