

512Kx8 Static RAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
 - Access time of 20 ns
- Low active power
 - 1.93W (max.)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs
- Low profile
 - Max. height of 0.34 inches

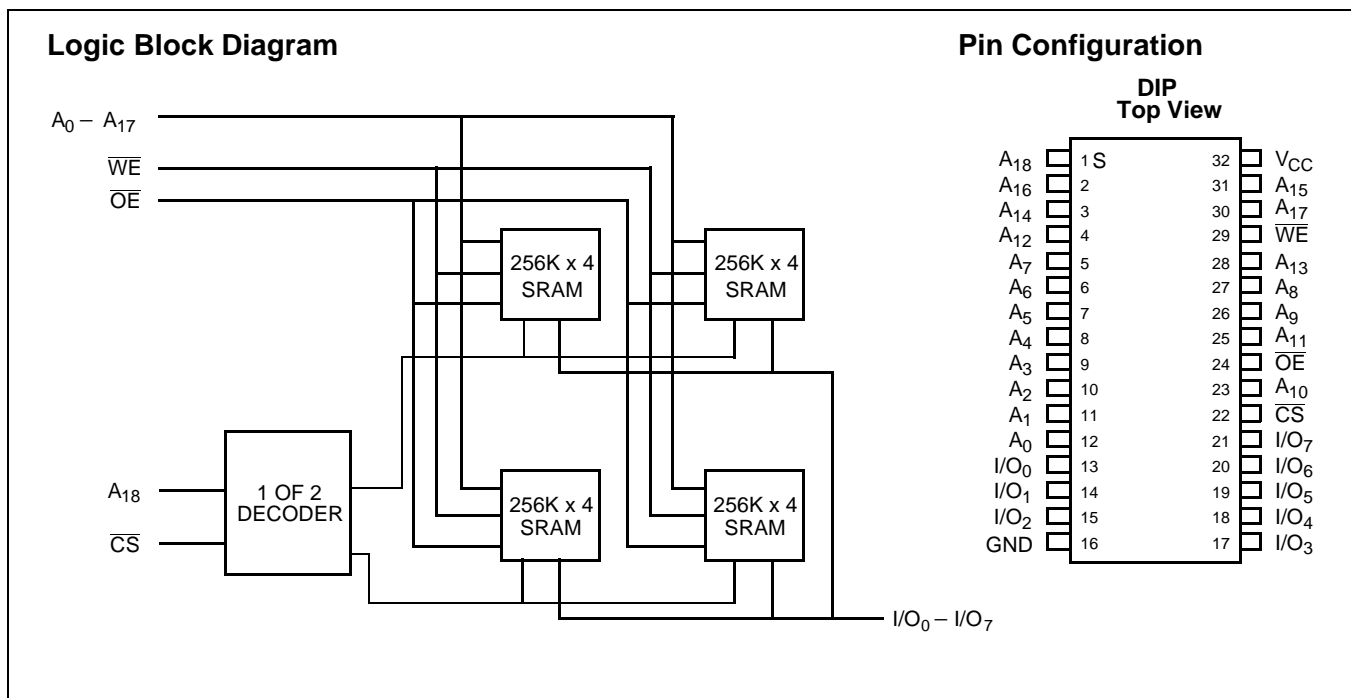
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is

constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable (\overline{OE}) LOW, while write enable (\overline{WE}) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.



Selection Guide

| | 1464-20 | 1464-22 | 1464-25 | 1464-30 | 1464-35 | 1464-45 | 1464-55 |
|--------------------------------|---------|---------|---------|---------|---------|---------|---------|
| Maximum Access Time (ns) | 20 | 22 | 25 | 30 | 35 | 45 | 55 |
| Maximum Operating Current (mA) | 350 | 350 | | 300 | | 300 | |
| Maximum Standby Current (mA) | 240 | 240 | | 240 | | 240 | |

Maximum Ratings

(Above which the useful life may be impaired.)

| | |
|--|-----------------|
| Storage Temperature | -55°C to +125°C |
| Ambient Temperature with Power Applied..... | -10°C to +85°C |
| Supply Voltage to Ground Potential | -0.5V to +7.0V |
| DC Voltage Applied to Outputs in High Z State..... | -0.5V to +7.0V |
| DC Input Voltage | -0.5V to +7.0V |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |

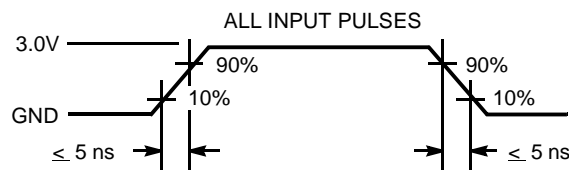
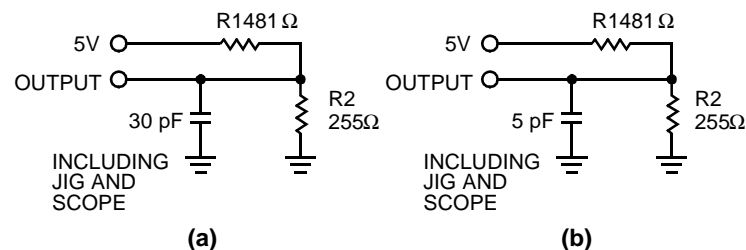
Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 1464-20, 22, 25 | | 1464-30, 35, 45, 55 | | Unit |
|------------------|--|---|-----------------|----------------------|---------------------|----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} +0.3 | 2.2 | V _{CC} +0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -10 | +10 | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -10 | +10 | -10 | +10 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL} | | 350 | | 300 | mA |
| I _{SB1} | Automatic CS Power-Down Current | V _{CC} = Max., CS ≥ V _{IH} , Min. Duty Cycle = 100% | | 240 | | 240 | mA |
| I _{SB2} | Automatic CS Power-Down Current | V _{CC} = Max., CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | | 60 | | 60 | mA |

Capacitance^[2]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 40 | pF |
| C _{OUT} | Output Capacitance | | 30 | pF |

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:

- V_{IL} (min.) = -3.0V for pulse widths less than 20 ns.
- Tested on a sample basis.

Switching Characteristics Over the Operating Range^[3]

| Parameter | Description | 1464-20 | | 1464-22 | | 1464-25 | | 1464-30 | | Unit |
|-----------------------------------|--|---------|------|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 20 | | 22 | | 25 | | 30 | | ns |
| t _{AA} | Address to Data Valid | | 20 | | 22 | | 25 | | 30 | ns |
| t _{OHA} | Data Hold from Address Change | 5 | | 5 | | 5 | | 5 | | ns |
| t _{ACS} | $\overline{\text{CS}}$ LOW to Data Valid | | 20 | | 22 | | 25 | | 30 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to Data Valid | | 13 | | 13 | | 15 | | 15 | ns |
| t _{LZOE} | $\overline{\text{OE}}$ LOW to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | $\overline{\text{OE}}$ HIGH to High Z | 0 | 10 | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| t _{LZCS} | $\overline{\text{CS}}$ LOW to Low Z | 5 | | 5 | | 5 | | 10 | | ns |
| t _{HZCS} | $\overline{\text{CS}}$ HIGH to High Z ^[4] | 0 | 15 | 0 | 15 | 0 | 15 | 0 | 20 | ns |
| WRITE CYCLE ^[5] | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 20 | | 22 | | 25 | | 30 | | ns |
| t _{SCS} | $\overline{\text{CS}}$ LOW to Write End | 15 | | 17 | | 20 | | 25 | | ns |
| t _{AW} | Address Set-Up to Write End | 15 | | 15 | | 20 | | 25 | | ns |
| t _{HA} | Address Hold from Write End | 3 | | 3 | | 3 | | 3 | | ns |
| t _{SA} | Address Set-Up to Write Start | 5 | | 5 | | 5 | | 5 | | ns |
| t _{PWE} | $\overline{\text{WE}}$ Pulse Width | 15 | | 15 | | 15 | | 20 | | ns |
| t _{SD} | Data Set-Up to Write End | 12 | | 12 | | 15 | | 15 | | ns |
| t _{HD} | Data Hold from Write End | 2 | | 2 | | 2 | | 2 | | ns |
| t _{LZWE} | $\overline{\text{WE}}$ HIGH to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| t _{HZWE} | $\overline{\text{WE}}$ LOW to High Z ^[4] | | 15 | | 15 | | 15 | | 15 | ns |

Switching Characteristics Over the Operating Range ^[3]

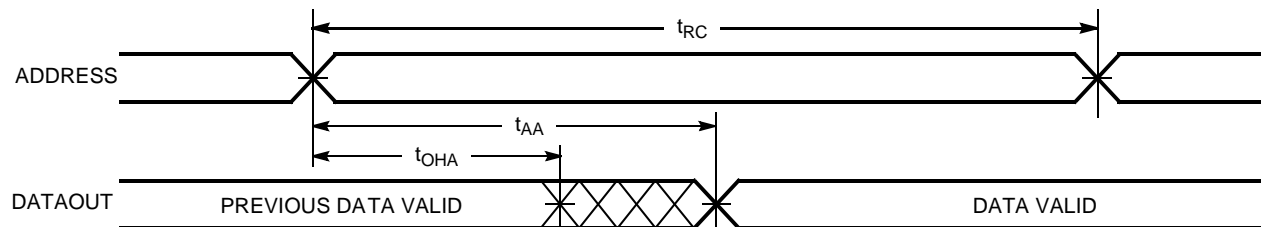
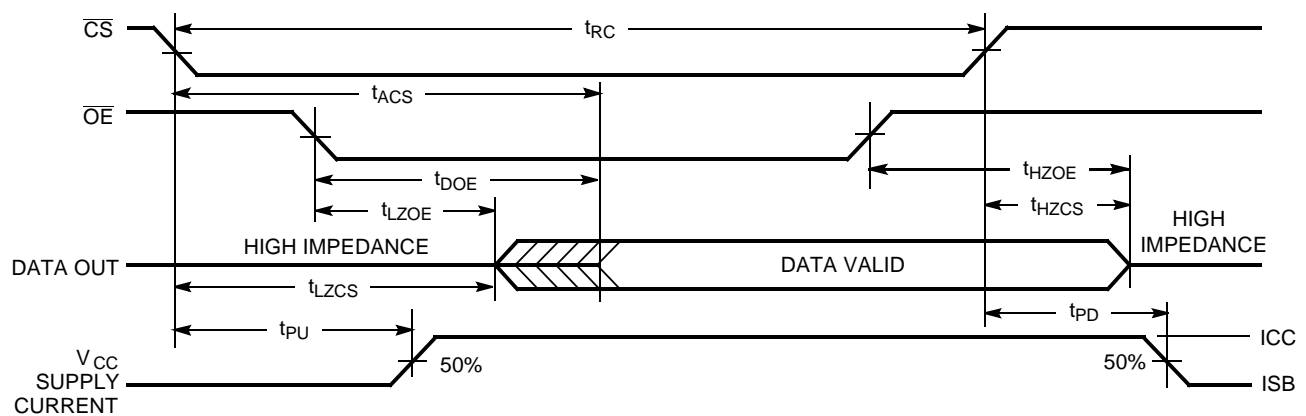
| Parameter | Description | 1464-35 | | 1464-45 | | 1464-55 | | Unit |
|-------------------|--|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 35 | | 45 | | 55 | | ns |
| t _{AA} | Address to Data Valid | | 35 | | 45 | | 55 | ns |
| t _{OHA} | Data Hold from Address Change | 5 | | 5 | | 5 | | ns |
| t _{ACS} | $\overline{\text{CS}}$ LOW to Data Valid | | 35 | | 45 | | 55 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to Data Valid | | 20 | | 25 | | 30 | ns |
| t _{LZOE} | $\overline{\text{OE}}$ LOW to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | $\overline{\text{OE}}$ HIGH to High Z | 0 | 15 | 0 | 15 | 0 | 15 | ns |
| t _{LZCS} | $\overline{\text{CS}}$ LOW to Low Z | 10 | | 10 | | 10 | | ns |
| t _{HZCS} | $\overline{\text{CS}}$ HIGH to High Z ^[4] | 0 | 20 | 0 | 20 | 0 | 20 | ns |

Notes:

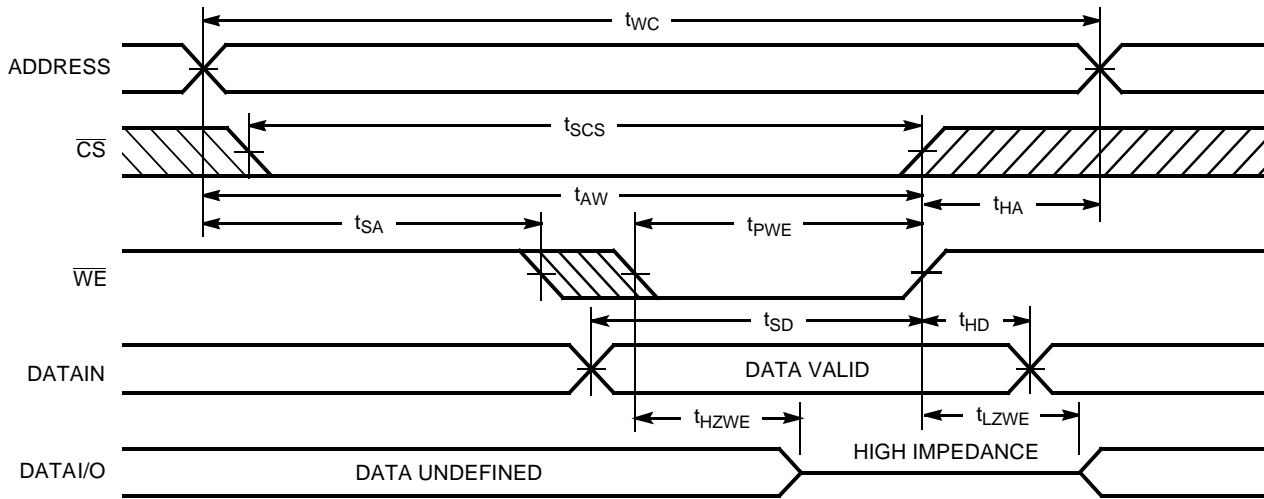
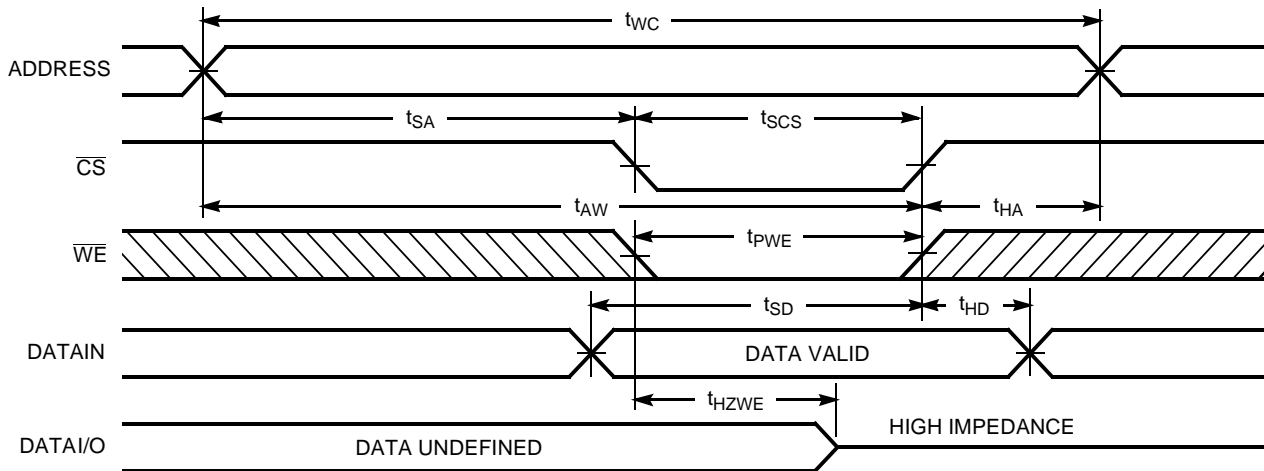
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)^[3]

| Parameter | Description | 1464-35 | | 1464-45 | | 1464-55 | | Unit |
|----------------------------------|--|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE^[5] | | | | | | | | |
| t_{WC} | Write Cycle Time | 35 | | 45 | | 55 | | ns |
| t_{SCS} | \overline{CS} LOW to Write End | 30 | | 40 | | 50 | | ns |
| t_{AW} | Address Set-Up to Write End | 30 | | 40 | | 50 | | ns |
| t_{HA} | Address Hold from Write End | 3 | | 3 | | 3 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 25 | | 35 | | 40 | | ns |
| t_{SD} | Data Set-Up to Write End | 20 | | 25 | | 35 | | ns |
| t_{HD} | Data Hold from Write End | 2 | | 3 | | 3 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z | 0 | | 0 | | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[4] | | 15 | | 15 | | 20 | ns |

Switching Waveforms
Read Cycle No. 1^[6,7]

Read Cycle No. 2^[6,8]

Notes:

6. \overline{WE} is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{LL}$.
8. Address valid prior to or coincident with \overline{CS} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled)^[5]

Write Cycle No. 2 (\overline{CS} Controlled)^[5,9]

Note:

9. If \overline{CS} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Truth Table

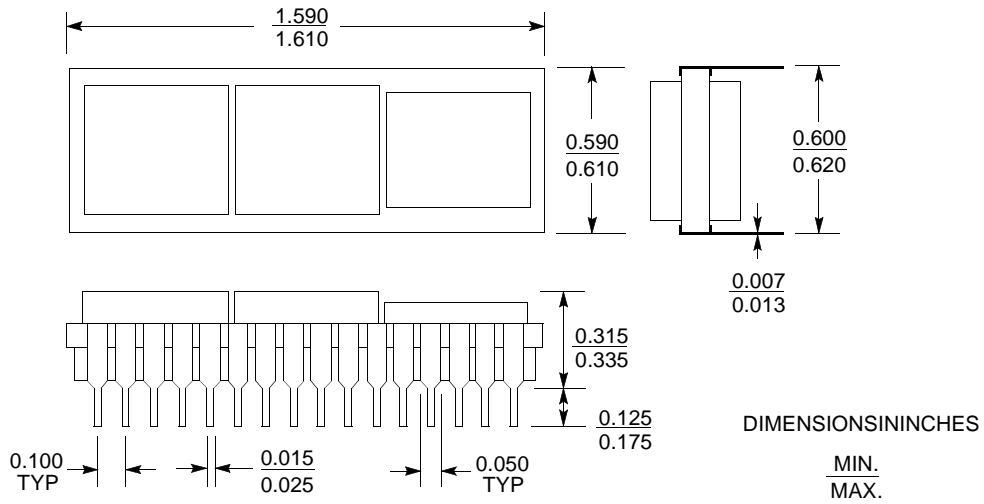
| CS | WE | OE | Input/Output | Mode |
|----|----|----|--------------|---------------------|
| H | X | X | High Z | Deselect/Power-Down |
| L | H | L | Data Out | Read Word |
| L | L | X | Data In | Write Word |
| L | H | H | High Z | Deselect |

Ordering Information

| Speed (ns) | Ordering Code | Package Type | Package Type | Operating Range |
|------------|---------------|--------------|-------------------|-----------------|
| 20 | CYM1464PD-20C | PD02 | 32-Pin DIP Module | Commercial |
| 22 | CYM1464PD-22C | PD02 | 32-Pin DIP Module | Commercial |
| 25 | CYM1464PD-25C | PD02 | 32-Pin DIP Module | Commercial |
| 30 | CYM1464PD-30C | PD02 | 32-Pin DIP Module | Commercial |
| 35 | CYM1464PD-35C | PD02 | 32-Pin DIP Module | Commercial |
| 45 | CYM1464PD-45C | PD02 | 32-Pin DIP Module | Commercial |
| 55 | CYM1464PD-55C | PD02 | 32-Pin DIP Module | Commercial |

Package Diagrams

32-Pin DIP Module PD02



| Document Title: CYM1464 512K x 8 Static RAM Module Document Number: 38-05272 | | | | |
|---|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 114173 | 3/19/02 | DSG | Change from Spec number: 38-M-00030 to 38-05272 |