# AN11675

## GreenChip TEA1833(L)TS fixed frequency flyback controller

Rev. 1 — 20 July 2015 Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | GreenChip, TEA1833(L)TS, SMPS, flyback, adapter, notebook, ultralight notebook, LCD TV, LCD monitors |
| **Abstract** | The TEA1833(L)TS is a low-cost member of the GreenChip family in a very small package. It is a fixed-frequency flyback controller, especially suited for medium-power applications, such as ultralight notebook, notebooks, printers, LCD TVs, and LCD monitors.<br>No-load power can be as low as 55 mW at 230 V (AC).<br>Delivery of 200 % peak power for short periods is possible.<br>Because of a reduced switching frequency, efficiency also remains high at low load. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| v.1 | 20150720 | first issue |

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# 1. General description

The TEA1833(L)TS is a fixed-frequency flyback controller that can be used for Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Despite the very small TSOP6 package, it almost has the full functionality of the TEA1738 series.

## 1.1 Scope

This application note describes the functionality of the TEA1833(L)TS series. Fixed-frequency flyback fundamentals and calculation of transformer and other large signal parts are not dealt with in this document.

## 1.2 Features

### 1.2.1 Power features

- SMPS controller IC enabling low-cost applications
- Small low-cost TSOP6 package
- Fixed switching frequency with frequency jitter to reduce ElectroMagnetic Interference (EMI)
- Frequency reduction with fixed minimum peak current to maintain high efficiency and low output ripple at low-power output levels
- Peak power operation in CCM, increased peak current (1.4 times) and switching frequency (2 times)
- Slope compensation for CCM operation
- Integrated soft start
- High/low line compensation for constant overpower protection level
- Wide $V_{CC}$ voltage range (10.5 V to 36 V)

### 1.2.2 Green features

- No-load power consumption < 55 mW at 230 V (AC) possible for 65 W applications.
- Very low supply current during start and restart (11 μA typical) enabling the use of a high-ohmic start-up resistor.
- Burst mode when the voltage on the VCC pin drops to the burst threshold level (just above UnderVoltage LockOut (UVLO) level) to prevent a restart during prolonged no switching. It enables using a small $V_{CC}$ capacitor and a high-ohmic start-up resistor.
- Low supply current during normal operation (0.58 mA typical).
- Frequency reduction at low load to maintain high efficiency at low load


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### 1.2.3 Protection features

- Accurate OverVoltage Protection (OVP) via the ISENSE pin
- OverVoltage Protection on the VCC supply pin
- UnderVoltage LockOut (UVLO) on the VCC supply pin
- Internal OverTemperature Protection (OTP)
- External OverTemperature Protection (OTP) using 100 kΩ NTC resistor
- Overpower time-out: 27.5 ms (TEA1833TS); 160 ms (TEA1833LTS)
- Overpower time-out during output short circuit conditions, reducing the average input power: 14.5 ms (TEA1833TS only)
- Restart timer after an overpower condition for low average input power at overload and short circuit (TEA1833TS only)
- Output Short Circuit Protection (OSCP) to prevent transformer saturation during start-up, overload events or short circuit events
- Maximum frequency limitation at high mains to prevent unnecessary high voltage on drain of MOSFET
- Brownin and brownout protection to avoid operation during mains undervoltage conditions
- Maximum duty cycle protection for $\delta > 90$ %

## 1.3 Applications

The TEA1833(L)TS is intended for applications that require an efficient and cost-effective power supply solution. It is especially suited for medium-power applications like:

- Ultrabooks and notebooks
- LCD TVs and LCD monitors
- Printers

## 1.4 Differences between the TEA1833 and the TEA1738 series

- Smaller package (TSOP6):
- The VINSENSE pin has been removed. The functionality has been combined on the PROTECT pin with the external overtemperature protection.
- The OPTIMER pin has been removed. The functionality has been integrated:
  - Internal overpower time-out: 27.5 ms (TEA1833TS); 160 ms (TEA1833LTS); external timing components no longer required.
  - Internal restart timer; extra external components for time constant no longer required.
- Increased rating of the VCC clamp (1 mA instead of 730 μA).
- Extra filtering on latched protections:
  - Latched protection can only be triggered if a fault condition lasts at least four consecutive switching cycles or measuring cycles (external OTP).
  - Low-pass filtering provides immunity against high-frequency signals, for example, from mobile phones.


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- Fixed frequency operation with frequency jitter for simple EMI filtering (no frequency reduction for lower power).
- Maximum duty cycle protection modified:

  In the TEA1738 series, the maximum on-time protection is only active during peak power conditions ($V_{ctrl(Ipeak)}$ > 400 mV). This restriction has been removed because of the new frequency control implementation. The maximum duty cycle is increased from 80 % to 90 %.
- VCC range increased to 10.5 V to 36 V (was 12 V to 30 V).
- New features:
  - Burst mode when the voltage on the VCC pin drops to below the burst threshold level (just above UVLO) preventing restart during prolonged no switching. It enables using a small VCC capacitor and a high-ohmic start-up resistor.
  - Output Short Circuit Protection (OSCP) to prevent transformer saturation at start-up, overload events, and short circuit events.

## 1.5 Differences between the TEA1833 and the TEA1733 series

- Smaller package (TSOP6):
- The VINSENSE pin has been removed. The functionality has been partly combined on the PROTECT pin with the external OTP. The mains OVP function does not exist in the TEA1833(L)TS anymore:
- The OPTIMER pin has been removed. The functionality has been integrated:
  - Internal overpower time-out: 27.5 ms (TEA1833TS); 160 ms (TEA1833LTS); external timing components no longer required
  - Internal restart timer; extra external components for time constant no longer required
- Internal OverVoltage Protection (OVP) added. If the VCC pin exceeds 36 V, the latched protection mode is triggered
- Increased rating of the VCC clamp (1 mA instead of 240 μA)
- Extra filtering on latched protections:
  - Latched protection can only be triggered if a fault condition lasts at least four consecutive switching cycles or measuring cycles (external OTP)
  - Low-pass filtering provides immunity against high-frequency signals; for example, from mobile phones
- Maximum duty cycle protection added; when 8 cycles $\delta$ > 90 %, the restart protection is activated
- Fixed frequency operation with frequency jitter for simple EMI filtering (no frequency reduction for lower power, as with the TEA1733)
- Increased switching frequency during peak load allowing more output power with the same core
- New features:
  - Burst mode when the voltage on the VCC pin drops to below the burst threshold level (just above UVLO) preventing restart during prolonged no switching. It enables using a small VCC capacitor and a high-ohmic start-up resistor


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  - Output Short Circuit Protection (OSCP) to prevent transformer saturation at start-up, overload events, and short circuit events
- Latch version (TEA1833LTS) only:

  UnderVoltage LockOut (UVLO) has changed to latched protection. It ensures that a shorted output always triggers the latched protection when $V_{CC}$ drops below $V_{th(UVLO)}$ before the overpower protection has a chance to respond.

## 1.6 Differences between TEA1833 and TEA1832

- Higher efficiency at 25 % load because of reduced switching frequency
- Improved slope compensation
- Maximum frequency limitation at high mains

## 1.7 Latch and safe restart version

The TEA1833(L)TS is available in a restart version and a latch version. The only differences between the two versions are the overpower time-out and how the OverPower Protection (OPP) and UnderVoltage LockOut (UVLO) events are handled:

- TEA1833TS: Overpower time-out = 27.5 ms, OPP, or UVLO event initiates safe restart
- TEA1833LTS: Overpower time-out = 160 ms, OPP, or UVLO event sets the IC to the latched off-state

See Section 3.4 for more detailed information about these protection features.


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## 1.8 Application diagram

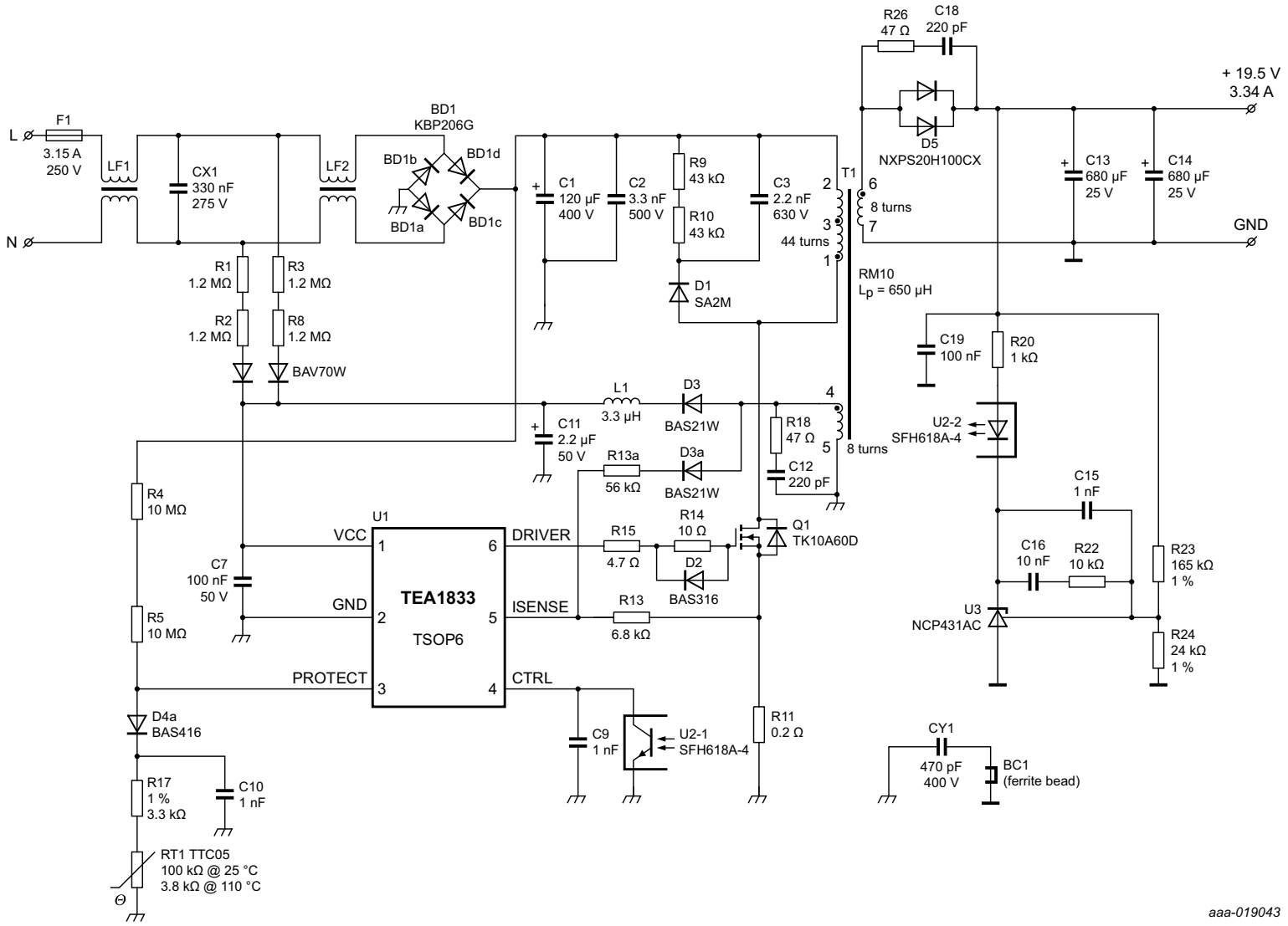



**Fig 1. TEA1833(L)TS application diagram - 65 W**



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# 2. Pinning

## 2.1 Pinning diagram

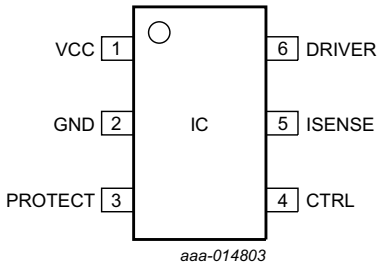



**Fig 2. Pinning diagram**

## 2.2 Pin description

**Table 1. Pin description**

| Pin number | Pin name | Description |
|---|---|---|
| 1 | VCC | **supply voltage**<br>**start-up**<br>At mains switch-on, an external start-up circuit (usually a passive resistor network) charges the capacitor connected to this pin.<br>When $V_{CC}$ exceeds $V_{startup}$ (= 22 V typical), the IC wakes up from power-down mode and checks if all other conditions are met to start switching.<br>**undervoltage lockout**<br>When the voltage on the pin drops below the 10.5 V (typical; the stop voltage ($V_{th(UVLO)}$)), the IC stops switching and restarts (TEA1833TS) or latches (TEA1833LTS).<br>**burst mode**<br>When no protection is active and the voltage on the pin drops to below 11.1 V ($V_{th(burst)}$), two strokes are initiated with minimal $I_{pk}$. These strokes keep the VCC capacitor charged and prevent a restart.<br>**latch reset and clamp**<br>During latched protection, this pin is internally clamped to just above the 4.5 V latch reset voltage ($V_{rst(latch)}$), enabling fast latch reset after unplugging the mains.<br>**internal overvoltage protection**<br>An internal OVP sets the IC to latched off-state when the voltage on pin VCC exceeds 36 V (typical) for four consecutive switching cycles. |
| 2 | GND | **ground** |


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**Table 1. Pin description**

| Pin number | Pin name | Description |
|---|---|---|
| 3 | PROTECT | **protection input**<br>Two independent protection features are combined on this pin. Both functions are alternatively activated for 500 μs.<br>**mains detection input**<br>During mains detection, the PROTECT pin is clamped to 0.25 V (no interference with OTP network due to used diode). It measures the current from a high-ohmic resistor, connected to the mains electrolytic capacitor. The measured current is used to realize the brownin and brownout functions and the High/low line compensation for the overpower protection.<br>**external OverTemperature Protection (OTP)**<br>For OTP, a diode in series with an NTC resistor is connected to ground. During OTP detection, a current of 200 μA flows out the pin via a diode and NTC to the ground. The voltage is measured. When it is four consecutive measuring cycles below $V_{det(PROTECT)}$ (2 V typical), the OTP protection is activated. |
| 4 | CTRL | **power control input**<br>**general**<br>The voltage on the CTRL pin controls both the switching frequency and the peak current.<br>**input configuration**<br>The input is internally connected to 5.4 V via a 26 kΩ resistor.<br>**range**<br>The active range of pin CTRL is from 1.45 V (no load) to 4.5 V (maximum peak load). |
| 5 | ISENSE | **current sense input**<br>**general**<br>This pin senses the primary coil current across an external resistor. It compares this coil current to an internal control voltage ($V_{ctrl(Ipeak)}$) which is proportional to the voltage on the CTRL pin. It switches off the MOSFET when the level is reached.<br>**propagation delay**<br>The delay time from detecting the level to actually switching off the driver is approximately 150 ns.<br>**leading-edge blanking**<br>During the first 325 ns of each switching cycle, the ISENSE input is internally blanked to prevent that spikes, due to parasitic capacitance, prematurely trigger the peak current comparator.<br>**overpower protection**<br>When the internal $I_{peak}$ control voltage ($V_{ctrl(Ipeak)}$) exceeds 400 mV, the overpower timer is started. When this condition lasts longer than 27.5 ms (TEA1833TS)/160 ms (TEA1833LTS), the IC triggers a long restart (TEA1833TS) or enters the latched protection mode (TEA1833LTS).<br>**overcurrent protection**<br>The internal control voltage is limited to 575 mV, which limits the primary peak current and thus the input power. |


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**Table 1. Pin description**

| Pin number | Pin name | Description |
|---|---|---|
| | | **Output Short Circuit Protection (OSCP)**<br>To prevent transformer saturation in CCM during start-up, overload events, or short circuit events, the switching frequency is lowered when the CTRL voltage exceeds 2.85 V (above nominal power level) and the measured level on the ISENSE pin is above 400 mV ($V_{th(sense)opp}$) within 1 μs after turn-on of the driver output.<br>**high/low line compensation**<br>A current, proportional to the measured current at the mains detect (see the PROTECT pin) flows out of the ISENSE pin. When connecting a resistor between the ISENSE pin and the $R_{sense}$ resistor, a proportional DC voltage is deducted from the $R_{sense}$ voltage generated by $I_{peak}$.The decreased level keeps the OPP level constant.<br>**overvoltage protection output voltage**<br>During the secondary stroke, the voltage on the auxiliary winding (which is related to the secondary winding voltage) is sensed using a diode and a resistor in series connected from the auxiliary winding to the ISENSE pin. When the measured voltage surpasses 2.5 V for four consecutive switching cycles, the latched protection is triggered.<br>**soft start**<br>A built-in soft start function slowly enables the primary peak current to grow.<br>**slope compensation**<br>The amount of slope compensation (related to the ISENSE pin): 18 mV/μs. The slope compensation is only active at duty cycles higher than 45 %. |
| 6 | DRIVER | **gate driver output for MOSFET**<br>**driver capability**<br>The driver can source and sink 0.3 A at 2 V. It can sink 0.75 A at 10 V.<br>**frequency modulation**<br>The switching frequency is modulated over a range of ±4 kHz at a rate of 260 Hz to improve EMI behavior. |


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# 3. Functional description

## 3.1 General

The TEA1833(L)TS has been designed for fixed-frequency flyback power supplies.

The TEA1833(L)TS uses peak current control. The output voltage is measured and transferred back via an optocoupler to the CTRL pin.

This chapter describes how the controller works. See Section 4 for specific application issues.

## 3.2 Start-up

### 3.2.1 Charging the VCC capacitor

To provide the start-up power, a resistor charges capacitor C11 (see Figure 1) on the VCC pin. When $V_{CC}$ is below $V_{startup}$ (22 V typical), the IC current consumption is low (11 μA typical). When the capacitor is charged above $V_{startup}$ and all other conditions have been met, the controller starts to switch. When the switching has started, the TEA1833(L)TS is supplied by the auxiliary winding.

Connect the resistor in front of the bridge rectifier for fast latch reset[1].

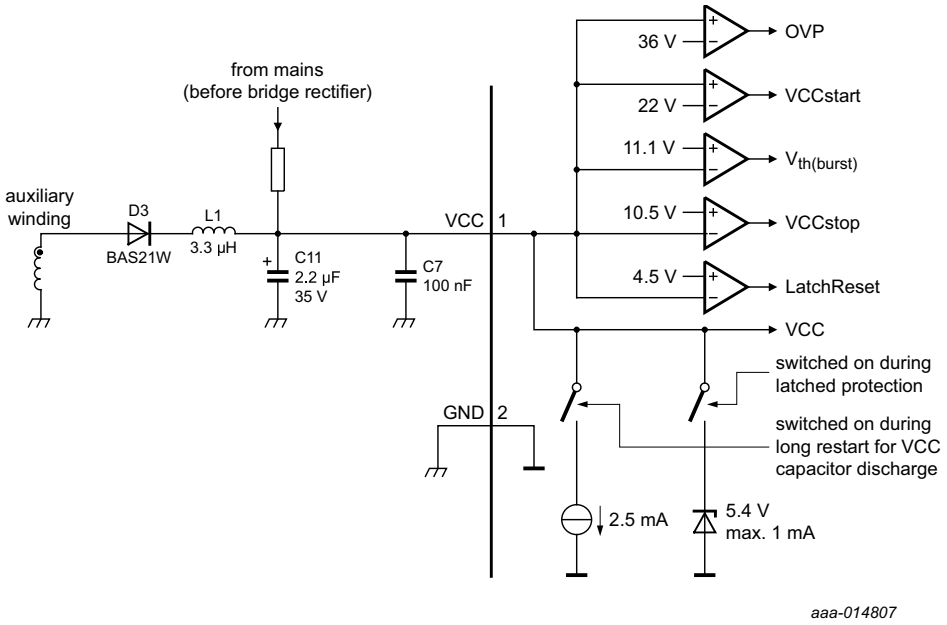



**Fig 3. VCC pin**

1. The only way to reset the latched protection is to bring the VCC pin below 4.5 V. During latched protection, the supply current is ≤ 15 μA. If the start-up resistor is connected after the bridge rectifier, the bulk capacitor continues to feed it for a long time after unplugging the mains.


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A low-cost and efficient implementation for the start-up circuit is using two resistors in series with a low voltage diode to L and N. The resistors also discharge the X-capacitor (CX1) after the mains has been unplugged (see Figure 1). See Section 5 for more information about the start-up circuit.

### 3.2.2 Start-up conditions

When the VCC pin reaches $V_{startup}$ (22 V typical), the controller wakes up from power-down mode and checks the PROTECT pin. The PROTECT pin cycles between mains voltage detection and external OverTemperature Protection (OTP). If during mains voltage detection the brownin level is not met, switching is not started. The IC waits until the brownin level is reached. If during OverTemperature Detection (ODT) the level on the external NTC is too low, switching is not started. The IC waits until the voltage on the PROTECT pin surpasses the $V_{det(PROTECT)}$ level (2 V typical). Due to the waking up, the supply current increases. When switching does not start, $V_{CC}$ drops to below $V_{th(UVLO)}$. The IC enters power-down mode. The start-up circuit charges the VCC capacitor and the cycle repeats itself.

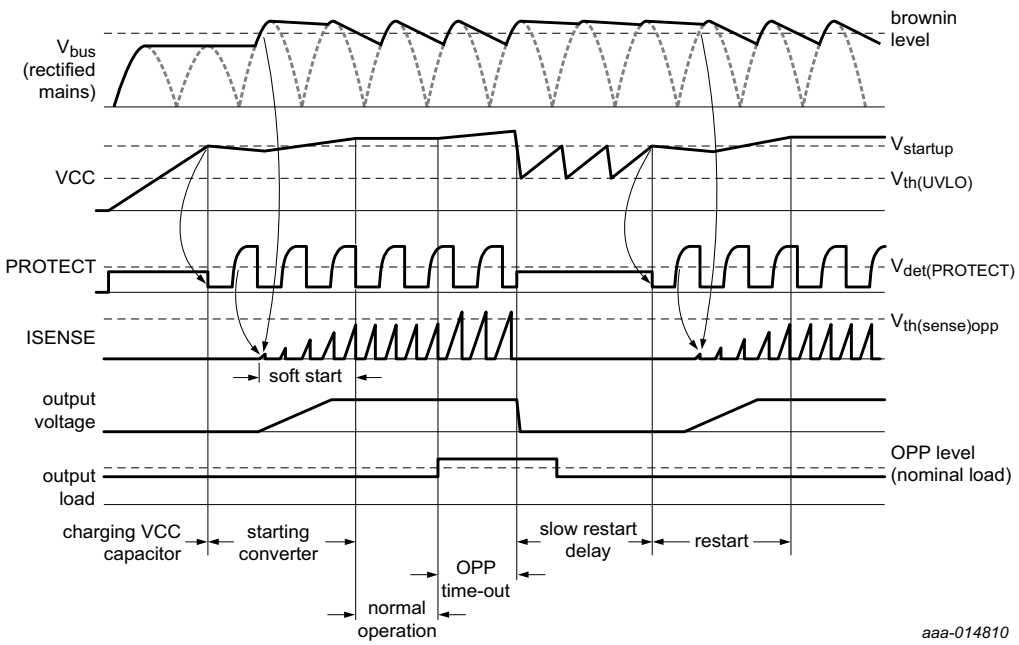



**Fig 4. Start-up sequence, normal operation and restart sequence**

### 3.2.3 Soft start

Only when both brownin and the OTP level are correct, the internal soft start is initiated.

During soft start, the $V_{ctrl(Ipeak)}$ level (level at the ISENSE pin where the MOSFET is switched off) increases from 0 mV to 575 mV within 3.6 ms. The increase causes the peak current to increase gradually. The switching frequency is at the maximum (130 kHz).

The purpose of the soft start feature is to avoid audible noise at start-up. Increasing the peak current instantly from 0 to the maximum is audible.


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### 3.2.4 Clamp

The 5.4 V clamp on the VCC pin is only active during the latched off-state (see Figure 3). The purpose of this clamp is to keep the VCC pin just above the 4.5 V latch reset level, ensuring a fast latch reset after unplugging the mains.

## 3.3 Power control

### 3.3.1 General

The CTRL pin controls the amount of output power by changing both the peak current and the switching frequency (see Figure 5).

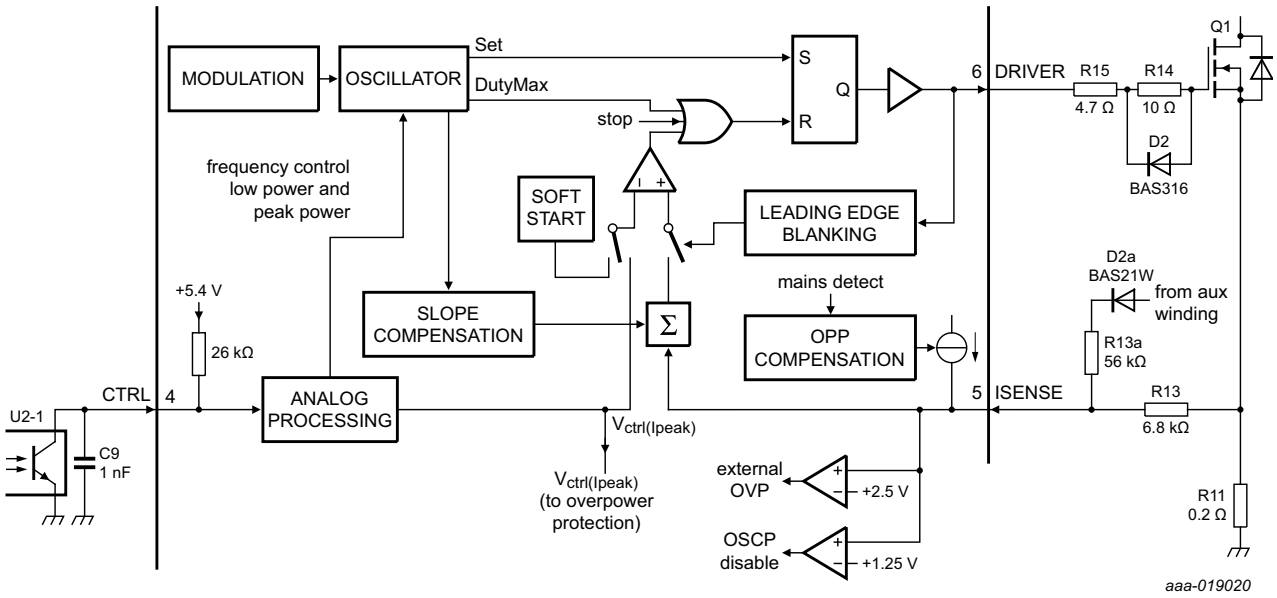



**Fig 5. CTRL, ISENSE, and DRIVER pins**

### 3.3.2 Input biasing

An internal 26 kΩ resistor connected to 5.4 V enables direct connection of an optocoupler transistor. External components to convert the output current of the optocoupler to the control voltage are not required. The relationship between the current and the voltage on the CTRL pin can be calculated with Equation 1 (see Figure 6).

$$V_{CTRL} = 5.4\ V - 26 \times 10^{3} \times I_{O(CTRL)} \quad (1)$$


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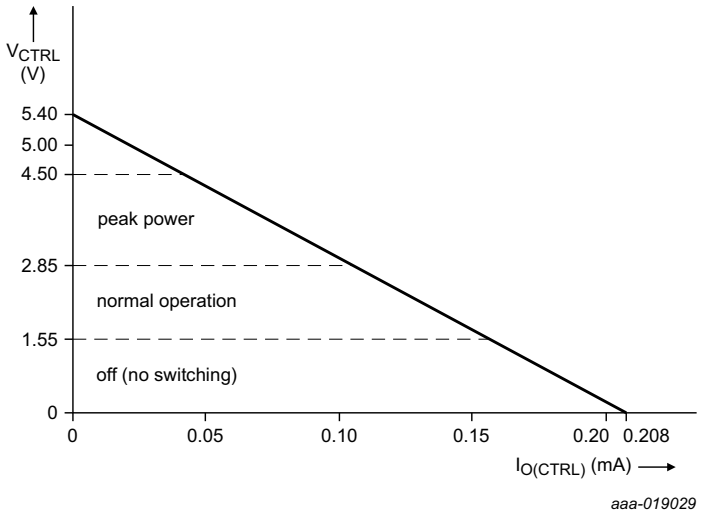



**Fig 6. $V_{CTRL}$ as a function of $I_{O(CTRL)}$**

### 3.3.3 Peak current control

The CTRL pin controls the primary peak current. Figure 7 shows the relationship between the voltage and the peak current on the CTRL pin.

The DRIVER output is switched on by each oscillator pulse. The voltage on the CTRL pin controls the oscillator frequency. It is switched off when the primary peak current measured on the ISENSE pin exceeds the peak current set by the CTRL pin or if the duty cycle exceeds 90 %.

### 3.3.4 Frequency control

The voltage on the CTRL pin controls the switching frequency. The frequency curve (see Figure 7) can be split into four areas:

- **Peak power**

  At peak power, the switching frequency is increased to 130 kHz to enable a higher output power from the same core. It also increases the switching losses but is irrelevant during temporary peak loads. For the maximum benefit of the frequency increase, the supply must operate (mainly) in DCM (in CCM, the frequency increase does not have much influence).

  Peak power can only be delivered during the 27.5 ms (TEA1833TS)/160 ms (TEA1833LTS) overpower time-out.

- **High power**

  At high power, the switching frequency is fixed to 65 kHz. Only the peak current is controlled.

- **Medium power**

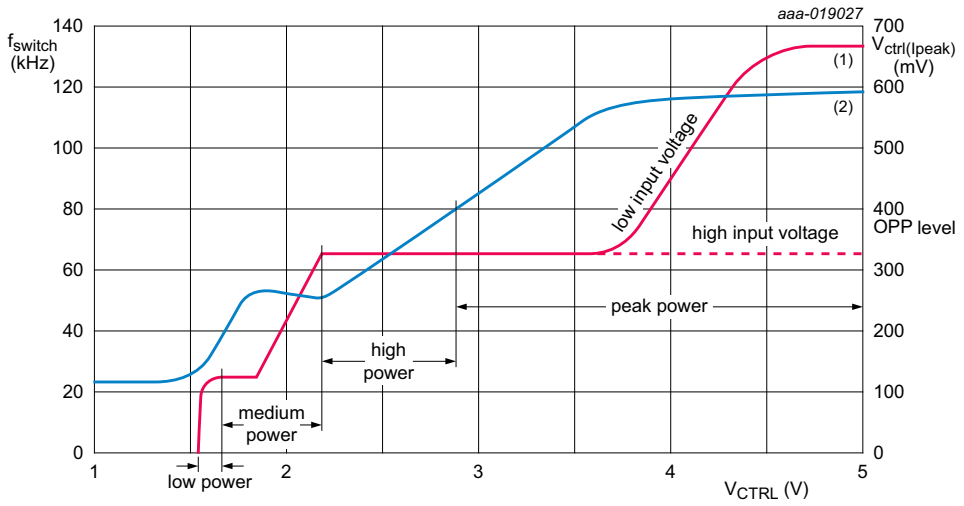
  At medium power, the switching frequency is reduced to 25 kHz to ensure high efficiency at low load. Reducing the switching frequency effectively reduces the switching losses. Before reducing the switching frequency below 25 kHz, the peak current is reduced to prevent audible noise.


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- **Low power**

  The peak current is not reduced below 22 % of its maximum value to ensure efficient operation at low output power. Instead, to reduce the output power, the switching frequency is reduced. The frequency now enters the audible spectrum but does not become audible because of the low peak current. This part of the frequency curve is also referred to as Voltage Controlled Oscillator (VCO) mode.




(1) $f_{sw}$

(2) $V_{ctrl(Ipeak)}$

**Fig 7. $V_{ctrl(Ipeak)}$ and $f_{sw}$ as a function of $V_{CTRL}$**

It is important to use the entire CTRL pin input range. If the chosen current sense resistor value is too low, only the lower part of the control curve is used. The frequency reduction already starts at a relatively high peak current which can result in audible noise.

### 3.3.5 Limitation of the maximum switching frequency

At low input voltage, the 130 kHz switching frequency is required during peak loads. But at high input voltage, the high switching frequency is not required. To limit the output power and to prevent stress on the peak clamp and the MOSFET, the maximum switching frequency is limited at high mains (see Figure 14). The frequency limitation starts at a bulk voltage of 180 V and reaches 65 kHz at 400 V.


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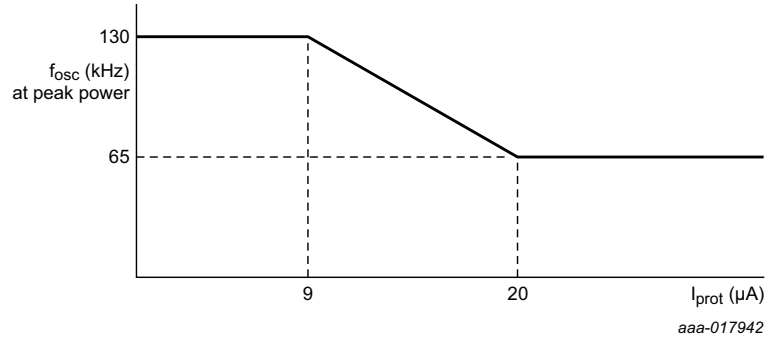



**Fig 8. Switching frequency limitation**

### 3.3.6 Burst mode

When the control voltage ($V_{CTRL}$) is pulled below 1.45 V (typical), the IC is not switching. It waits until the $V_{CTRL}$ exceeds this minimum level before starting the next cycle. During this period of no switching, the supply current of the TEA1833(L)TS discharges the VCC capacitor. When the voltage on the VCC pin drops to below $V_{th(burst)}$ (11.1 V typical), two strokes are asserted with minimal $I_{pk}$ to recharge the VCC capacitor. The assertion avoids that the voltage on the VCC pin drops to below UVLO level during a longer off-time.

Longer off-times occur when the output switches from peak load to no-load. The output voltage shows an overshoot and the system holds switching until the output voltage drops to below the regulation level while there is no load at the output.

The burst mode enables the use of a smaller VCC capacitor, shortening the start-up time or decreasing the no-load power by using higher value start-up resistors.

The burst mode is only intended to help with load changes. It is not intended for use under normal no-load conditions. For a minimum no-load power, the system must be in $V_{out}$ regulation, not in VCC regulation. The auxiliary winding voltage and the size of the VCC capacitor must be chosen so that this condition is met.

### 3.3.7 Switch-off delay

The primary peak current does not immediately stop when it passes the threshold level because there is some internal and external delay. During this delay, the primary current still continues to grow. The exact increase depends on the delay, the primary inductance and the voltage on the main electrolytic capacitor. The OPP compensation largely compensates this dependency on the bulk voltage. Due to this switch-off delay, fine-tuning of the $R_{sense}$ resistor value may be required to obtain the correct output power level.

The switch-off delay can be split into three delays:

- **External filter delay**

  Resistor R13 (see Figure 5) and the parasitic capacitance of the track (2 pF to 10 pF) create a delay. For minimal disturbance and capacitance, place R13 as close as possible to the ISENSE pin. The delay approximately equals R × C (13 ns to 68 ns).

- **Propagation delay**

  The internal delay from passing the threshold level on the ISENSE pin to the actual switching off the DRIVER pin is approximately 150 ns.


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- **MOSFET switch-off delay**

  The MOSFET does not immediately switch off when the DRIVER pin switches off. The MOSFET switch-off delay is defined as the delay from the moment the voltage on the DRIVER pin starts to drop until the drain of the MOSFET reaches the bulk voltage. It must be measured in the application.

### 3.3.8 Leading-Edge Blanking (LEB)

The ISENSE input is internally blanked for the first 325 ns of each switching cycle. The blanking prevents that spikes caused by parasitic capacitance (gate-source and drain-source capacitance of the MOSFET and the parasitic capacitance of the transformer) trigger the peak current comparator prematurely.

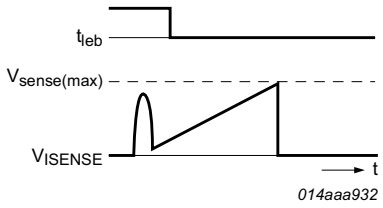



**Fig 9. Leading edge blanking**

## 3.4 Protections

### 3.4.1 Overview

Depending on which protection is triggered and on the version of the IC, the protection causes a safe restart or latches the converter to an off-state. Table 2 shows an overview of the protection features.

**Table 2. Protection handling TEA1833(L)TS**

| Protection | TEA1833TS | TEA1833LTS | Comment |
|---|---|---|---|
| internal $V_{CC}$ OVP | latch | latch | four consecutive switching cycles |
| UVLO | restart | latch | |
| maximum duty cycle | restart | restart | eight consecutive switching cycles |
| internal OTP | latch | latch | four consecutive switching cycles |
| brownin/brownout | restart | restart | |
| external OTP | latch | latch | four consecutive measuring cycles |
| external OVP | latch | latch | four consecutive switching cycles |


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**Table 2. Protection handling TEA1833(L)TS** *…continued*

| Protection | TEA1833TS | TEA1833LTS | Comment |
|---|---|---|---|
| OPP | slow restart | latch | TEA1833TS:<br>27.5 ms overpower time-out (14.7 ms in case of OSCP)<br>TEA1833LTS:<br>160 ms overpower time-out (also in case of OSCP) |
| OCP | cycle-by-cycle | cycle-by-cycle | |
| OSCP | cycle-by-cycle | cycle-by-cycle | |

See Section 3.4.2 and Section 3.4.3 for explanation of safe restart and latched off-state.

### 3.4.2 Protection handling: Restart

#### 3.4.2.1 Regular restart (short)

If one of the protections triggers a restart, the TEA1833(L)TS immediately stops switching and the supply current of the IC quickly discharges the VCC capacitor. When $V_{CC}$ drops below the undervoltage lockout level, the IC enters power-down mode. The supply current drops to approximately 11 μA and a normal start-up sequence follows.

#### 3.4.2.2 OPP restart (slow restart, not in TEA1833LTS)

If the OPP triggers a restart, the regular restart delay is insufficient to keep the average input power below an acceptable level (usually 5 W) in a continuous overload. The TEA1833TS first carries out a regular restart sequence, but instead of starting up when $V_{CC}$ reaches 22 V, it does not wake up from power-down mode. Instead it discharges the VCC capacitor to 10.5 V again and lets the start-up circuit charge the capacitor. It continues charging and discharging between $V_{startup}$ and $V_{th(UVLO)}$ three times before starting up (see Figure 4).

The rising slope of this saw tooth depends on the mains voltage, the start-up circuit and the VCC capacitor. At low input voltage the restart time increases. An internal current source (2.5 mA) determines the falling slope of the saw tooth.

### 3.4.3 Protection handling: Latch

#### 3.4.3.1 Latched off-state

When one of the protection features triggers the latched off-state, the IC immediately stops switching and enters power-down mode. It clamps the VCC pin to 5.4 V, which is just above the reset level (4.5 V).

#### 3.4.3.2 Resetting a latched protection

To reset a latched protection, the voltage on the VCC pin must drop to below 4.5 V. A "power-cycle" of the mains must be done. Unplug the mains, wait a moment and then reconnect the mains.

If a latched protection is triggered, the VCC pin is automatically clamped to a voltage just above the reset level. When the mains is unplugged, the start-up current stops and the 11 μA supply current to the TEA1833(L)TS discharges the VCC capacitor. Because the capacitor only is required to discharge from 5.4 V to 4.5 V, it resets quickly.


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When capacitor $C_{VCC}$ = 2.2 μF, the discharge time is 0.3 s. In practice, the start-up current does not always immediately stop charging the VCC capacitor after unplugging the mains because the X-cap can still be charged for about one second.

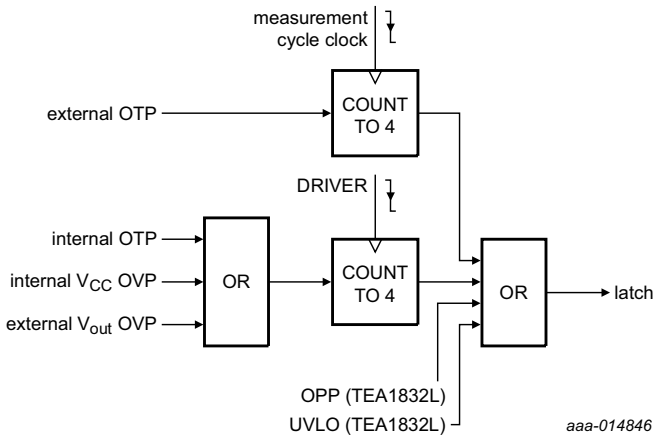



**Fig 10. Latched protections**

### 3.4.4 Internal $V_{CC}$ OVP

An internal overvoltage protection sets the IC to latched-off state when the voltage on the VCC pin exceeds 36 V for four consecutive switching cycles (all TEA1833 versions). The internal OVP measures on the falling edge of the DRIVER signal.

### 3.4.5 UnderVoltage LockOut (UVLO)

#### 3.4.5.1 Restart version (TEA1833TS)

When during normal operation the voltage on the VCC pin drops to below the undervoltage lockout threshold ($V_{th(UVLO)}$ = 10.5 V typical), the IC stops switching and enters power-down mode. The start-up circuit charges the VCC capacitor and a normal start-up sequence follows.

#### 3.4.5.2 Latch version (TEA1833LTS)

When during normal operation VCC drops below the undervoltage lockout threshold, the IC is set to the latched protection mode. It ensures that a shorted output always triggers the latched protection mode, including if $V_{CC}$ drops below $V_{th(UVLO)}$ before the OPP has a chance to respond.

### 3.4.6 Maximum duty cycle protection

The main purpose of the maximum duty cycle protection is to ensure a well-defined response to mains supply dips.

If the peak current measured by the ISENSE pin does not reach the $V_{ctrl(Ipeak)}$ level set by the CTRL pin within a duty cycle of 90 %, the maximum duty cycle limitation ends the driver pulse. If the maximum duty cycle is exceeded during eight consecutive switching cycles, the maximum duty cycle protection triggers a restart.


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In low-power mode, the switching frequency can become very low. Limiting the duty cycle to 90 % is insufficient to prevent a long on-time. In low-power mode, the maximum duty cycle limitation changes to maximum on-time limitation. The maximum on-time is 36 μs.

### 3.4.7 Internal OverTemperature Protection (OTP)

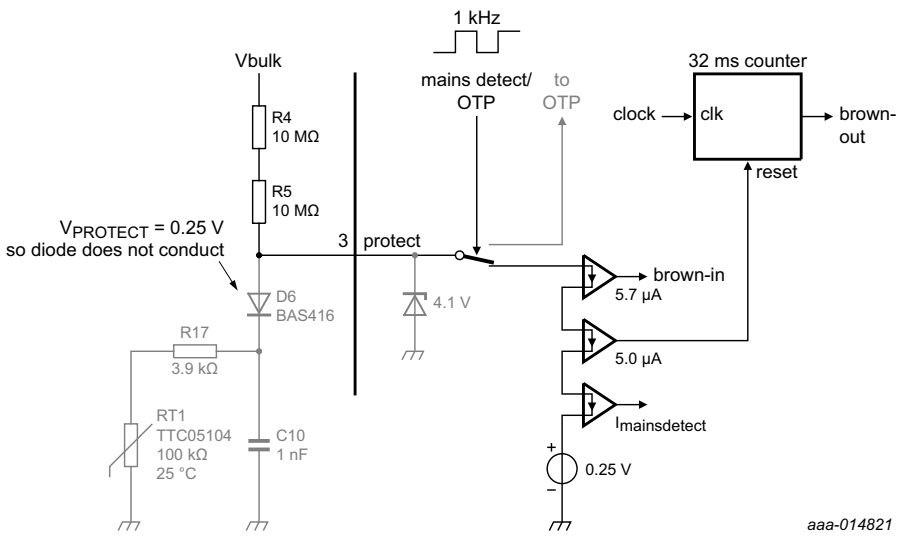
When the temperature in the chip exceeds 140 °C, the internal OTP sets the controller to the latched off-state (in all TEA1833 versions).

### 3.4.8 Brownin/brownout and external OTP protection (PROTECT pin)

The PROTECT pin cycles between mains detection measurement used for brownin/brownout and high/low line compensation and external OTP. Each measurement lasts 500 μs.

#### 3.4.8.1 Brownin

Figure 17 shows the circuit.




The components, related to the external OTP, are grayed out but present for reference.

**Fig 11. PROTECT pin: Mains detection function**

The mains detection function determines the bulk voltage on the mains electrolytic capacitor by measuring the current through a 20 MΩ resistor connected to the PROTECT pin. During mains detection measurement, the PROTECT pin is clamped to 0.25 V ensuring that diode D6 blocks the influence of the connected external OTP circuit. The measured mains detection current is stored for reference.

To minimize the error in the measured mains detection current, select a low reverse leakage type for diode D6. The NXP BAS416 is suited for this purpose.

To allow the start-up of the IC when VCC reaches $V_{startup}$ (22 V typical), the mains detection current must exceed 5.7 μA. It correlates to a bulk voltage of 5.7 μA × 20 MΩ = 114 V (DC). Because there is no load yet, the bulk voltage equals the peak voltage of the mains minus 2 diodes, which yield for the AC voltage:

$(114 + 1.4)/\sqrt{2} = 82\ V$.


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### 3.4.8.2 Brownout

The mains detection current is also used to realize the brownout function. When the mains detect current drops to below 5 μA for 32 ms, switching is stopped and a restart is made for both the latched and the non-latched versions.

Each time the mains detection current exceeds 5 μA, the 32 ms counter is reset. The counter-reset ensures that only the peak of the mains is measured and the brownout level is independent of the load (see Figure 12).

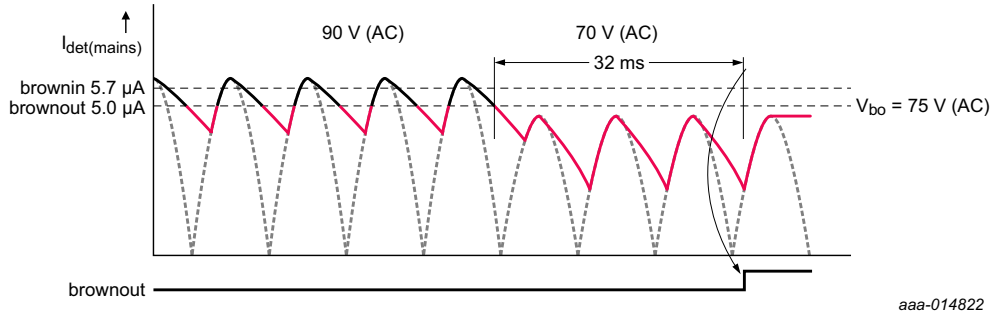



**Fig 12. Bulk voltage versus brownout detection**

At 90 V (AC), the valley of the mains ripple drops to below 5 μA. However, each peak exceeding 5 μA resets the 32 ms counter. Only when the peak of the mains detection current remains < 5 μA, the protection is triggered.

The brownout level of 5 μA corresponds with a bulk voltage of $5\ \mu A \times 20\ M\Omega = 100\ V\ (DC)$. Because this level corresponds with the peak of the AC input voltage, we get: $(100 + 1.4)/\sqrt{2} = 72\ V\ (AC)$

### 3.4.8.3 High/low line compensation

In fixed-frequency DCM, peak current limitation can also act as overpower protection because the maximum output power is independent of the input voltage. In fixed-frequency CCM, the maximum amount of power that can be transferred to the output not only depends on the primary peak current. It also depends on the duty cycle and therefore on the input voltage.

To obtain the same overpower protection level over the mains input range, high/low line compensation adjusts the peak current level as a function of the mains input voltage.

The high/low line compensation is realized by forcing a current $I_{opc}$ (overpower correction) out of the ISENSE pin (see Figure 13).


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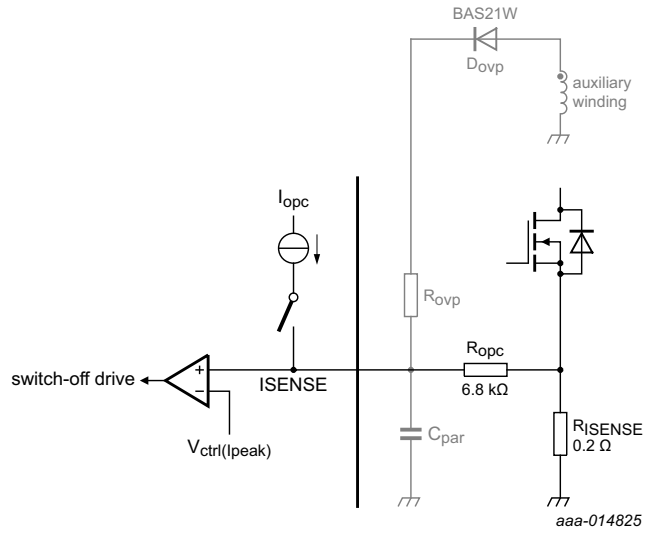



**Fig 13. High/low line compensation ISENSE pin**

The current $I_{opc}$ is related to the measured mains detection current. It causes a voltage drop over resistor $R_{opc}$ between the ISENSE pin and $R_{sense}$. The higher $I_{opc}$, the earlier the required $V_{ctrl(Ipeak)}$ is reached at the ISENSE pin.

Figure 14 shows the relationship between the mains detection current and $I_{opc}$.

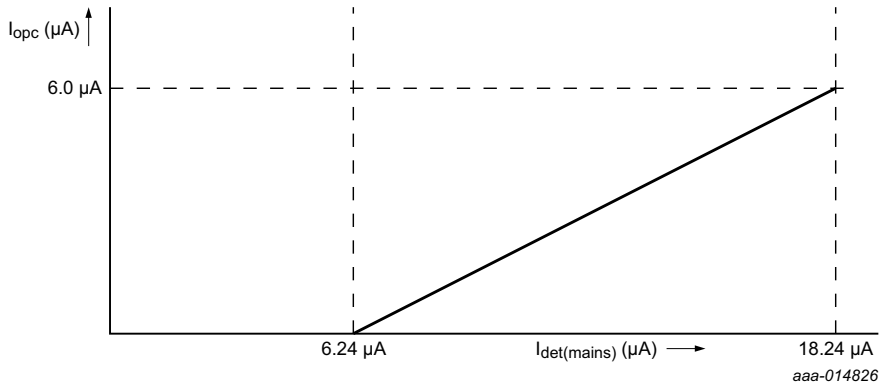



**Fig 14. Relationship between $I_{det(mains)}$ and $I_{opc}$**

The compensation starts from $I_{det(mains)}$ = 6.24 µA which corresponds with 125 V (DC) bulk voltage. For 365 V bulk voltage, $I_{det(mains)}$ = 18.24 µA and $I_{opc}$ = 6 µA. For $I_{det(mains)}$ > 6.24 µA: $I_{opc} = 0.50 \times (I_{det(mains)} - 6.24)\ \mu A$.

The value of resistor $R_{opc}$ determines the level of compensation. With the $R_{opc}$ value used in the schematic (6.8 kΩ; see Figure 13), the correction of the voltage on the ISENSE pin is 41 mV at 365 V (DC) bulk voltage (264 V (AC)). This correction equals about 10 % of the 400 mV $V_{th(sense)opp}$.

At low output power ($V_{ctrl(Ipeak)}$ < 350 mV), the high/low line compensation is switched off.


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#### 3.4.8.4 External OverTemperature Protection (OTP)

The external OverTemperature measurement is combined with the mains detection function on the PROTECT pin (see Section 3.4.8). The PROTECT pin cycles between mains detect (500 μs) and external OverTemperature measurement (500 μs). Figure 15 show the circuit. The components for mains detection are grayed out but present for reference.

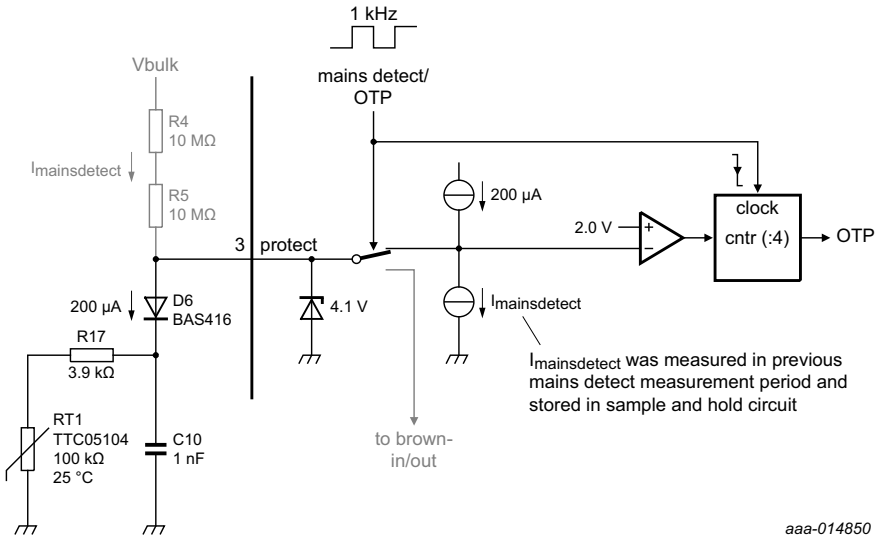



**Fig 15. External OTP circuit**

During temperature measurement, a 200 μA current flows out of the PROTECT pin through the connected diode in series with an NTC to ground. The additional fixed series resistor can be used to tune the temperature trigger point of the detection. The latched protection is triggered when, during the 500 μs measurement, the voltage on the PROTECT pin remains below 2.0 V for four consecutive measurement cycles (see Figure 16). At trigger point, the voltage over the NTC plus optional series resistor equals 2.0 V minus the forward voltage of the diode: $V_{NTC} + V_{Rseries} = 2.0 - 0.55 = 1.45\ V$.

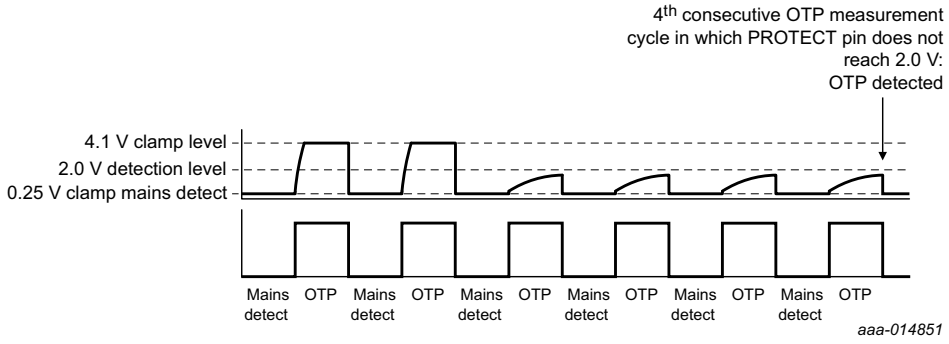



**Fig 16. Voltage on the PROTECT pin**


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The mains detection measurement does not disturb the temperature measurement. The current through the 20 MΩ resistor, measured during mains detection, is stored and subtracted from the 200 μA current during the OTP measurement.

Two remarks regarding diode D6:

- The forward voltage of diode D6 is temperature-dependent. However, it does not influence the detection accuracy. It behaves as an additional temperature sensor with a negative temperature coefficient of 2 mV/K.
- To minimize the error of the mains detect current measurement, diode D6 must be a low leakage type. The NXP Semiconductors BAS416 is suited for this purpose.

#### 3.4.8.5 Clamp

An internal clamp prevents that the voltage level at the pin exceeds 4.1 V (typical) when a high ohmic NTC is used. At start-up, when the pin is not active yet, the divider of the mains detection resistor and the NTC can cause a voltage level that is too high at high mains when a high ohmic NTC is used. The clamp voltage is specified at a 200 μA input current (the exact voltage depends on the current). In power-down mode, the clamp voltage drops to approximately 2.0 V.

### 3.4.9 External output OverVoltage Protection (OVP)

The purpose of the overvoltage protection is to protect the devices connected to the output. It also protects the supply itself against output voltages that are too high, for example, when the voltage feedback loop is disturbed.

The output voltage is measured via the auxiliary winding using a diode in series with a resistor connected to the ISENSE pin (see Figure 17).

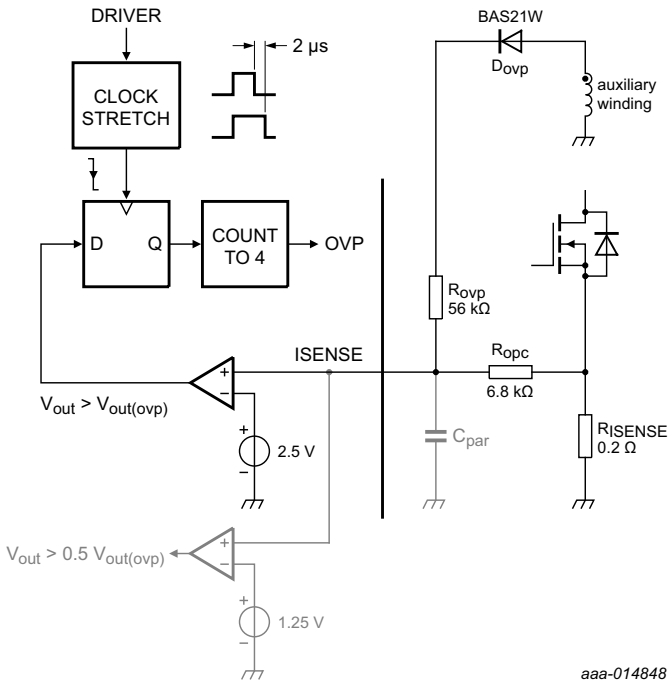



**Fig 17. External output OVP circuit**


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Resistors $R_{ovp}$, $R_{opc}$, and $R_{sense}$ form a resistive divider. The voltage on the ISENSE pin is measured during the secondary stroke. When the voltage exceeds 2.5 V for four consecutive switching cycles, the controller is set to the latched-off state.

The first 2 µs of the secondary stroke are discarded to avoid incorrect level measurement due to ringing (see Figure 18).

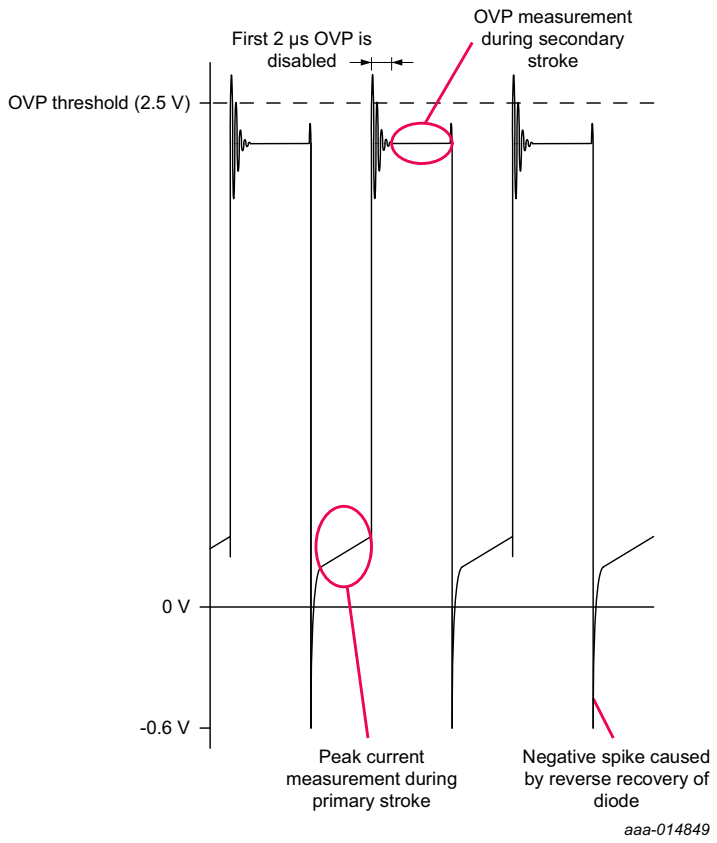



**Fig 18. Voltage on the ISENSE pin**

The $V_{out}$ OVP measurement can be combined with the peak current measurement because the branch with resistor $R_{ovp}$ is inactive during the primary stroke. The branch with resistor $R_{ovp}$ is inactive during the primary stroke because of the added diode and the negative voltage on the auxiliary winding.

At the start of the primary stroke, a negative spike is present on the ISENSE pin. The reverse recovery of the diode causes the spike. The internal ESD diode of the ISENSE pin, which can handle 10 mA, clamps the spike.

### 3.4.10 OverPower Protection (OPP)

The maximum nominal output power is reached when the internal control voltage $V_{ctrl(Ipeak)}$ exceeds the overpower level (400 mV typical) while switching at 65 kHz (see Figure 19).


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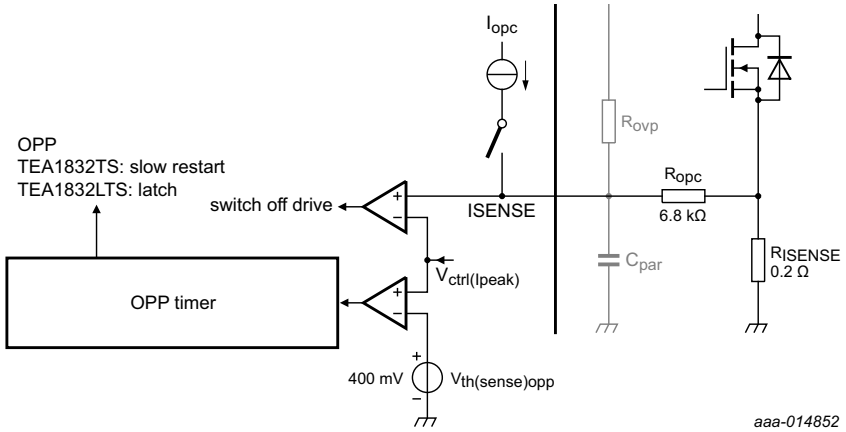



**Fig 19. Overpower protection and compensation**

When $V_{ctrl(Ipeak)}$ exceeds 400 mV, the OPP timer is started. When the maximum nominal output power is continuously exceeded for the overpower time-out duration (see Table 3), the OverPower Protection (OPP) is activated. The controller immediately stops switching and performs a slow restart (TEA1833TS) or enters the latched-off state (TEA1833LTS).

**Table 3. Overpower time-out**

| $V_{out}$ level | TEA1833TS | TEA1833LTS |
|---|---|---|
| $V_{out} > 0.5\ V_{out(ovp)}$[1] | 27.5 ms | 160 ms |
| $V_{out} < 0.5\ V_{out(ovp)}$[1] | 14.5 ms | 160 ms |

[1] $V_{out(ovp)}$ is the output voltage at which the external OVP triggers.

During a slow restart, the IC cycles the voltage on the VCC pin three times between $V_{th(UVLO)}$ and $V_{startup}$ before switching begins. It reduces the input power for continuous overload due to the lower repetition rate of the switching cycles (see Section 3.4.2.2).

When $V_{ctrl(Ipeak)}$ drops to below 400 mV before the OPP timer reaches the overpower time-out, the timer is immediately reset. The reset enables (repeated) temporary overloads (see Figure 20).

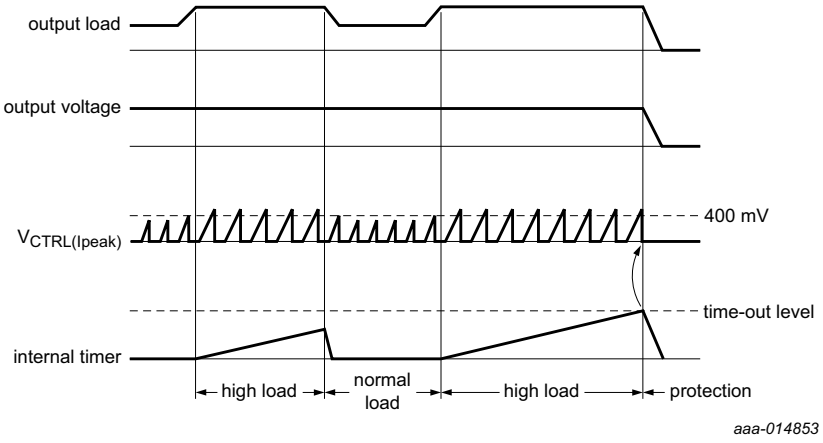



**Fig 20. Overpower time-out**


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The OPP time-out is reduced during heavy overload or short circuit events, where the output voltage drops to below half the OVP level of $V_{out}$ (TEA1833TS only). Reducing the OPP time-out limits the input power during slow restart in continuous overload condition. Details are described in Section 3.4.13.

The OPP time-out is realized by dividing the internal jitter clock. Because an occurrence of an OPP condition is not synchronized with the internal jitter clock, the OPP time-out varies with one clock cycle of the internal jitter clock (3.8 ms).

The TEA1833(L)TS incorporates a built-in high/low line compensation to ensure that the OPP level is constant over the full mains input range. This feature is described in Section 3.4.8.

#### 3.4.10.1 Slow restart delay timing calculation (TEA1833TS only)

When the OPP triggers a safe restart procedure, the TEA1833TS immediately stops switching, discharges $V_{CC}$ to below $V_{th(UVLO)}$ and enters power-down mode.

The start-up circuit charges the VCC capacitor to $V_{startup}$ but instead of starting up, the VCC capacitor is discharged again. To obtain a longer restart time, the charging/discharging is repeated for three cycles.

The restart time of one restart cycle consists of two periods:

- Discharging the VCC capacitor by an internal current source (2.5 mA). The discharge time is independent of the mains voltage[2].
- Charging the capacitor from $V_{th(UVLO)}$ to $V_{startup}$ by the external start-up circuit of typically 81 μA at 264 V (AC).

The discharge current is much higher than the charge current. So the mains voltage and the start-up circuit mainly determine the restart time.

The discharge time is approximately:

$$t_{dch} = \frac{C_{VCC} \times (V_{startup} - V_{th(UVLO)})}{I_{CC}} = \frac{2.3\ \mu F \times (22\ V - 10.5\ V)}{2.5\ mA} = 10\ ms \quad (2)$$

Where:

- $C_{VCC}$ is the total capacitance on the VCC pin
- $I_{CC(restart)}$ is the current discharged by the internal current source

**Remark:** The first discharge time differs from the one calculated in Equation 2. The starting voltage can be higher or lower (depending on the load) and the discharge current source is not yet switched on. The operating supply current (= 0.58 mA) discharges the VCC capacitor.

The charge time is pending on the value of the start-up resistors. Worst case (shortest charge time) occurs for the highest mains voltage.

The charge current at 264 V (AC) and $R_{startup}$ = 2.4 MΩ becomes

2. The first discharge differs somewhat from the following ones. The starting voltage can be lower or higher (depending on the load) and the discharge current source is not yet switched on. The operating supply current (= 0.58 mA) discharges The VCC capacitor.


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$$I_{ch} = \frac{\frac{2}{\pi} \times \sqrt{2} \times V_{mains} - \frac{V_{startup} + V_{th(UVLO)}}{2}}{R1} - I_{CC(startup)}$$
$$= \frac{0.64 \times 1.41 \times 264\ V\ (AC) - \frac{22\ V + 10.5\ V}{2}}{2.4\ M\Omega} - 11\ \mu A = 81\ \mu A \quad (3)$$

Where:

- $V_{mains}$ is the RMS input voltage

The charge time becomes:

$$t_{ch} = \frac{C_{VCC} \times (V_{startup} - V_{th(UVLO)})}{I_{ch}} = \frac{2.3\ \mu F \times (22\ V - 10.5\ V)}{81\ \mu A} = 0.32\ s \quad (4)$$

Where:

- $I_{ch}$ is the charge current into the VCC capacitor (see Equation 3)

The total restart delay for the start-up circuit with two resistors and diodes approximately equals:

$$t_{restart} = 3 \times (t_{dch} + t_{ch}) = 3 \times (0.01\ s + 0.32\ s) = 0.99\ s\ at\ V_{mains} = 264\ V \quad (5)$$

#### 3.4.10.2 Ratio OPP time-out/restart delay

In a continuous overload, the supply keeps switching on and off (only valid for the non-latched version). At high mains, the ratio of the on-time and off-time is approximately 1:31 for the 27.5 ms OPP timer. It is sufficient to keep the average input power during a continuous overload below 5 W in most applications.

The average input power during a continuous overload at maximum peak power is:

$$P_{i(AV)} = \left(\frac{t_{opp}}{t_{opp} + t_{restart}}\right) \times \left(\frac{P_{o(max)}}{\eta}\right) = \left(\frac{27.5\ ms}{27.5\ ms + 930\ ms}\right) \times \frac{130\ W}{0.9} = 4.15\ W$$
$$at\ V_{mains} = 264\ V\ (AC) \quad (6)$$

Where:

- $P_{i(AV)}$ is the average input power during an overload
- $t_{opp}$ is the overpower protection time-out time, the time from exceeding the overpower threshold to triggering the protection. This time is fixed to 27.5 ms in the IC.
- $t_{restart}$ is the restart delay, the time from triggering the protection until the next start-up attempt
- $P_{o(max)}$ is the maximum peak output power; the maximum power that the supply can deliver during the overpower protection time-out time.

For a short circuit at the output, the OSCP protection shortens the maximum OPP time to 14.5 ms. The delivered output power is also reduced due to the lower output voltage and the lower switching frequency when OSCP is triggered. The shortening of the OPP time leads to a reduction of the $P_{i(AV)}$ by a factor 4.


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During an output short $P_{i(AV)} \approx 1.05$ W at 264 V (AC).

In practice, measurements < 1 W at 264 V (AC) were done in a 65 W demo board.

The restart delay depends on the input voltage, the start-up circuit and the VCC capacitor. The restart delay can be changed by changing the values of the start-up circuit or the VCC capacitor. However, changing the values of the start-up circuit of the VCC capacitor also influences the start-up time.

The input power at continuous overload can be decreased in the following way:

1. Increase the restart delay by increasing the start-up resistors or capacitor $C_{VCC}$.
2. Decrease the maximum output power by increasing the current sense resistor (if possible).

### 3.4.11 OverCurrent Protection (OCP)

To prevent saturation of the transformer and so currents in the MOSFET that are too high, a cycle-by-cycle primary inductor current limitation is built in.

When the voltage on the ISENSE pin exceeds 575 mV, the current switching cycle is immediately ended. When the OCP limits the peak current, the output voltage can no longer be maintained. The converter continues to switch until the OPP is triggered or until $V_{CC}$ has dropped to below $V_{th(UVLO)}$ (10.5 V typical).

### 3.4.12 Temporary peak power

It is possible to deliver a peak power of 200 % for a short time. To keep the output voltage within regulation and prevent that protections are triggered, the following conditions must be met:

- The voltage on the ISENSE pin must remain < 575 mV (to prevent that OCP is triggered and limits the power)
- The duration must be shorter than the OPP time-out (to avoid the triggering of OPP)

To deliver the power, the switching frequency increases from 65 kHz to 130 kHz. The voltage on the ISENSE pin increases from 400 mV to 575 mV.

The actual peak power which can be delivered depends on the input voltage, the size of the mains electrolytic capacitor, and the duration of the peak power. The high/low line compensation for the input voltage is also active during peak power. However, the correction is optimized for OPP. For low input voltage, the mains electrolytic capacitor and the duration determine the maximum peak power.

### 3.4.13 Output Short Circuit Protection (OSCP)

The OSCP prevents saturation of the transformer during continuous overload or shorted output. Transformer saturation can cause runaway of the input power and the peak current. The OSCP lowers the switching frequency and shortens the duration of the OPP timer from 27.5 ms to 14.5 ms (typical).

To clarify the phenomenon, a simplified circuit is used. In the simplified circuit, a transformer with a turn ratio of 1:1 is used because then the start value and the peak value of the primary and secondary currents are the same (see Figure 21).


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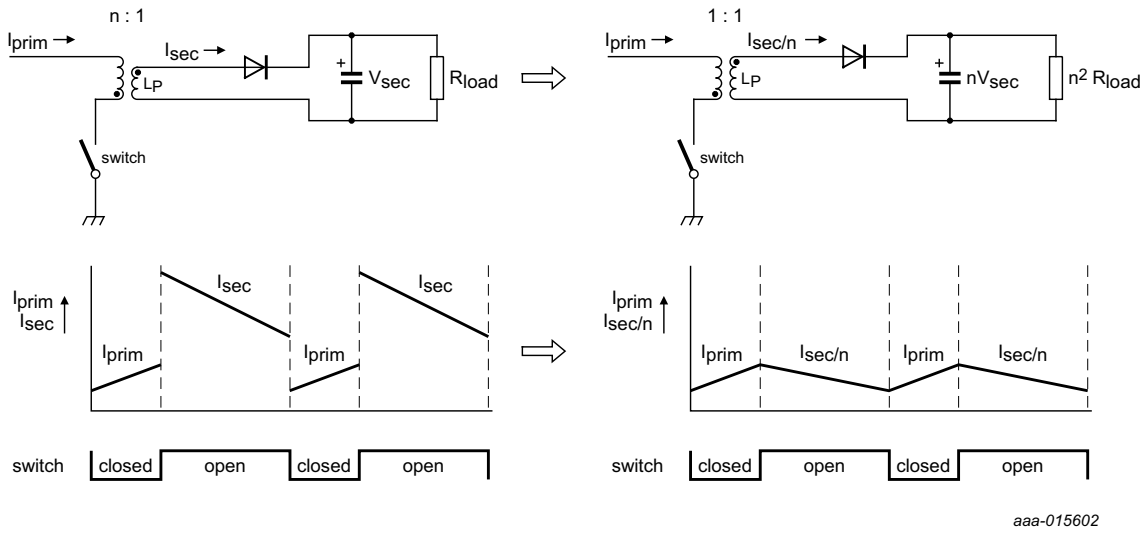



**Fig 21. Simplified flyback circuit**

The currents are drawn for CCM. The primary current starts with an offset equal to the value of $I_{sec/n}$ at the moment the primary stroke is initiated. The primary current increases until the drive is switched off. The secondary current $I_{sec/n}$ starts with the value of the primary current at switch-off and decreases until the next primary stroke is initiated. The transfer of the transformer winding ratio from n:1 to 1:1 means that the secondary current is divided by the turn ratio n. The output voltage is multiplied with the turns ratio n.

The simplified flyback circuit is used to explain the saturation/runaway problem. When the circuit is in balance, the current increase during the primary stroke equals the current decrease during secondary stroke. If the output is short-circuited, $V_O$ (and also $nV_O$) becomes low. The decay of the secondary current $I_{sec/n}$ also becomes low because it is proportional to $V_O$ ($I_{decrease} = (n \times V_O / L_p) \times t_s$.

In CCM, the switching time is fixed. When the current increase during the primary stroke exceeds the decrease during the secondary stroke, the DC offset part of the current increases at every stroke. This effect is called runaway, because it is not possible to reach a balanced state (see Figure 22).

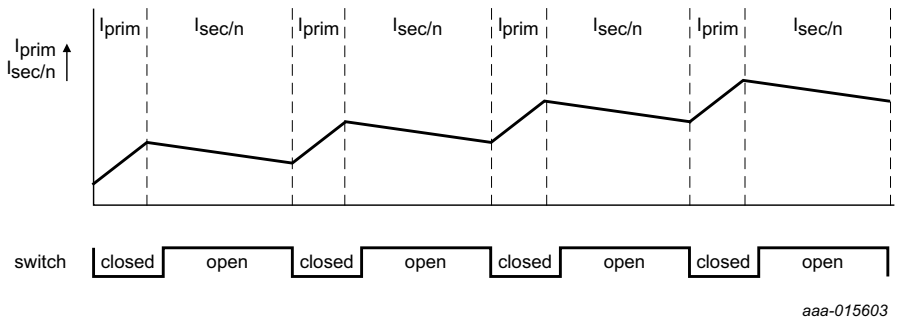



**Fig 22. Runaway effect**


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Because the maximum flux density B of the core is proportional to the primary current ($B = L_p \times I_p / N_p \times A_e$), the core flux density also increases. The transformer finally saturates and $L_p$ reduces dramatically. The primary current can increase to very high levels.

To avoid runaway, the current decrease during the secondary stroke must be enlarged. The only available option is to enlarge the secondary stroke time $t_s$ by lowering the switching frequency. The increased secondary stroke time allows the secondary current to decrease to zero before the next primary stroke is initiated. It also reduces the DC offset at the start of the primary stroke to zero which stops the runaway. The OSCP initiates the lower switching frequency when activated. (see Figure 23).

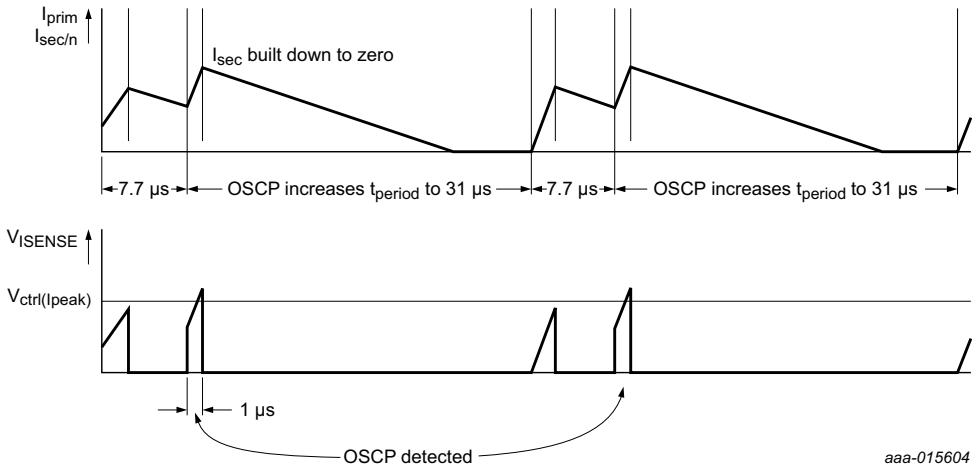



**Fig 23. OSCP cycle-by-cycle protection**

To detect if the risk of runaway is present and the OSCP must be activated, the voltage level at the ISENSE pin is monitored. When the voltage, reflecting the primary peak current, is too high within 1 µs after switch-on of the drive, the OSCP is activated. The exact conditions are:

- The $V_{ctrl(Ipeak)}$ level must be > 400 mV (OPP condition). The typical control voltage ($V_{ctrl}$) on the CTRL pin > 2.85 V.
- The measured voltage level on the ISENSE pin must be higher than the $V_{ctrl(Ipeak)}$ level after 1 µs. Depending on the voltage on the CTRL pin, $V_{CTRL(Ipeak)}$ ranges from 400 mV to 575 mV.

When these conditions are met, the next stroke is delayed with a factor 4 (31 µs instead of 7.7 µs). This delay is repeated as long as the above conditions exist. If the voltage on the ISENSE pin is < $V_{ctrl(Ipeak)}$ after 1 µs or $V_{ctrl(Ipeak)}$ drops to below the OPP condition, normal switching is resumed.

Because the runaway problem only happens when the output voltage is far below its nominal value, the OSCP is only enabled if the output voltage is lower than half the $V_{out}$ OVP value. The $V_{out}$ level is detected in a similar way as the $V_{out}$ OVP (see Figure 24).


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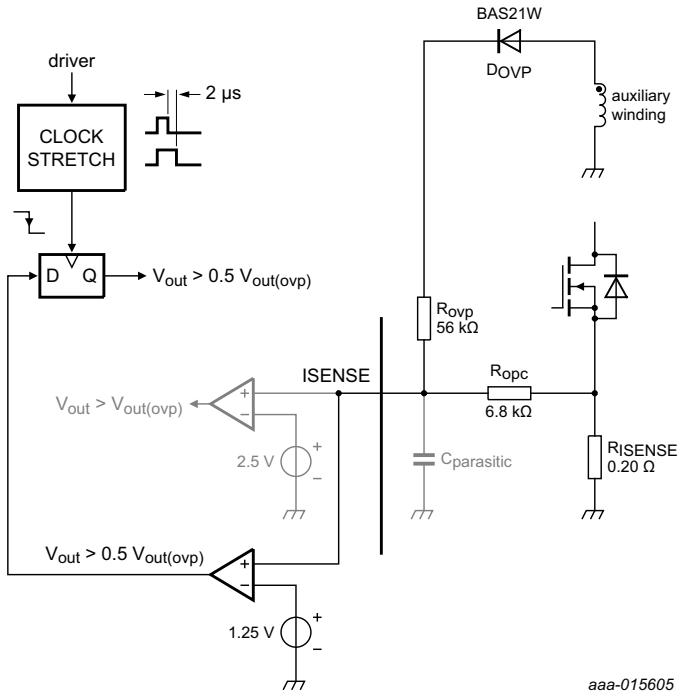



**Fig 24. Detection 0.5 $V_{out}$ OVP level**

To lower the average input power further during a short circuit event, the OPP timer is reduced from 27.5 ms to 14.7 ms when OSCP is enabled (TEA1833TS only).

The OSCP prevents overstress during start-up. Because the output capacitors are discharged, they behave as a short circuit until the output voltage starts to increase after the first strokes.

## 3.5 Slope compensation

The TEA1833(L)TS has built-in slope compensation to prevent subharmonic oscillation in CCM at duty cycles above 50 %. The slope compensation is internally added to the CTRL input signal (see Figure 25). The slope compensation is 18 mV/µs referred to the ISENSE pin. The slope compensation is only active on duty cycles higher than 45 %.

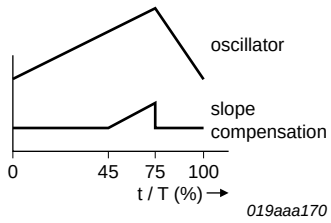



**Fig 25. Slope compensation waveforms**


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## 3.6 Driver

The driver circuit has a current sourcing capability of 300 mA typical and a current sink capability of 750 mA typical, permitting a fast turn-on and turn-off of the power MOSFET for efficient operation. See Figure 5 for the DRIVER pin control.

## 3.7 Frequency modulation

The switching frequency and its harmonics are responsible for a large part of the conducted EMI problems. Modulation of the switching frequency spreads all frequency peaks that are related to the switching frequency over wider bands, significantly decreasing the so-called "average measurement". See Figure 5 for the location of oscillator and frequency modulation.

The oscillator is continuously modulated at a rate of 260 Hz and a range of ±6 % (±4 kHz at 65 kHz). For example, the third harmonic of 65 kHz is spread over a frequency band of 3 × 8 = 24 kHz.

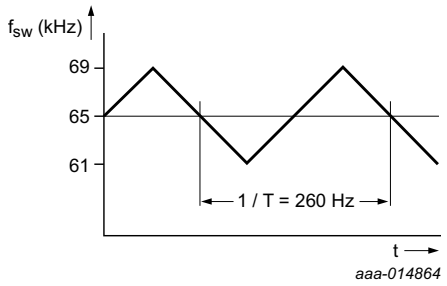



**Fig 26. Frequency modulation**


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# 4. Application (pin-by-pin)

## 4.1 VCC pin

### 4.1.1 Start-up circuit

A low-cost start-up circuit that caters for the X-cap discharge is the two-resistor-+-diode start-up circuit. The added diode improves the start-up time. See Section 5 for a full explanation of the start-up circuit.

### 4.1.2 VCC capacitor

The VCC capacitor must be as small as possible to make the start-up time (and the latch reset time) as short as possible.

First of all, the value of the capacitor must be sufficient to supply the TEA1833(L)TS until the auxiliary winding takes over. It depends on the soft start time, the load on the output and the values of the secondary capacitors.

Other factors also determine the minimum value of the capacitor. Some worst case tests to determine the minimum value of the VCC capacitor are:

- **No-load operation**

  The supply runs at low frequency so there is a long interval between two consecutive charge pulses from the auxiliary winding. To prevent that the IC runs on $V_{CC}$ regulation instead of $V_{out}$ regulation, the lowest level of $V_{CC}$ must remain 2 V above $V_{th(burst)}$.

- **Transient from full load to no-load**

  A transient from full load to no-load can cause a small overshoot on the output voltage. It can take a long time for the output capacitor to discharge to the level at which the supply starts to switch again because of the absence of any external load.

  During this time, the auxiliary winding does not charge the VCC capacitor. Because the implemented burst mode which asserts two strokes with minimum $I_{pk}$ to recharge the VCC capacitor when VCC drops below $V_{th(burst)}$ overcomes this problem, this condition puts no requirement on the value of the VCC capacitor.

- **Low ESR type**

  The VCC capacitor must be a low Equivalent Series Resistance (ESR) type. Under low load or no load conditions, the switching frequency can be very low, for example, 250 Hz. The auxiliary voltage, which can have a duty cycle of only 0.1 %, must charge the VCC capacitor. It is only present for a few μs per cycle and the time between two cycles can be a few ms. So, the VCC capacitor charge current at no load is roughly equal to the current consumption of the IC multiplied by 1000: $1000 \times 0.5\ mA = 0.5\ A$.

  Use a low ESR capacitor because the relatively high ESR of a regular electrolytic capacitor limits the charge current and can cause the $V_{CC}$ to drop below $V_{th(burst)}$. If $V_{CC}$ drops to below $V_{th(burst)}$, the IC runs on $V_{CC}$ regulation instead of $V_{out}$ regulation increasing the no-load input power.


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### 4.1.3 Auxiliary winding or take-over winding

The optimal voltage of the auxiliary winding is approximately 20 V:

- Not much lower because during a no-load operation it has to be able to keep the $V_{CC}$ above the $V_{th(burst)}$. Keep a margin of 2 V above the maximum $V_{th(burst)}$ value to have some margin for disturbances and component spread.
- Not much higher because at maximum load the $V_{CC}$ must not trigger the OVP.

The series inductor L1 serves two purposes:

- To ensure that the VCC capacitor is charged evenly at very low switching frequencies during no-load. The high recharge current of the VCC capacitor can lead to loop disturbance and irregular switching in the no-load condition. L1 smoothes the charge current of the VCC capacitor which stabilizes the behavior.
- To prevent that the ringing at the start of the secondary stroke is rectified. Ringing can charge the VCC capacitor to above the OVP level.

L1 is not always required. It depends on the coupling between the windings. Sometimes a resistor of approximately 4.7 Ω is good enough.

### 4.1.4 Maximum start-up current

The maximum current that can be supplied by the start-up circuit must not exceed 1 mA. The start-up circuit must not be able to deliver more than 1 mA at maximum mains voltage. During latched protection, VCC is clamped to 5.4 V. The clamp can sink at least 1 mA over the entire operating temperature range. Above 1 mA, the clamp holding VCC below its maximum rating cannot be guaranteed[3]. The minimum $R_{startup}$ value is 470 kΩ.

If a charge current higher than 1 mA is required, a 33 V Zener diode from the VCC pin to the GND pin can be used to protect the IC. In that case, the internal OVP cannot work anymore because the Zener keeps the VCC below 33 V. An external OVP at a slightly lower voltage, for example 30 V, must replace the internal OVP.

### 4.1.5 PCB layout

The VCC pin must not be treated as a small signal pin because the relatively high current to charge the gate of the MOSFET also passes through this pin. Keep the loop from the positive terminal of the VCC capacitor to the VCC pin, via the DRIVER pin, to the gate of the MOSFET, and via the source of the MOSFET back to the negative terminal of the VCC capacitor, as small as possible.

## 4.2 CTRL pin

A capacitor of 1 nF on the CTRL pin is a good value for most applications.

If the capacitor is much larger, it responds too slowly to load transients.

If the capacitor is much smaller, the control loop can become unstable and sensitive to disturbances.

3. Above a certain current, the clamp behaves like a current source. The voltage increases and the current remains constant.


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In the layout, treat both the ground and the collector connections of the optocoupler to the CTRL pin as small signal tracks. To minimize disturbance, avoid additional currents through these tracks.

## 4.3 DRIVER pin

The source and sink currents on the DRIVER pin can be high. The source current also rushes through pin VCC and the sink current through the GND pin. The PCB layout requires extra attention to avoid large loops.

## 4.4 ISENSE pin

### 4.4.1 General application recommendations

Place $R_{ovp}$ and $R_{opc}$ (see Figure 24) close to the ISENSE pin. It helps to filter out disturbances.

Do not place a capacitor directly on the ISENSE pin. The voltage during the secondary stroke can be as high as 2.5 V. However, the voltage during the primary stroke is below 500 mV. So, at the end of the secondary stroke, the voltage on the ISENSE pin must drop quickly. A capacitor slows this discharge down. It also causes a delay in the peak current measurement (much more than in an application with TEA1733/TEA1738 because $R_{ocp}$ is not bypassed by a capacitor). Extra delay is unwanted because it has the opposite effect as the high/low line compensation. Place $R_{opc}$ and $R_{ovp}$ close to the IC to keep the parasitic capacitance on the ISENSE pin low.

### 4.4.2 Configuration order

The ISENSE pin combines three functions on one pin. To avoid unnecessary iterations, these functions must be configured in the right order.

1. At low mains, adjust $R_{ISENSE}$ to obtain the required OPP level.
2. At high mains, adjust $R_{opc}$ to obtain the required amount of high/low line compensation
3. Adjust $R_{ovp}$ to obtain the required OVP level

**Remark:** Changing brownin/brownout resistor also changes high/low line compensation. So, after changing brownin/brownout resistor, high/low line compensation must also be changed.

### 4.4.3 Configuring the current sense resistor

Calculate the maximum primary peak current before the correct value of the current sense resistor is calculated (Equation 7 or Equation 8).

In DCM:

$$I_{peak(max)} = \sqrt{\frac{2 \times P_{o(max)}}{\eta \times L \times f_{sw}}} \quad (7)$$


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In CCM:

$$I_{peak(max)} = \frac{P_{o(max)}}{\eta} \times \frac{V_i + NV_o}{V_i \times NV_o} + \frac{1}{2 \times L \times f_{sw}} \times \frac{V_i \times NV_o}{V_i + NV_o} \quad (8)$$

Where:

- $I_{peak(max)}$ is the maximum continuous primary peak current, the peak current at which the OPP triggers
- $P_{o(max)}$ is the maximum continuous output power, the output power at which the OPP triggers
- $\eta$ is the expected efficiency of the flyback at maximum output power
- $V_i$ is the minimum rectified mains voltage (= $\sqrt{2} \times$ the minimum mains voltage) at which the supply must be able to deliver the maximum continuous output power[4].
- N is the winding ratio of the transformer
- $V_o$ is the output voltage
- $f_{sw}$ is the switching frequency, in this case 65 kHz

Now the (maximum) current sense resistor value can be calculated with Equation 9:

$$R_{ISENSE} = \frac{V_{th(sense)opp}}{I_{peak(max)}} = \frac{400\ mV}{I_{peak(max)}} \quad (9)$$

Where:

- $V_{th(sense)opp}$ is the overpower protection threshold voltage on the ISENSE pin
- $I_{peak(max)}$ is the maximum continuous primary peak current, the peak current at which the OPP triggers

Another way to determine the correct value for the sense resistor is by trial and error:

1. Connect a load to the output.
2. Apply the minimum mains voltage at which the supply must be able to deliver the maximum continuous output power.
3. Increase the load to maximum nominal power. If the OPP kicks in before, decrease the value of the $R_{sense}$ resistor until the nominal power can be delivered. If OPP does not kick in, increase the value of the $R_{sense}$ resistor until the OPP is triggered.
4. Finally, decrease the value of the $R_{sense}$ resistor by about 5 % to keep some margin for normal operation.

The sense resistor must be accurate (1 %) and have a low inductance. Splitting the sense resistance into two or three parallel resistors not only makes it easier to implement the desired resistance and power rating but it also helps to reduce the inductance.

4. The peak current is larger during the valley of the mains ripple. During normal operation, the OPP threshold can already be exceeded during the valleys of the ripple on the bulk capacitor voltage. However, it does not trigger the OPP. As long as the threshold is not exceeded during the tops of the bulk capacitor ripple voltage, the OPP time-out counter is reset each 8.33 ms or 10 ms. It never reaches the 27.5 ms (TEA1833TS)/160 ms (TEA1833LTS) OPP time-out. The OPP can only trigger if the OPP threshold is exceeded throughout the entire mains cycle.


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### 4.4.4 Calculating the maximum temporary peak output power

The maximum instantaneous primary peak current can now be calculated with Equation 10:

$$I_{peak(M)(max)} = \frac{V_{ctrl(Ipeak)max}}{R_{ISENSE}} = \frac{575\ mV}{R_{ISENSE}} \quad (10)$$

Where:

- $V_{ctrl(Ipeak)max}$ is the maximum peak control voltage on the ISENSE pin

Now the maximum temporary peak output power can be calculated[5].

In DCM:

$$P_{o(M)(max)} = \eta \times \frac{1}{2} \times L \times (I_{peak(M)(max)})^2 \times f_{sw} \quad (11)$$

In CCM:

$$P_{o(M)(max)} = \eta \times \frac{V_i \times NV_o}{V_i + NV_o} \times \left(I_{peak(M)(max)} - \frac{V_i \times NV_o}{2 \times L \times f_{sw} \times (V_i + NV_o)}\right) \quad (12)$$

Where:

- $\eta$ is the expected efficiency of the flyback at maximum output power
- $I_{peak(M)(max)}$ is the maximum instantaneous primary peak current, limited by the OCP
- $f_{sw}$ is the switching frequency, in this case 130 kHz, the "peak power" area of the frequency curve, see Figure 7
- $V_i$ is the value of the rectified mains voltage during the valley of the ripple

This value is the maximum temporary peak output power at which the output voltage remains intact.

If the temporary peak output power is not high enough, it can only be increased by decreasing the current sense resistor value. Decreasing the current sense resistor value also increases the maximum continuous output power.

### 4.4.5 Tuning the OPP compensation ($R_{opc}$)

The value of $R_{opc}$ determines the amount of overpower compensation (see Section 3.4.8.3 and Figure 13). The ISENSE pin generates a current $I_{opc}$ from 0 μA to 6 μA. This current depends on $V_{bulk}$ of the mains capacitor. The voltage drop over $R_{opc}$ reduces the actual peak level over resistor $R_{sense}$ at switch-off.

The amount of compensation required depends on the value of the current sense resistor. So the current sense resistor must be chosen first.

5. Calculating the maximum temporary output power is complicated because it depends on the mains ripple on the bulk capacitor, which itself depends on the output power.


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Steps for trimming the overpower compensation:

1. Start with a 6.8 kΩ for resistor $R_{opc}$.
2. Apply the minimum mains voltage at which the supply must be able to operate.
3. Measure the maximum output power by slowly increasing the load until the OPP is triggered.
4. Apply the maximum mains voltage at which the supply must be able to operate.
5. Measure the maximum output power by slowly increasing the load until the OPP is triggered.
6. Increase the $R_{opc}$ value if the maximum output power at high input voltage is higher than the maximum output power at low input voltage (not sufficiently compensated). Decrease the $R_{opc}$ value if the maximum output power at high input voltage is lower than the maximum output power at low input voltage (overcompensated).
7. Repeat steps 2 to 6 until the maximum output power at high and low input voltage is equal.

**Remarks:**

- The output power as a function of the input voltage is not a linear function. When the maximum output power has been tuned to be equal for both the absolute minimum input voltage (90 V (AC)) and the absolute maximum input voltage (264 V (AC)), the actual maximum output power is slightly higher between these limits.
- The external overvoltage protection also depends on $R_{opc}$. So, after changing $R_{opc}$, adjusting $R_{ovp}$ is also required (see Section 4.4.6)

### 4.4.6 Calculating the effect of the OPP compensation

The resulting peak current reduction of the OPP compensation can be calculated with Equation 13:

$$\Delta I_{peak} = \frac{(I_{opc} \times R_{opc})}{R_{sense}} \quad (13)$$

Where:

- $\Delta I_{peak}$ is the peak current reduction
- $R_{sense}$ is the value of the current sense resistor (R11 in Figure 1)

Section 4.4.3 describes how to calculate the peak current and the resulting output power without input voltage compensation. $\Delta I_{peak}$ must be subtracted from the peak current before calculating the maximum output power. This subtraction is required to calculate the output power with input voltage compensation.

### 4.4.7 Disabling the overpower protection

Unlike in the TEA1733 series or the TEA1738 series, the overpower protection in the TEA1833(L)TS cannot be disabled because it is fully integrated in the IC. If the internal OPP is not required because, for example, a secondary IC handles the overpower protection, the internal OPP level can be shifted to a higher power by lowering the current sense resistor. Do not decrease the $R_{sense}$ value too much because:


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- Controlling a relatively high power using only a fraction of the CTRL range results in a very high gain and can cause instability.
- Skipping part of the peak current reduction means that it is not sufficiently reduced before entering the VCO mode. It can cause audible noise. Normally, the peak current is first reduced by a factor 3 before the frequency enters the audible spectrum.

### 4.4.8 Calculating the OVP

The resistor for adjusting the OVP can be calculated with:

$$R_{ovp} = R_{ocp} \cdot \left( \frac{\frac{N_{aux}}{N_{sec}} \cdot (V_{out(ovp)} + V_{F(sec)}) - V_{F(aux)}}{V_{ovp(ISENSE)}} - 1 \right) \quad (14)$$

Where:

- $V_{out(ovp)}$ is the output voltage at which the OVP should be triggered
- $V_{F(sec)}$ is the forward voltage of the secondary diode
- $V_{F(aux)}$ is the forward voltage of $D_{ovp}$
- See Figure 24 for $R_{ovp}$ and $R_{opc}$
- $V_{ovp(ISENSE)}$ is the OVP detection level of the ISENSE pin (= 2.5 V)

Example:

- $R_{opc}$ = 6.8 kΩ
- $V_{out(ovp)}$ = 24 V
- $V_{F(sec)} = V_{F(aux)}$ = 0.6 V
- $N_{aux} = N_{sec}$ = 8 turns

The result: $R_{ovp} = 6.8\ k\Omega \cdot \left( \frac{\frac{8\ turns}{8\ turns} \cdot (24\ V + 0.6\ V) - 0.6\ V}{2.5\ V} - 1 \right) = 58.5\ k\Omega$


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## 4.5 PROTECT pin

### 4.5.1 Mains detection

To measure $V_{bulk}$ of the mains electrolytic capacitor, connect a high-ohmic resistor (20 MΩ) from the positive terminal of C1 to the pin. The voltage at C1 ranges up to 375 V (DC). Because the maximum voltage over 1206 resistors is 200 V (DC), it is best to place two resistors of 10 MΩ in series. To avoid disturbance pickup, place the resistors as close as possible to the PROTECT pin. During the mains detection measurement, the PROTECT pin is clamped to 260 mV (typical).

To minimize the error in the measured mains detection current, select a low reverse leakage type[6] for diode D6. The NXP BAS416 is suited for this purpose.

### 4.5.2 External OverTemperature Protection (OTP)

The external OTP function is designed for use with a 100 kΩ NTC. The NTC is connected to ground and via a series resistor + a low leakage diode to the PROTECT pin. To filter disturbance, a 1 nF capacitor is connected from the cathode of the diode to ground. During the measurement, 200 μA current flows out of the pin. OTP is detected when the level on the PROTECT pin during the measurement remains below 2 V (typical). The voltage over the NTC + series resistor is then 1.45 V, assuming a 0.55 V drop over the diode in series. This voltage/current equals a resistor value of 7.25 kΩ. To tune the OTP point, the value of the series resistor can be adapted. When $R_{series}$ is zero, the trigger point is around 87 °C. For $R_{series}$ = 1.8 kΩ, it is around 95 °C. For $R_{series}$ = 3.3 kΩ, it reaches 105 °C. All values given are typical and for indication only.

The NTC is often placed near the hottest component on the PCB, which is not always close to the IC. The long PCB track from NTC to the PROTECT pin can act as an antenna and pick up disturbances. A filter against such disturbances can be constructed without additional components by placing the series resistor (which is often required anyway) between the NTC and the PROTECT pin and as close as possible to the pin.

## 4.6 GND pin

Do not treat the GND pin as a small signal ground because the DRIVER discharge current also flows through this pin.

6. Because the diode is used in a forward direction, low reverse leakage may not seem an important parameter for a diode in this application. However, a low leakage diode is preferred here because of its higher forward voltage at low forward currents. To ensure that during the brownin/brownout measurement the entire measurement current flows into the PROTECT pin and not into the diode, the forward current must be negligible at 0.26 V forward voltage and at high temperatures.


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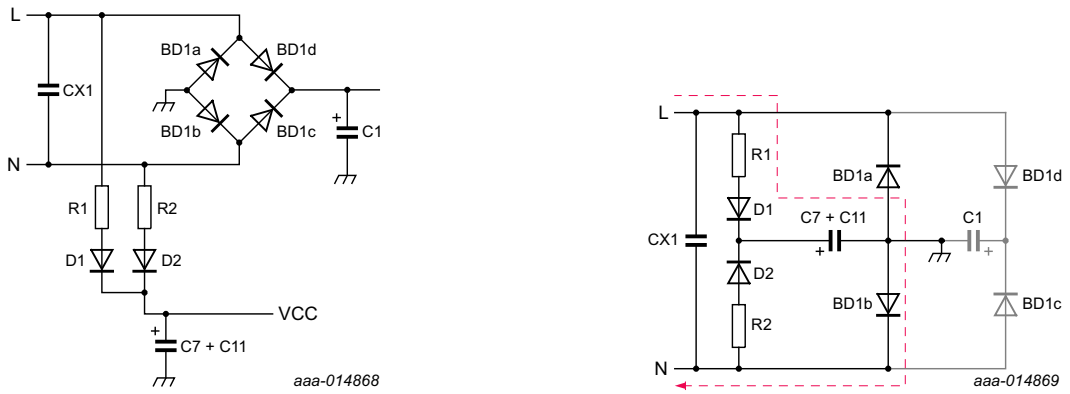
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# 5. Start-up circuit

## 5.1 Start-up circuit with two resistors and two diodes

Figure 27(a) shows a simple circuit with good performance which not only caters for start-up but also for X-capacitor discharge.

Figure 27(b) shows the circuit shown in Figure 27(a) but drawn to show more clearly how the $V_{CC}$ capacitor is charged.




a. Start-up circuit using diodes in series

b. Simplified representation

**Fig 27. Start-up circuits**

Once the bulk capacitor C1 is fully charged, the diodes of the bridge stop conducting. During the positive half of the mains, current flows from the L terminal through resistor R1, diode D1, capacitor C11 + C7, and bridge rectifier BD1b to the N terminal, charging C11 + C7. Diode D2 prevents that R2 discharges C11 + C7 during the positive half. During the negative half of the mains, resistor R2, diode D2, capacitor C11 + C7, and bridge rectifier BD1a form the current charging path. Diode D1 prevents discharge by R1.

The charge current into the VCC capacitor approximately can be calculated with Equation 15:

$$I_{ch} = \frac{\left(\frac{2}{\pi} \times \sqrt{2} \times V_{mains} - V_{CC}\right)}{R1} - I_{CC(startup)} \quad (15)$$

Where:

- $V_{mains}$ is the effective mains voltage
- $I_{CC(startup)}$ is the supply current of the IC in power-down mode (11 μA)

When $V_{CC}$ = 11 V, the average over the charge period (0 V to $V_{startup}$), the charge current for R1 = R2 = 2.4 MΩ at 90 V (AC) equals:

$$I_{ch} = \frac{\left(\frac{2}{\pi} \times \sqrt{2} \times 90\ V - 11\ V\right)}{2.4\ M\Omega} - 11\ \mu A = 29 \times 10^{-6} - 11 \times 10^{-6} = 18\ \mu A$$


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The diodes do not block the X-capacitor discharge path. The discharge of the X-capacitor takes place via resistor R1 or R2 through the series diode to the VCC pin. From the VCC pin, there are several paths to ground. Even when the IC is in power-down mode a clamp on the VCC pin is active. From ground, it can find its return path to the X-capacitor through one of the bridge diodes.

For discharging the X-capacitor, the RC time constant must be < 1 s. For an X-capacitor of 220 nF, it means a maximum value for resistors R1 and R2 of 4.5 MΩ. For 330 nF, it means a maximum 3 MΩ. Table 4 contains for some start-up resistors and their performance in a 65 W application.

**Table 4. Start-up resistors and their performance**

| $R_{startup}$ (MΩ) | $t_{startup}$ (s) | | $P_{noload}$ (mW) at 230 V (AC) |
|---|---|---|---|
| | 90 V (AC) | 115 V (AC) | |
| 1 | 0.72 | 0.52 | 80 |
| 1.5 | 1.13 | 0.80 | 64 |
| 2 | 1.57 | 1.12 | 59 |
| 2.4 | 1.99 | 1.34 | 53 |
| 2.7 | 2.37 | 1.57 | 52 |
| 3 | 2.77 | 1.77 | 51 |

Selecting the best value for the start-up resistor is a balance between start-up time and no-load input power, taking into account the maximum allowed value for discharging the X-capacitor.

When cost is premium and start-up time or no-load power is less important, it is possible to omit the two diodes D1 and D2. The circuit still works fine. However, while one start-up resistor is providing the charge current, the other is loading the $V_{CC}$ capacitor and draining off part of the charge current.

This has a negative effect on the start-up time. For 90 V (AC), the start-up time increases about 20 %, for 115 V (AC) about 10 %.

Example: $I_{ch}$ = 18 μA at $R_{startup}$ = 2.4 MΩ (see Figure 27). $I_{dch}$ = 4.6 μA (take the average value of $V_{CC}$). The available charge current for the VCC capacitor decreases with 25 %.

The voltage rating of most 1206 resistors is only 200 V. For 230 V (AC) applications, the voltage across the start-up resistors can become nearly 400 V. If SMD type resistors are used, resistors R1 and R2 must each be split into two resistors in series.


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## 5.2 Measuring start-up time

Capacitance across the bridge diodes changes the wave shape of the voltage before the bridge rectifier regarding the primary ground. It can significantly decrease the start-up time. Depending on the capacitance of the mains supply to ground, connecting the ground clip of an oscilloscope to the primary ground of the flyback converter can add a few nF across the bridge diodes.

Make sure that the board has no capacitive coupling to primary ground, so the correct worst case start-up time is measured:

- Use a current probe in the mains input cable to detect mains switch-on.
- The same current probe in the mains input cable can also be used to detect when the supply starts switching. The time, from the moment the supply starts to switch until it reaches 90 % of the output voltage, is only a few milliseconds. It can be ignored regarding the total start-up time. If it is required to measure the output voltage with an oscilloscope, remove the Y-cap so that there is no capacitive coupling to primary ground.
- Use a resistor load instead of an electronic load. Remove the Y-cap if electronic load must be used.

Also important when measuring the start-up time:

- Make sure that the VCC capacitor is entirely discharged before starting a measurement.
- Do not connect a probe or multimeter to the VCC. Even a 10 MΩ impedance influences the measurement.


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# 6. Layout recommendations

The component numbers used in this section refer to the schematic diagram (see Figure 1).

## 6.1 Input section

- Keep the mains tracks (L and N) low ohmic and close to each other to avoid loops.
- Position common-mode chokes away from the power section (MOSFET and transformer) and from each other to prevent magnetic coupling to any of the other components.
- Keep tracks from the bridge rectifier to capacitor C1 low ohmic and close to each other.

## 6.2 Power section

- The connection from the negative terminal of the bridge rectifier to the current sense resistor R11 must be routed via capacitor C1.
- The connection from the positive terminal of the bridge rectifier to the transformer must be routed via capacitor C1.
- Keep the cross section of the loop from capacitor C1 via the transformer, MOSFET Q1 and current sense resistor R11 back to capacitor C1 as small as possible.
- Place capacitor C2 close to capacitor C1.
- Place peak clamp circuit consisting of resistors R9 and R10, capacitor C3 and diode D1 close to the transformer and away from the TEA1833(L)TS.
- If MOSFET Q1 has a metal tab, insulate it from the heat sink. Connect the heat sink to the primary power ground.

## 6.3 Auxiliary winding

- Place rectifier diode D3, coil L1, VCC capacitor C11, and the network, consisting of resistor R18 and capacitor C12, close to the auxiliary winding.
- The connection of the ground of the auxiliary winding to the central signal ground point must go via capacitor C11. Use a separate track to avoid the noise in this ground causing noise in the PROTECT pin, the ISENSE pin, etc.
- Connect the central signal ground with a low-ohmic track to the central power ground (capacitor C1).
- Keep the cross section of the loop from the auxiliary winding (via diode D3 and coil L1) to VCC capacitor C11 and back to the auxiliary winding as small as possible. The same applies for the network R18/C12.


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## 6.4 Flyback controller

- Place the TEA1833(L)TS away from the transformer and MOSFET Q1.
- Keep the connection from current sense resistor R11 to the TEA1833(L)TS close to the ground track.
- Place VCC decoupling capacitor C7 close to the VCC pin.
- The connection from the VCC pin to VCC capacitor C11 must be routed via VCC decoupling capacitor C7.
- The connection from the GND pin to the central signal ground must be routed via VCC decoupling capacitor C7.
- Place resistors R13 and R13a close to the ISENSE pin.
- Place resistors R4 and R5 close to the PROTECT pin.
- Place diode D4a, capacitor C10, and resistor R17 close to the PROTECT pin as well. The other terminal of capacitor C10 must have a short connection to the GND pin.
- Place capacitor C9 close to the CTRL pin.

## 6.5 Mains insulation

- Keep at least 6 mm distance between the copper tracks of the primary and the secondary side.
- Place Y-cap CY1 close to the transformer.

## 6.6 Secondary side

- Heat sink secondary diode D5:

  Connect the metal tab (which is internally connected to the cathode) directly to the heat sink. Connect the heat sink to the positive output track. If the diode has no metal tab, the heat sink can be connected to ground or to the positive output track.
- Keep the cross section of the loop from the transformer via diode D5 and capacitors C13 and C14 back to the transformer as small as possible. Keep output tracks close to each other.
- Use a separate signal ground for resistor R24 and shunt regulator U3. Connect the signal ground from resistor R24 and shunt regulator U3 via capacitor C19 to the power ground at capacitors C13 and C14.
- Place capacitor C19 close to resistors R20 and R23.
- The connection of resistors R20 and R23 to the positive output voltage must go via capacitor C19 to capacitors C13 and C14.
- Place the shunt regulator U3 and surrounding components away from transformer.


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# 7. Abbreviations

**Table 5. Abbreviations**

| Acronym | Description |
|---|---|
| CCM | Continuous Conduction Mode |
| CDM | Charged Device Model |
| DCM | Discontinuous Conduction Mode |
| EMI | ElectroMagnetic Interference |
| LEB | Leading-Edge Blanking |
| NTC | Negative Temperature Coefficient |
| OCP | OverCurrent Protection |
| OPP | OverPower Protection |
| OSCP | Output Short Circuit Protection |
| OTP | OverTemperature Protection |
| OVP | OverVoltage Protection |
| PFC | Power Factor Corrector |
| SMPS | Switched Mode Power Supply |
| UVLO | UnderVoltage LockOut |
| VCO | Voltage Controlled Oscillator |

# 8. References

**[1] TEA1833TS data sheet —** *GreenChip SMPS control IC*

**[2] TEA1833LTS data sheet —** *GreenChip SMPS control IC*


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