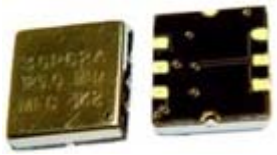
SMD LVDS output
11.4 x 9.6 x 2.5 mm



RoHS Compliance

Features

- Tri-state function available on pad No. 2.

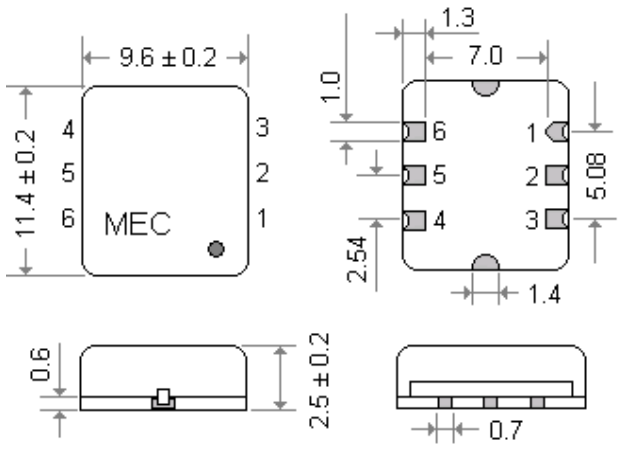
Applications

- For high frequency LVDS output clock oscillators .
- " HDW " use a high-Q fundamental crystal and a multiplier circuit for low cost applications.

General Specifications

Paramenters		Electrical Spec.							
Input Voltage (V_{DD})		3.3 V ± 5 %							
Frequency Range / Load		750 KHz ~ 800,0 MHz							
Output Wave Form		LVDS output							
Output Logic High " 1 "	typical	1.43 V (RL = 100 Ω)							
	max.	1.60 V (RL = 100 Ω)							
Output Logic Low " 0 "	min.	0.9 V (RL = 100 Ω)							
	typical	1.1 V (RL = 100 Ω)							
Integrated Phase Noise (12 KHz to 20 MHz)		2.6 ps (typical) ; 4.0 ps (max.)							
Rise Time (Tr) / Fall Time (Tf)		0.6n sec.(typical) ; 1.5 n sec. (max.)							
Output Voltage Swing		350 mV min. (V_{DD} = +2.5V)							
Duty Cycle		50% ± 10% [50% ± 5% is also available]							
Load		50 Ω into Vcc - 2V or Thevenin equivalent							
Current Consumption (15 pF load)		< 24.0 MHz		24.1 ~ 96.0 MHz		96.1 ~ 800.0 MHz			
		25 mA (max.)		65 mA (max.)		100 mA (max.)			
Start - Up Time (Ts)		10 m sec.(typical)							
Storage Temperature		- 50°C to 100°C							
Aging		± 3 ppm per year (max.)							
Frequency Stability [1] Codes	Frequency Stability over Operating Temperature Range	± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " For example : " C20 " ±20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C				
	Commercial (*-10°C to +70°C*)	*A*	*B*	*C*					
	Industrial (*-40°C to +85°C*)	*D*	*E*	*F*					
Phase Noise (typical) [156.250 MHz]		Offset	10 Hz	100 Hz	1K Hz	10 KHz	100KHz	1 MHz	10 MHz
		dBc / Hz	-60	-90	-115	-125	-119	-120	-140

Outline Dimensions (Unit : mm)



Pad Connections			
1	Tri - state	4	Output
2	No Connection	5	Complimentary output
3	Ground	6	Supply Voltage