



# THS7530-Q1 高速、全差分、连续 可变增益放大器

## 1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 分类等级 2
  - 器件组件充电模式 (CDM) 分类等级 C6
- 低噪声： $V_n = 1.1\text{nV}/\sqrt{\text{Hz}}$ ，  
噪声系数 = 9dB
- 低失真：
  - 频率为 32MHz 时： $\text{HD}_2 = -65\text{dBc}$ ， $\text{HD}_3 = -61\text{dBc}$
  - 频率为 70MHz 时： $\text{IMD}_3 = -62\text{dBc}$ ， $\text{OIP}_3 = 21\text{dBm}$
- 300MHz 带宽
- 连续可变增益范围：11.6dB 至 46.5dB
- 增益斜率：38.8dB/V
- 全差分输入和输出
- 输出共模电压控制
- 输出电压限制

## 2 应用

- 超声波应用、声纳和雷达中的时间增益放大器
- 通信和和视频中的自动增益控制

- 通信中的系统增益校准
- 仪表中的可变增益

## 3 说明

THS7530-Q1 器件采用德州仪器 (TI) 先进的 BiCom III SiGe 互补双极工艺制造。THS7530-Q1 是一款带有压控增益的直流耦合高带宽放大器。该放大器具有高阻抗差分输入和低阻抗差分输出，提供高带宽增益控制、输出共模控制和输出电压钳位功能。

该器件在 300MHz 带宽下

的动态性能优异。当频率为 32MHz，同时将 1 V<sub>PP</sub> 输出施加于 400Ω 负载，三次谐波失真为 -61dBc。

增益控制（单位：dB）呈线性变化。在 0V 至 0.9V 电压范围内，增益以 38.8dB/V 的斜率由 11.6dB 变化为 46.5dB。

输出电压限制功能用于限制输出电压摆幅并避免后续级发生饱和。

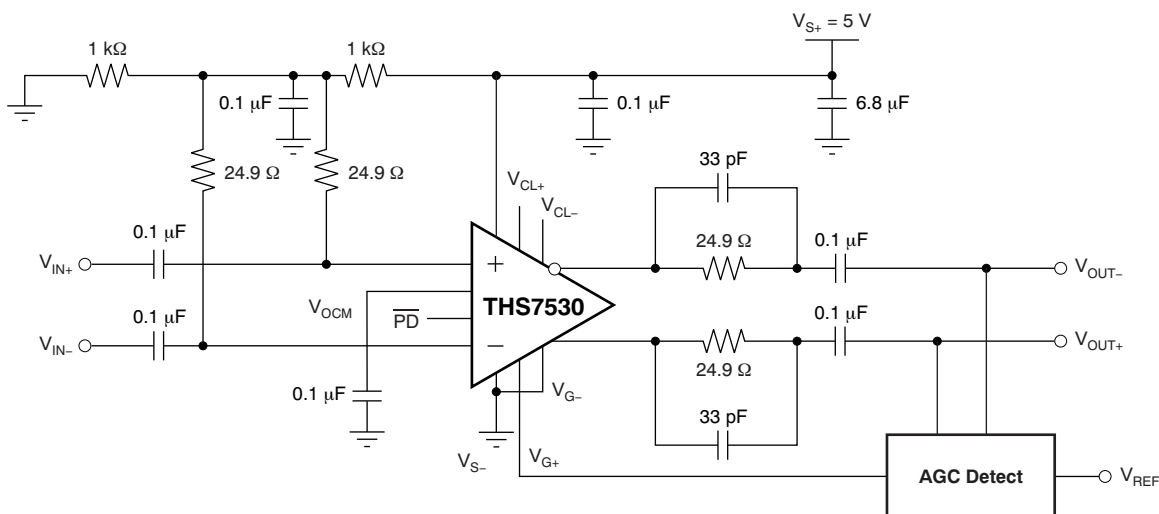
该器件可在汽车级温度范围内（-40°C 至 +125°C）额定运行。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
THS7530-Q1	HTSSOP (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	8.3	Feature Description .....	<b>11</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	8.4	Device Functional Modes .....	<b>12</b>
<b>3</b>	<b>说明</b> .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>13</b>
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	9.1	Application Information .....	<b>13</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	9.2	Typical Application .....	<b>15</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>17</b>
6.1	Absolute Maximum Ratings .....	<b>4</b>	<b>11</b>	<b>Layout</b> .....	<b>18</b>
6.2	ESD Ratings .....	<b>4</b>	11.1	Layout Guidelines .....	<b>18</b>
6.3	Recommended Operating Conditions .....	<b>4</b>	11.2	Layout Examples .....	<b>20</b>
6.4	Thermal Information .....	<b>4</b>	<b>12</b>	<b>器件和文档支持</b> .....	<b>22</b>
6.5	Electrical Characteristics: Main Amplifier .....	<b>5</b>	12.1	器件支持 .....	<b>22</b>
6.6	Package Thermal Data .....	<b>6</b>	12.2	文档支持 .....	<b>22</b>
6.7	Typical Characteristics .....	<b>7</b>	12.3	社区资源 .....	<b>22</b>
<b>7</b>	<b>Parameter Measurement Information</b> .....	<b>10</b>	12.4	商标 .....	<b>22</b>
7.1	Test Circuits .....	<b>10</b>	12.5	静电放电警告 .....	<b>22</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>11</b>	12.6	Glossary .....	<b>22</b>
8.1	Overview .....	<b>11</b>	<b>13</b>	<b>机械、封装和可订购信息</b> .....	<b>22</b>
8.2	Functional Block Diagram .....	<b>11</b>			

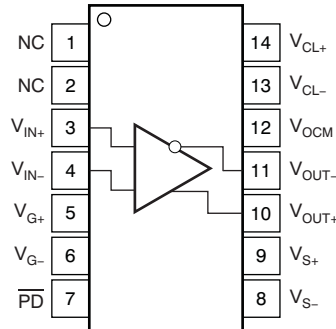
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	注释
2015 年 12 月	*	最初发布版本。

## 5 Pin Configuration and Functions

**PWP Package**  
**14-Pin HTSSOP With PowerPAD™**  
**Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1	—	No internal connection
	2		
$\overline{\text{PD}}$	7	—	Power down, $\overline{\text{PD}}$ = logic low puts the device into low power mode; $\overline{\text{PD}}$ = logic high or open for normal operation
$V_{\text{CL-}}$	13	I	Output negative clamp voltage input
$V_{\text{CL+}}$	14	I	Output positive clamp voltage input
$V_{\text{G-}}$	6	I	Gain setting negative input
$V_{\text{G+}}$	5	I	Gain setting positive input
$V_{\text{IN-}}$	4	I	Inverting amplifier input
$V_{\text{IN+}}$	3	I	Noninverting amplifier input
$V_{\text{OCM}}$	12	I	Output common-mode voltage input
$V_{\text{OUT-}}$	11	O	Inverted amplifier output
$V_{\text{OUT+}}$	10	O	Noninverted amplifier output
$V_{\text{S-}}$	8	I	Negative amplifier power-supply input
$V_{\text{S+}}$	9	I	Positive amplifier power-supply input

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{S+} - V_{S-}$	Supply voltage		5.5	V
$V_I$	Input voltage		$\pm V_S$	V
$I_O$	Output current		65	mA
$V_{ID}$	Differential input voltage		$\pm 4$	V
	Continuous power dissipation	See <a href="#">Thermal Information</a>		
$T_J$	Maximum junction temperature		150	°C
	Maximum junction temperature for long term stability <sup>(2)</sup>		125	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$\pm 2000$
		Charged-device model (CDM), per AEC Q100-011	$\pm 1000$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$[V_{S-} \text{ to } V_{S+}]$	Supply voltage	4.5	5	5.5	V
	Input common mode voltage	$[V_{S-} \text{ to } V_{S+}] = 5 \text{ V}$			V
	Output common mode voltage	$[V_{S-} \text{ to } V_{S+}] = 5 \text{ V}$			V
$T_A$	Operating free-air temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THS7530	UNIT
		PWP (HTSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	28.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: Main Amplifier

$V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = 2.5\text{ V}$ ,  $V_{ICM} = 2.5\text{ V}$ ,  $V_{G-} = 0\text{ V}$ ,  $V_{G+} = 1\text{ V}$  (maximum gain),  $T_A = 25^\circ\text{C}$ , AC performance measured using the AC test circuit shown in [Figure 16](#) (unless otherwise noted). DC performance is measured using the DC test circuit shown in [Figure 17](#) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC PERFORMANCE</b>					
Small-signal bandwidth	All gains, $P_{IN} = -45\text{ dBm}$		300		MHz
Slew rate <sup>(1)</sup>	1- $V_{PP}$ Step, 25% to 75%, minimum gain		1250		V/ $\mu\text{s}$
Settling time to 1% <sup>(1)</sup>	1- $V_{PP}$ Step, minimum gain		11		ns
Harmonic distortion, 2nd harmonic	$f = 32\text{ MHz}$ , $V_{O(PP)} = 1\text{ V}$ , $R_{L(diff)} = 400\ \Omega$		-65		dBc
Harmonic distortion, 3rd harmonic	$f = 32\text{ MHz}$ , $V_{O(PP)} = 1\text{ V}$ , $R_{L(diff)} = 400\ \Omega$		-61		dBc
Third-order intermodulation distortion	$P_O = -10\text{ dBm}$ each tone, $f_C = 70\text{ MHz}$ , 200-kHz tone spacing		-62		dBc
Third-order output intercept point	$f_C = 70\text{ MHz}$ , 200-kHz tone spacing		21		dBm
Noise figure (with input termination)	Source impedance: $50\ \Omega$		9		dB
Total input voltage noise	$f > 100\text{ kHz}$		1.1		nV/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE—INPUTS</b>					
Input bias current	$T_A = 25^\circ\text{C}$		20	39	$\mu\text{A}$
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			40	
Input bias current offset			<150		pA
Minimum input voltage	Minimum gain, $T_A = 25^\circ\text{C}$		1.5	1.6	V
	Minimum gain, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			1.7	
Maximum input voltage	Minimum gain, $T_A = 25^\circ\text{C}$	3.2	3.3		V
	Minimum gain, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	3.15			
Common-mode rejection ratio	$T_A = 25^\circ\text{C}$	56	114		dB
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	44			
Differential input impedance			8.5    3		k $\Omega$    pF
<b>DC PERFORMANCE—OUTPUTS</b>					
Output offset voltage	All gains, $T_A = 25^\circ\text{C}$		$\pm 100$	$\pm 410$	mV
	All gains, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 480$	
Maximum output voltage high	$T_A = 25^\circ\text{C}$	3.25	3.5		V
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	3			
Minimum output voltage low	$T_A = 25^\circ\text{C}$		1.5	1.8	V
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2	
Output current	$T_A = 25^\circ\text{C}$	$\pm 16$	$\pm 30$		mA
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$\pm 16$			
Output impedance			15		$\Omega$
<b>OUTPUT COMMON-MODE VOLTAGE CONTROL</b>					
Small-signal bandwidth			32		MHz
Gain			1		V/V
Common-mode offset voltage	$T_A = 25^\circ\text{C}$		4.5	12	mV
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			13.8	
Minimum input voltage			1.75		V
Maximum input voltage			3.25		V
Input impedance			25    1		k $\Omega$    pF
Default voltage, with no connect			2.5		V
Input bias current			<1		$\mu\text{A}$
<b>GAIN CONTROL</b>					
Gain control differential voltage range	$V_{G+}$		0 to 1		V
Minus gain control voltage	$V_{G-} - V_{S-}$		-0.6 to 0.8		V
Minimum gain	$V_{G+} = 0\text{ V}$		11.6		dB
Maximum gain	$V_{G+} = 0.9\text{ V}$		46.5		dB
Gain slope	$V_{G+} = 0\text{ V}$ to $0.9\text{ V}$		38.8		dB/V

(1) Slew rate and settling time measured at amplifier output.

## Electrical Characteristics: Main Amplifier (continued)

$V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = 2.5\text{ V}$ ,  $V_{ICM} = 2.5\text{ V}$ ,  $V_{G-} = 0\text{ V}$ ,  $V_{G+} = 1\text{ V}$  (maximum gain),  $T_A = 25^\circ\text{C}$ , AC performance measured using the AC test circuit shown in [Figure 16](#) (unless otherwise noted). DC performance is measured using the DC test circuit shown in [Figure 17](#) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain slope variation	$V_{G+} = 0\text{ V to } 0.9\text{ V}$		$\pm 1.5$		dB/V
Gain error	$V_{G+} = 0\text{ V to } 0.15\text{ V}$		$\pm 4$		dB
	$V_{G+} = 0.15\text{ V to } 0.9\text{ V}$		$\pm 2.25$		
Gain control input bias current			$< 1$		$\mu\text{A}$
Gain control input resistance			40		$\text{k}\Omega$
Gain control bandwidth	Small signal $-3\text{ dB}$		15		MHz
VOLTAGE CLAMPING					
Output voltages ( $V_{\text{OUT}\pm}$ ) relative to clamp voltages ( $V_{\text{CL}\pm}$ )	Device in voltage limiting mode, $T_A = 25^\circ\text{C}$		$\pm 25$	$\pm 40$	mV
	Device in voltage limiting mode, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			$\pm 180$	
Clamp voltage ( $V_{\text{CL}\pm}$ ) input resistance	Device in voltage limiting mode		3.3		$\text{k}\Omega$
Clamp voltage ( $V_{\text{CL}\pm}$ ) limits			$V_{S-}$ to $V_{S+}$		V
POWER SUPPLY					
Specified operating voltage	$T_A = 25^\circ\text{C}$		5	5.5	V
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			5.5	
Maximum quiescent current	$T_A = 25^\circ\text{C}$		40	48	mA
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			49	
Power supply rejection ( $\pm\text{PSRR}$ )	$T_A = 25^\circ\text{C}$	70	77		dB
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	45			
POWER DOWN					
Enable voltage threshold	TTL low = shut down, $T_A = 25^\circ\text{C}$		1.4		V
	TTL low = shut down, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$	1			
Disable voltage threshold	TTL high = normal operation, $T_A = 25^\circ\text{C}$		1.4		V
	TTL high = normal operation, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			1.65	
Power-down quiescent current	$T_A = 25^\circ\text{C}$		0.35	0.4	mA
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			0.55	
Input current high	$T_A = 25^\circ\text{C}$		$\pm 9$	$\pm 16$	$\mu\text{A}$
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			$\pm 19$	
Input current low	$T_A = 25^\circ\text{C}$		$\pm 109$	$\pm 116$	$\mu\text{A}$
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			$\pm 130$	
Input impedance			$50\parallel 1$		$\text{k}\Omega\parallel\text{pF}$
Turnon time delay	Measured to 50% quiescent current		820		ns
Turnoff time delay	Measured to 50% quiescent current		500		ns
Forward isolation in power down			80		dB
Input resistance in power down			$> 1$		$\text{M}\Omega$
Output resistance in power down			16		$\text{k}\Omega$

## 6.6 Package Thermal Data

PACKAGE	PCB	$T_A = 25^\circ\text{C}$ POWER RATING <sup>(1)</sup>
PWP (14-pin) <sup>(2)</sup>	See <a href="#">Layout</a> .	3 W

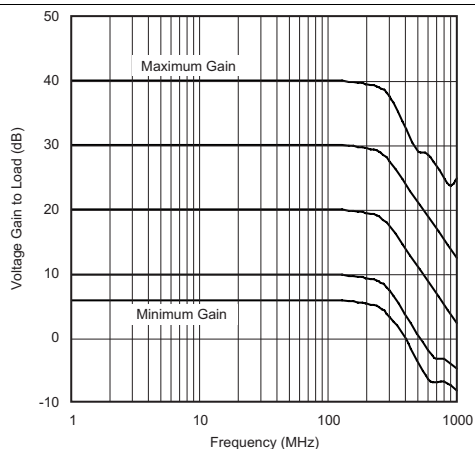
- (1) This data was taken using 2 oz trace and copper pad that is soldered directly to a 3 in x 3 in PCB.
- (2) The THS7530-Q1 incorporates a PowerPAD on the underside of the chip. The PowerPAD acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs [SLMA002](#) and [SLMA004](#) for more information about using the PowerPAD thermally enhanced package.

## 6.7 Typical Characteristics

Measured using the AC test circuit shown in Figure 16 (unless otherwise noted).

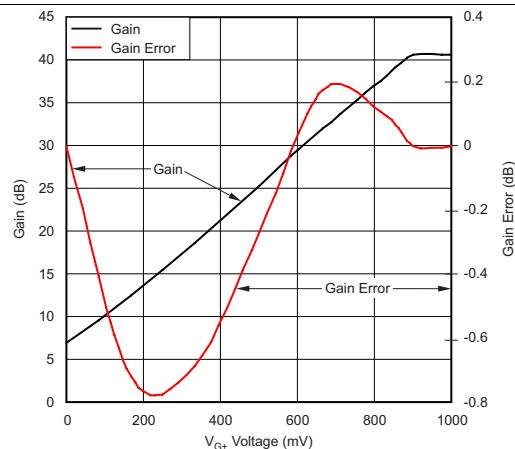
**Table 1. Table Of Graphs**

		FIGURE
Voltage Gain to Load	vs Frequency (Input at 45 dBm)	Figure 1
Gain and Gain Error	vs $V_{G+}$	Figure 2
Noise Figure	vs Frequency	Figure 3
Output Intercept Point	vs Frequency	Figure 4
1-dB Compression Point	vs Frequency	Figure 5
Total Input Voltage Noise	vs Frequency	Figure 6
Intermodulation Distortion	vs Frequency	Figure 7
Harmonic Distortion	vs Frequency	Figure 8
S-Parameters	vs Frequency	Figure 24
Differential Input Impedance of Main Amplifier	vs Frequency	Figure 25
Differential Output Impedance of Main Amplifier	vs Frequency	Figure 9
$V_{G+}$ Input Impedance	vs Frequency	Figure 10
$V_{OCM}$ Input Impedance	vs Frequency	Figure 11
Common-Mode Rejection Ratio	vs Frequency	Figure 12
Step Response: 2 $V_{PP}$	vs Time	Figure 13
Step Response: Rising Edge	vs Time	Figure 14
Step Response: Falling Edge	vs Time	Figure 15

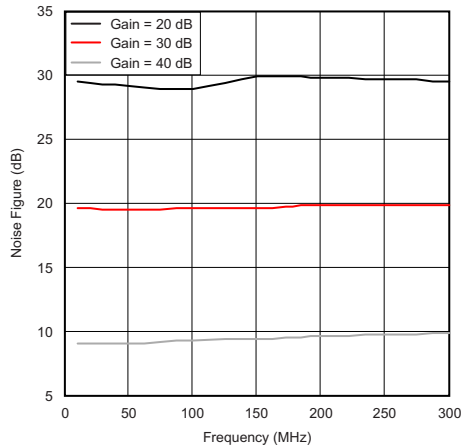


Gain is taken at load. Add 6 dB to refer to amplifier output  
 $P_{IN} = -45$  dBm

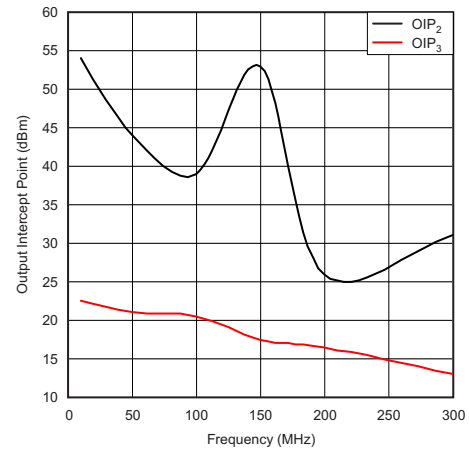
**Figure 1. Voltage Gain to Load vs Frequency**



**Figure 2. Gain and Gain Error vs  $V_{G+}$**

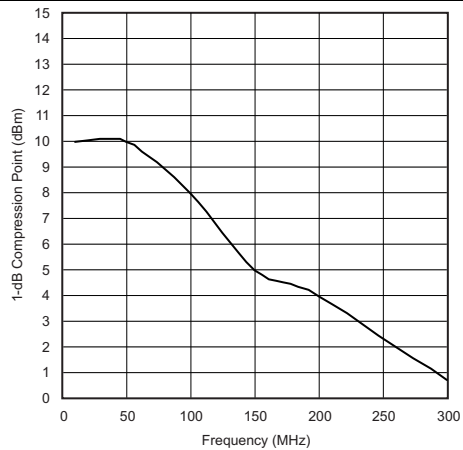


Terminated input

**Figure 3. Noise Figure vs Frequency**


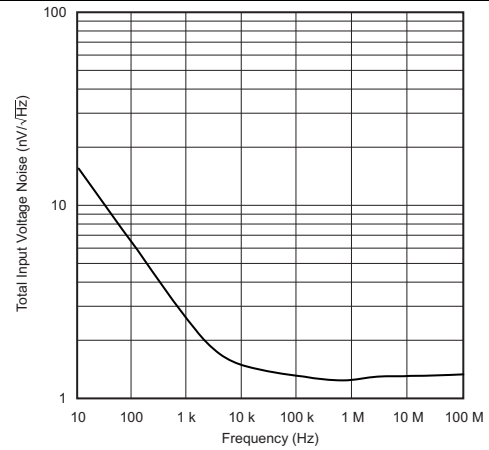
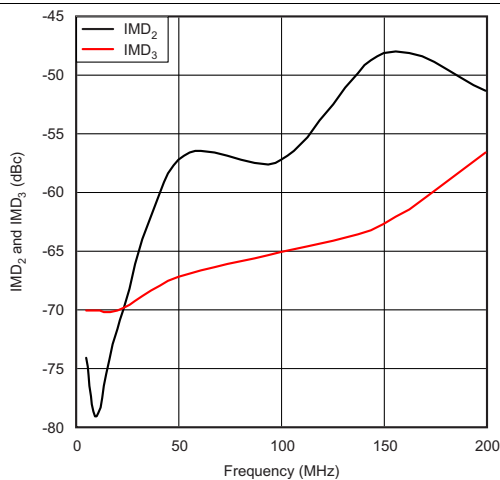
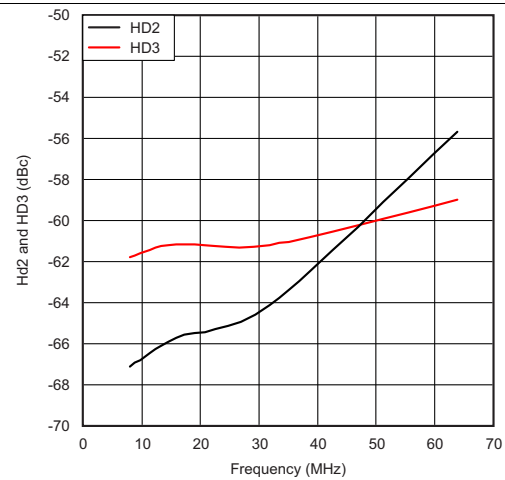
Taken at load.

Add 3 dB to refer to amplifier output.

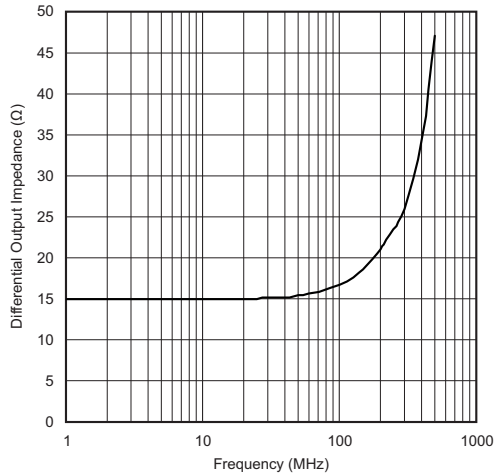
**Figure 4. Output Intercept Point vs Frequency**


Taken at load.

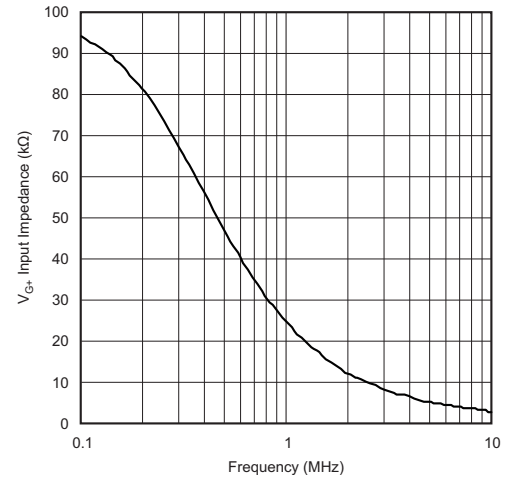
Add 3 dB to refer to amplifier output.

**Figure 5. 1-dB Compression Point vs Frequency**

**Figure 6. Total Input Voltage Noise vs Frequency**

 $V_{G+} = 1\text{ V}$      $V_O = 1\text{ V}_{PP}$  (composite)     $R_L = 400\ \Omega$ 
**Figure 7. Intermodulation Distortion vs Frequency**

 $V_{G+} = 1\text{ V}$      $V_O = 1\text{ V}_{PP}$      $R_L = 400\ \Omega$ 
**Figure 8. Harmonic Distortion vs Frequency**

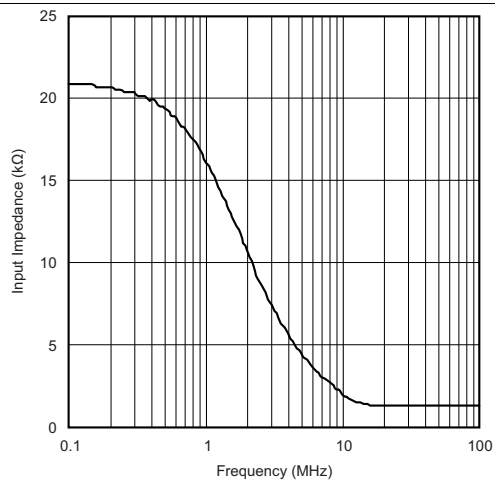




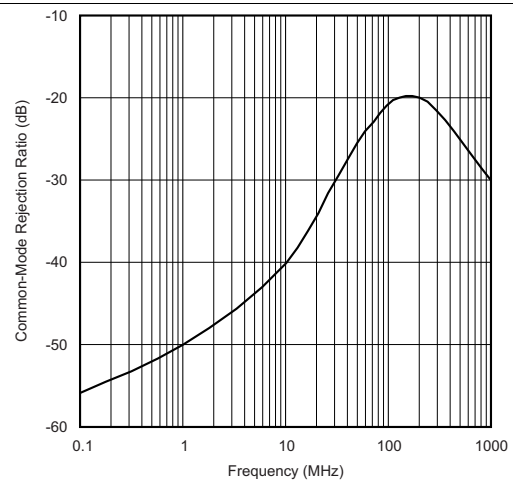
**Figure 9. Differential Output Impedance of Main Amplifier vs Frequency**



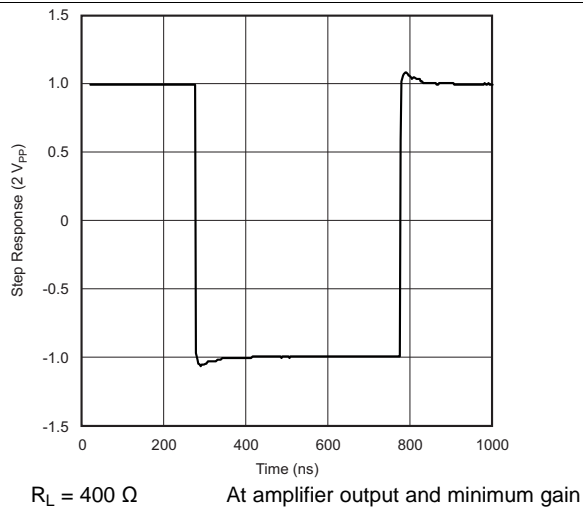
**Figure 10.  $V_{G+}$  Input Impedance vs Frequency**



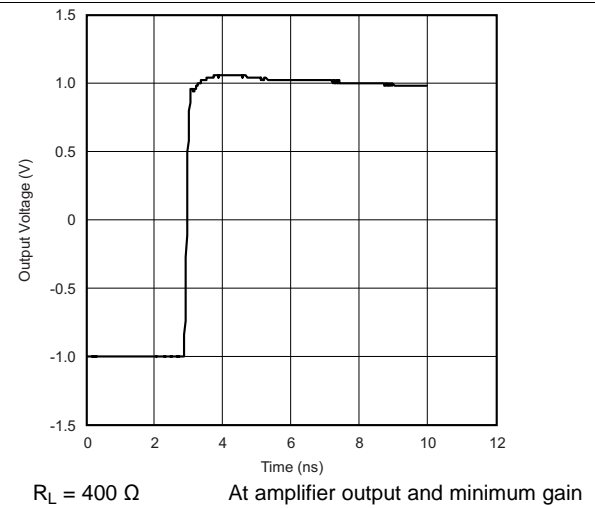
**Figure 11.  $V_{OCM}$  Input Impedance vs Frequency**



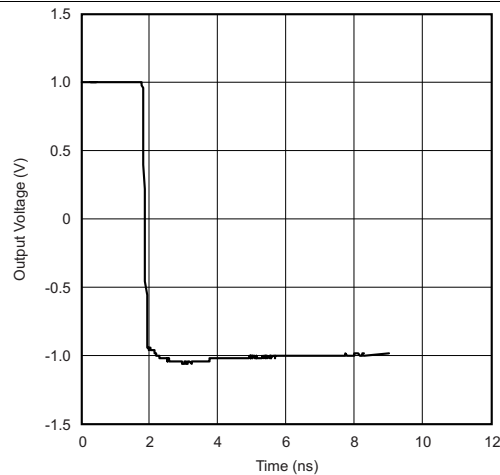
**Figure 12. Common-Mode Rejection Ratio vs Frequency**



**Figure 13. Step Response**



**Figure 14. Step Response: Rising Edge**



$R_L = 400 \Omega$

At amplifier output and minimum gain

Figure 15. Step Response: Falling Edge

## 7 Parameter Measurement Information

### 7.1 Test Circuits

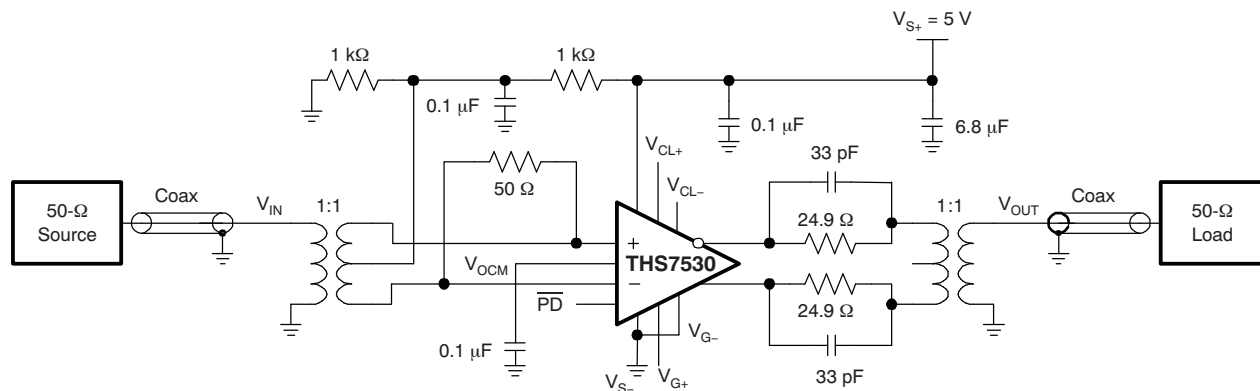


Figure 16. AC Test Circuit

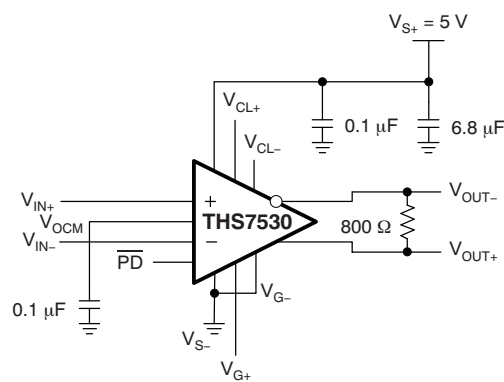


Figure 17. DC Test Circuit

## 8 Detailed Description

### 8.1 Overview

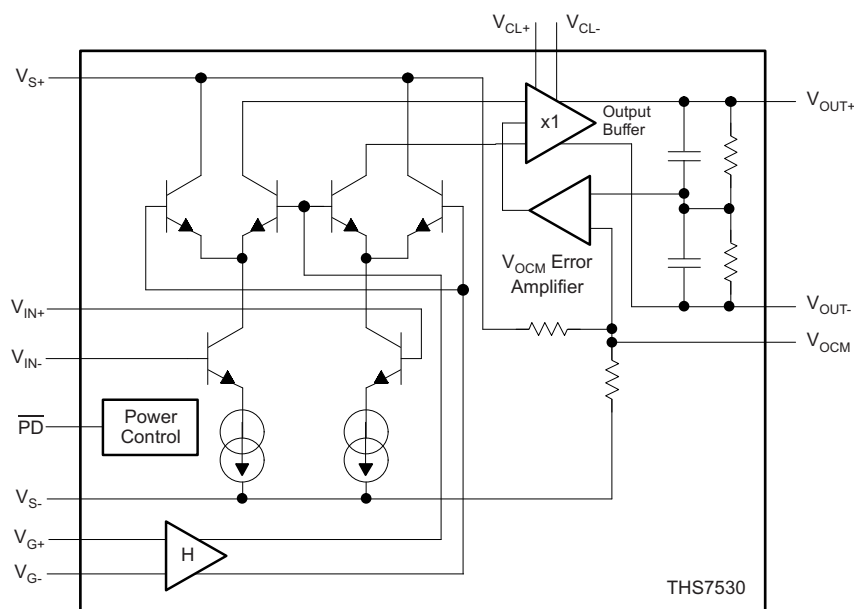
The THS7530-Q1 device is a fully-differential amplifier with 300-MHz bandwidth and with continually-variable gain from 11.6 dB to 46.5 dB. This amplifier together with an automatic gain control (AGC) circuit will precisely established a desired amplitude at its output.

The input architecture is a modified Gilbert cell. The output from the Gilbert cell is converted to a voltage and buffered to the output as a fully-differential signal. A summing node between the outputs is used to compare the output common-mode voltage to the  $V_{OCM}$  input. The  $V_{OCM}$  error amplifier then servos the output common-mode voltage to maintain it equal to the  $V_{OCM}$  input. Left unterminated,  $V_{OCM}$  is set to midsupply by internal resistors.

The gain control input is conditioned to give linear-in-dB gain control (block H). The gain control input is a differential signal from 0 V to 0.9 V which varies the gain from 11.6 dB to 46.5 dB.

$V_{CL+}$  and  $V_{CL-}$  provide inputs that limit the output voltage swing of the amplifier.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The main features of the THS7530-Q1 device are continually-variable gain control, common-mode voltage control, output voltage clamps, and power-down mode.

#### 8.3.1 Continually-Variable Gain Control

The amplifier gain in dB is a linear function of the gain control voltage, which has a range of 0 V to 0.9 V. The slope of the gain control input is 38.8 dB/V with a gain range of 11.6 dB to 46.5 dB, which is 3.8 to 211.3 V/V, respectively. The bandwidth of the gain control is 15 MHz, typically.

The gain control is a differential input to reduce noise due to ground bounce, coupling, and so forth. The negative gain-control input  $V_{G-}$  can be below the negative supply by as much as 600 mV.

#### 8.3.2 Common-Mode Voltage Control

The common-mode voltage control sets the common-mode voltage of the differential output. The gain of the control voltage is 1 V/V with a range of 1.75 V to 3.25 V above the negative supply. If unconnected, the common-mode voltage control is at mid-supply, typically 2.5 V above the negative supply. The bandwidth of the common-mode voltage control is an impressive 32 MHz.

## Feature Description (continued)

### 8.3.3 Output Voltage Clamps

Separate inputs,  $V_{CL-}$  and  $V_{CL+}$ , establish the minimum and maximum output voltages, respectively. The typical error of the output voltage compared to the clamp voltage is only 25 mV. This feature can be used to avoid saturating the inputs of a receiving device, thereby precluding long recovery times in the signal path.

### 8.3.4 Power-Down Mode

To minimize power consumption when idle, the THS7530-Q1 device has an active-low power-down control that reduces the quiescent current from 40 mA to 350  $\mu$ A. The turnon delay is only 820 ns.

When in power-down mode, the THS7530-Q1 device has a 80-dB forward isolation to allow other devices to drive the same signal path with minimal interference from the idle THS7530-Q1 device.

## 8.4 Device Functional Modes

The THS7530-Q1 device has two functional modes: full-power mode and power-down mode. The power-down mode reduces the quiescent current of the device to 350  $\mu$ A from a typical value of 40 mA.

With a turnon time of only 820 ns and a turnoff time of 500 ns, the power-down mode can be used to greatly reduce the average power consumption of the device without sacrificing system performance.

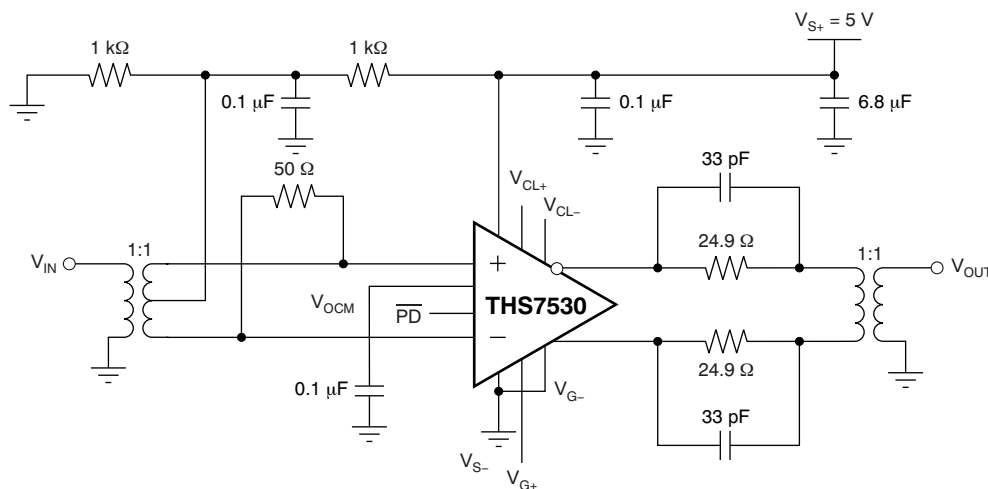
## 9 Application and Implementation

### NOTE

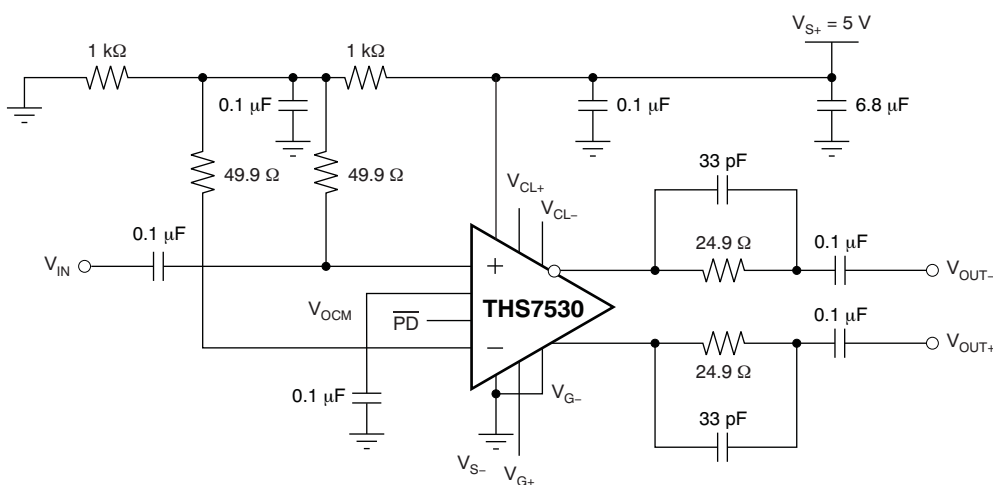
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The THS7530-Q1 device is designed to work in a wide variety of applications requiring continuously variable gain and a fully-differential signal path. The common-mode voltage control and the output voltage clamps enable the THS7530-Q1 device to drive a diverse array of receiving circuits.

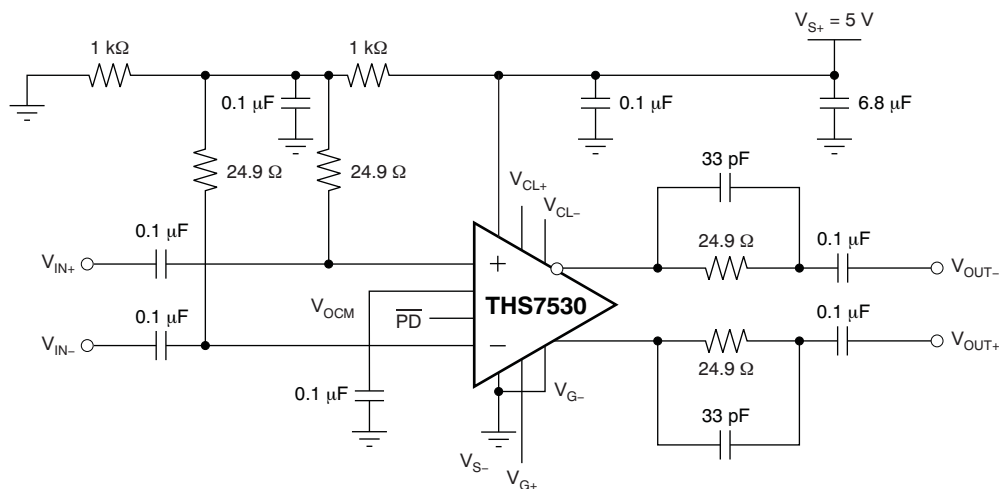


**Figure 18. EVM Schematic: Designed for Use With Typical 50-Ω RF Test Equipment**

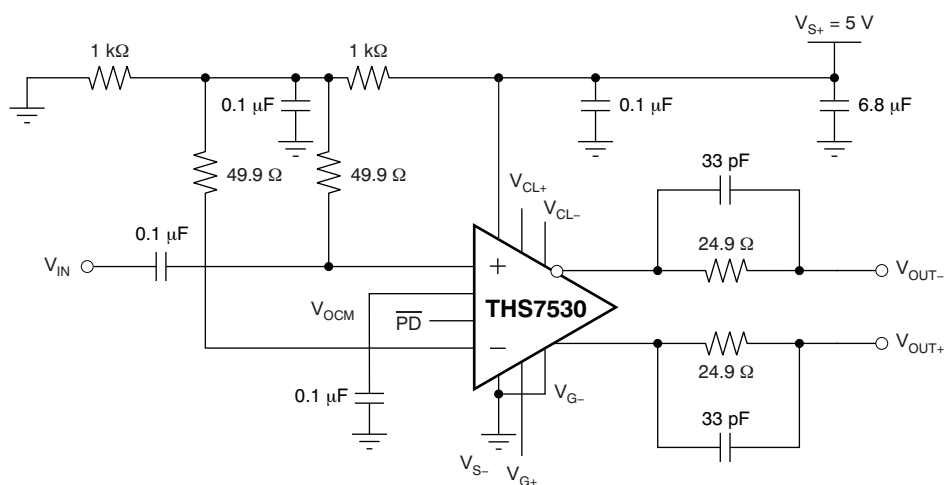


**Figure 19. AC-Coupled Single-Ended Input With AC-Coupled Differential Output**

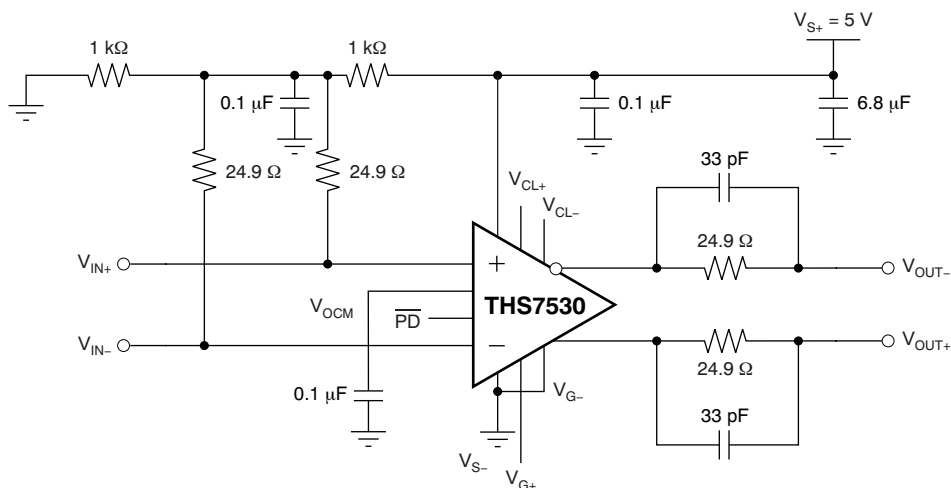
## Application Information (continued)



**Figure 20. AC-Coupled Differential Input With AC-Coupled Differential Output**

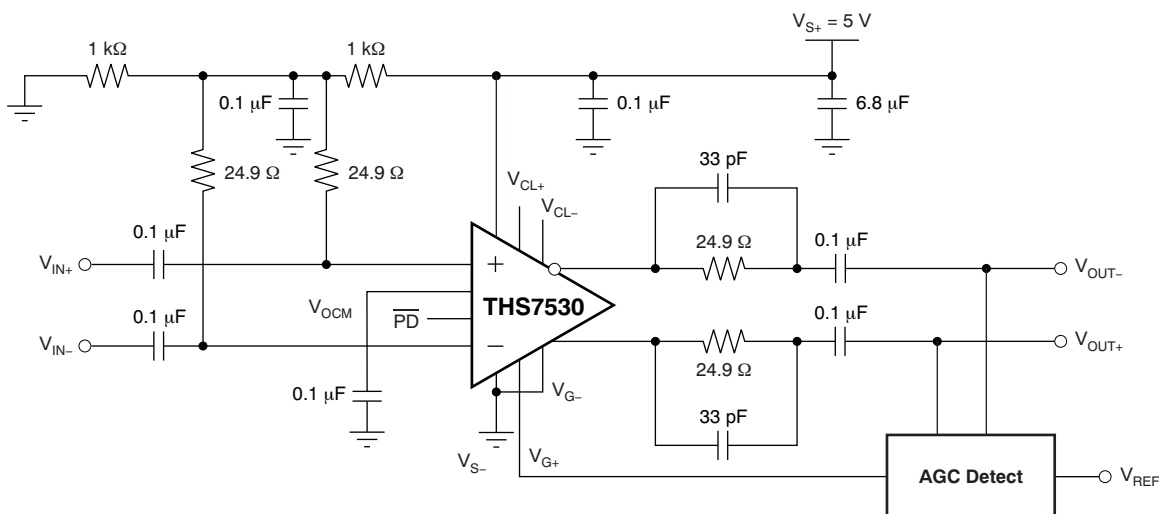


**Figure 21. DC-Coupled Single-Ended Input With DC-Coupled Differential Output**



**Figure 22. DC-Coupled Differential Input With DC-Coupled Differential Output**

## 9.2 Typical Application



### Figure 23. Typical Application Circuit

### 9.2.1 Design Requirements

A typical application circuit is shown in [Figure 23](#). Two noteworthy aspects of this circuit are the customer's automatic gain control (AGC) circuit and the THS7530-Q1 input bias circuit.

The proper design of the AGC circuit is essential for the TSH7530-Q1 device to operate properly in the customer's application. The method of detecting the amplitude of the differential output of the TSH7530-Q1 device and creating the gain-control voltage,  $V_{G+}$ , from the detected amplitude and the reference amplitude,  $V_{ref}$ , are application-specific and beyond the scope of this document. The bandwidth of the amplitude of the TSH7530-Q1 amplitude control is 15 MHz, which allows for rapid corrections of amplitude errors but which also allows noise from DC to 15 MHz to create an amplitude error. The trade-off between rapid amplitude correction and amplitude modulation due to noise is an important design consideration.

The input bias currents of the differential inputs of the TSH7530-Q1 device are typically 20  $\mu\text{A}$ . When the differential inputs are AC-coupled, the bias currents must be supplied as shown in [Figure 23](#). In this circuit, the DC bias voltage is mid-supply and the AC differential input impedance is 50  $\Omega$ . The 0.1- $\mu\text{F}$  capacitor between the two 24.9- $\Omega$  resistors creates an AC ground for the driving circuit.

### 9.2.2 Detailed Design Procedure

The THS7530-Q1 device is designed for nominal 5-V power supply from  $V_{S+}$  to  $V_{S-}$ .

The amplifier has fully differential inputs,  $V_{IN+}$  and  $V_{IN-}$ , and fully differential outputs,  $V_{OUT+}$  and  $V_{OUT-}$ . The inputs are high impedance and outputs are low impedance. External resistors are recommended for impedance matching and termination purposes.

The inputs and outputs can be DC-coupled, but for best performance, the input and output common-mode voltage should be maintained at the midpoint between the two supply pins. The output common-mode voltage is controlled by the voltage applied to  $V_{OCM}$ . Left unterminated,  $V_{OCM}$  is set to midsupply by internal resistors. A 0.1- $\mu$ F bypass capacitor should be placed between  $V_{OCM}$  and ground to reduce common-mode noise. The input common-mode voltage defaults to midrail when left unconnected. For voltages other than midrail,  $V_{OCM}$  must be biased by external means.  $V_{IN+}$  and  $V_{IN-}$  both require a nominal 30- $\mu$ A bias current for proper operation. Therefore, ensure equal input impedance at each input to avoid generating an offset voltage that varies with gain.

Voltage applied from  $V_{G-}$  to  $V_{G+}$  controls the gain of the part with 38.8-dB/V gain slope. The input can be differential or single ended.  $V_{G-}$  must be maintained within  $-0.6$  V and  $0.8$  V of  $V_{S-}$  for proper operation. The negative gain input should typically be tied directly to the negative power supply.

## Typical Application (continued)

$V_{CL+}$  and  $V_{CL-}$  are inputs that limit the output voltage swing of the amplifier. The voltages applied set an absolute limit on the voltages at the output. Input voltages at  $V_{CL+}$  and  $V_{CL-}$  clamp the output, ensuring that neither output exceeds those values.

The power-down input is a TTL compatible input, referenced to the negative supply voltage. A logic low puts the THS7530-Q1 device in power-saving mode. In power-down mode the part consumes less than 1-mA current, the output goes high impedance, and a high amount of isolation is maintained between the input and output.

Power-supply bypass capacitors are required for proper operation. A 6.8- $\mu$ F tantalum bulk capacitor is recommended if the amplifier is located far from the power supply and may be shared among other devices. A ceramic 0.1- $\mu$ F capacitor is recommended within 0.1-in of the device power pin. The ceramic capacitors should be located on the same layer as the amplifier to eliminate the use of vias between the capacitors and the power pin.

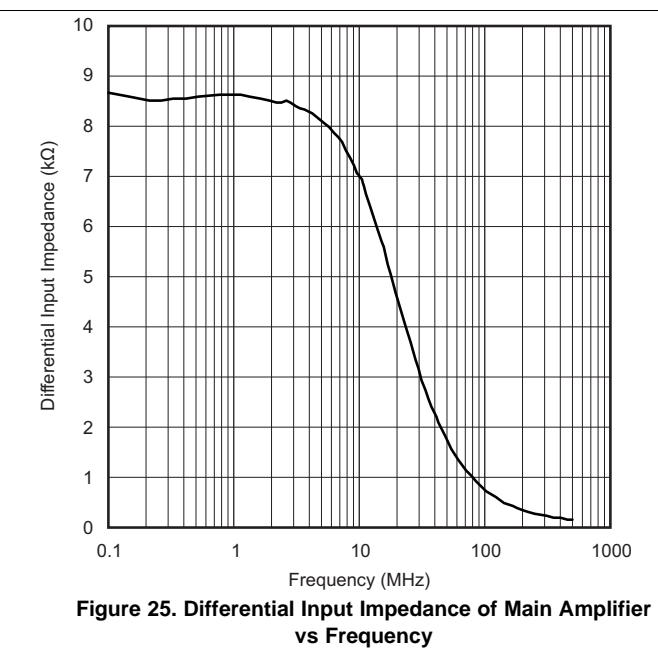
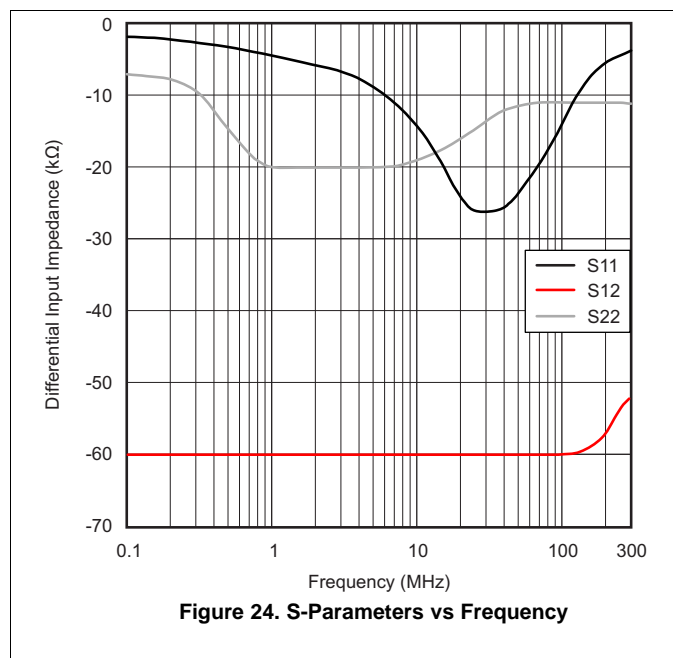
**Table 2. THS7530EVM Bill of Materials**

ITEM NO.	DESCRIPTION	SIZE	REFERENCE DESIGNATOR	QTY	PART NUMBER
1	Bead, ferrite, 3 A, 80 $\Omega$	1206	FB1	1	(Steward) HI1206N800R-00
2	Capacitor, tantalum, 6.8 mF, 35 V, 10%	D	C2	1	(AVX) TAJD685K035R
3	Capacitor, ceramic, 0.1 mF, X7R, 16V	508	C1	1	(AVX) 0508YC104KAT2A
5	Capacitor, ceramic, 0.1 mF, X7R, 50 V	805	C3, C7, C12, C13, C14, C15, C16, C17	8	(AVX) 08055C104KAT2A
6	Diode, Schottky, 20 V, 0.5 A	SOD-123	D1	1	(Diodes Inc.) B0520LW-7
7	Resistor, 10 $\Omega$ , 1/8 W, 1%	805	R24, R25, R26	3	(PHYCOMP) 9C08052A10R0FKHFT
8	Resistor, 24.9 $\Omega$ , 1/8 W, 1%	805	R9, R15	2	(PHYCOMP) 9C08052A24R9FKHFT
9	Resistor, 1 k $\Omega$ , 1.8W, 1%	805	R7, R12	2	(PHYCOMP) 9C08052A1001FKHFT
10	Resistor, 3.92 k $\Omega$ , 1/8 W, 1%	805	R1	1	(PHYCOMP) 9C08052A3921FKHFT
11	Resistor, 0 $\Omega$ , 1/4 W	1206	C4, C5	2	(PHYCOMP) 9C12063A0R00JLHFT
12	Resistor, 49.9 $\Omega$ , 1/4 W, 1%	1206	R4	1	(PHYCOMP) 9C12063A49R9FKRFT
13	Pot., ceramic, 1/4 inch square, 1 k $\Omega$		R2	1	(Bourns) 3362P-1-102
14	Pot., ceramic, 1/4 inch square, 10 k $\Omega$		R21, R22, R23	3	(Bourns) 3362P-1-103
15	IC, TLV2371	SOT-23	U2, U3, U4	3	(TI) TLV2371IDBVT
16	Transformer, 1:1	CD542	T1, T2	2	(Mini-Circuits) ADT1-1WT
17	Connector, edge, SMA PCB Jack		J3, J4	2	(Johnson) 142-0701-801
18	Jack, banana receptacle, 0.25-in diameter hole		J1, J2	2	(HH Smith) 101
19	Header, 0.1-in Ctrs, 0.025-in square pins	2 POS.	JP1	1	(Sullins) PZC36SAAN
20	Shunts		JP1	1	(Sullins) SSC02SYAN
21	Test point, black		TP2, TP3, TP4	3	(Keystone) 5001
22	Test points, red		TP1, TP8, TP9, TP10	4	(Keystone) 5000
23	Standoff, 4-40 Hex, 0.625-in Length			4	(Keystone) 1804
24	Screw, Phillips, 4-40, .250-in			4	SHR-0440-016-SN
25	IC, THS7530-Q1		U1	1	(TI) THS7530QPWPRQ1
26	Board, printed circuit			1	(TI) EDGE # 6441987



### 9.2.3 Application Curves

Figure 24 and Figure 25 highlight the input characteristics of the THS7530-Q1 device that should be used to design the circuit driving the THS7530-Q1 device.



## 10 Power Supply Recommendations

The THS7530-Q1 device is principally intended to operate with a nominal single-supply voltage of 5 V. Supply voltage tolerances of  $\pm 10\%$  are supported. The absolute maximum supply is 5.5 V.

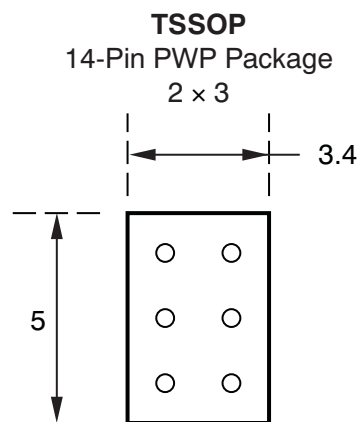
Supply decoupling is required, as described in [Application and Implementation](#).

Split (or bipolar) supplies can be used with the THS7530-Q1 device, as long as the total value across the device remains less than 5.5 V (absolute maximum).

## 11 Layout

### 11.1 Layout Guidelines

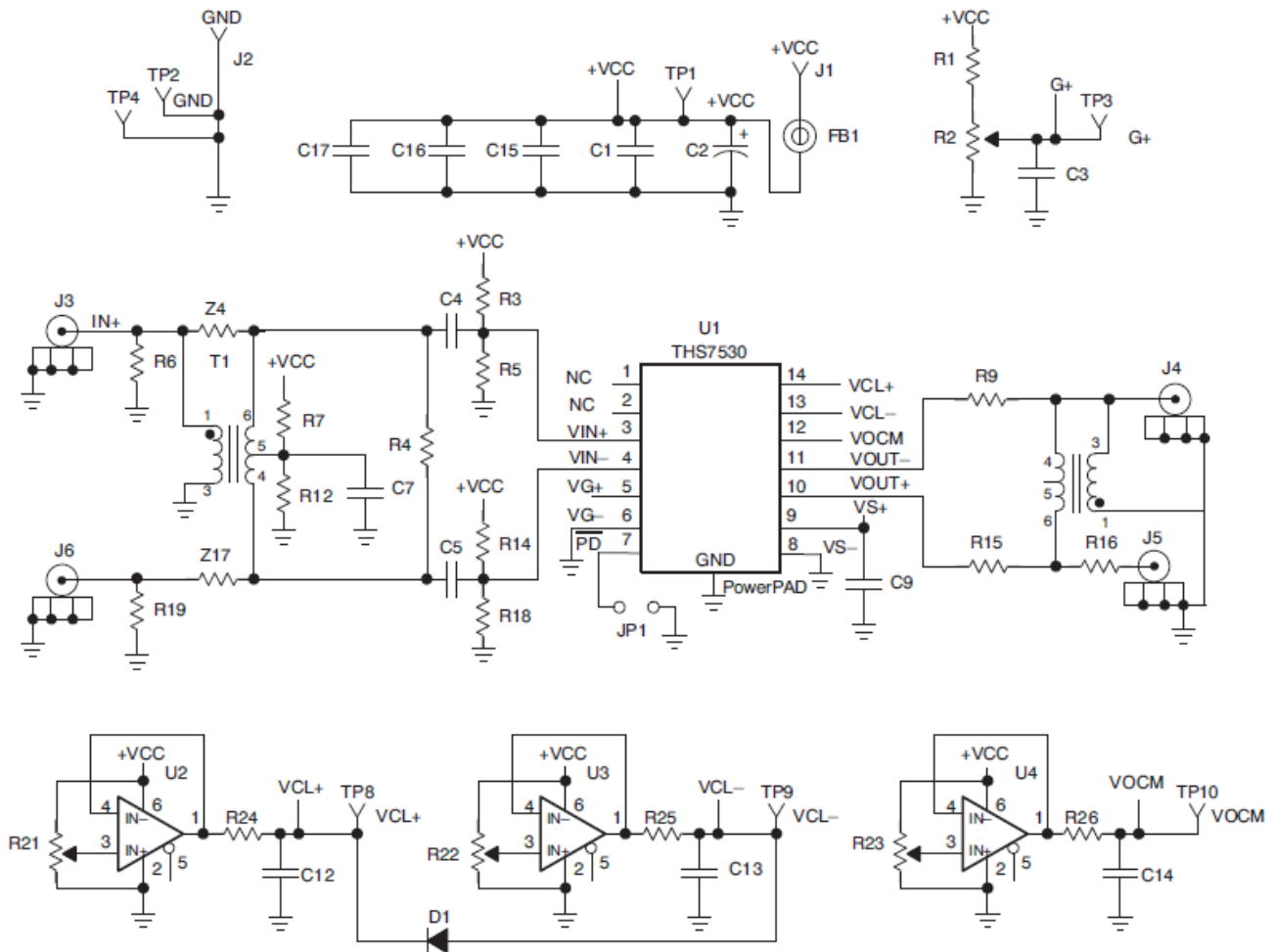
The THS7530-Q1 device is available in a thermally-enhanced PowerPAD™ package. Figure 26 shows the recommended number of vias and thermal land size recommended for best performance. Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solelectron Texas indicate that a via drill diameter of 0.33 mm (13 mils, or .013 in) or smaller works well when 1-ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1 mm minimum. This prevents the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.



**Figure 26. Recommended Thermal Land Size and Thermal Via Patterns (Dimensions in mm)**

See TI's Technical Brief titled, *PowerPAD™ Thermally Enhanced Package* ([SLMA002](#)) for a detailed discussion of the PowerPAD™ package, its dimensions, and recommended use.

## Layout Guidelines (continued)



**Figure 27. EVM Schematic**

## 11.2 Layout Examples

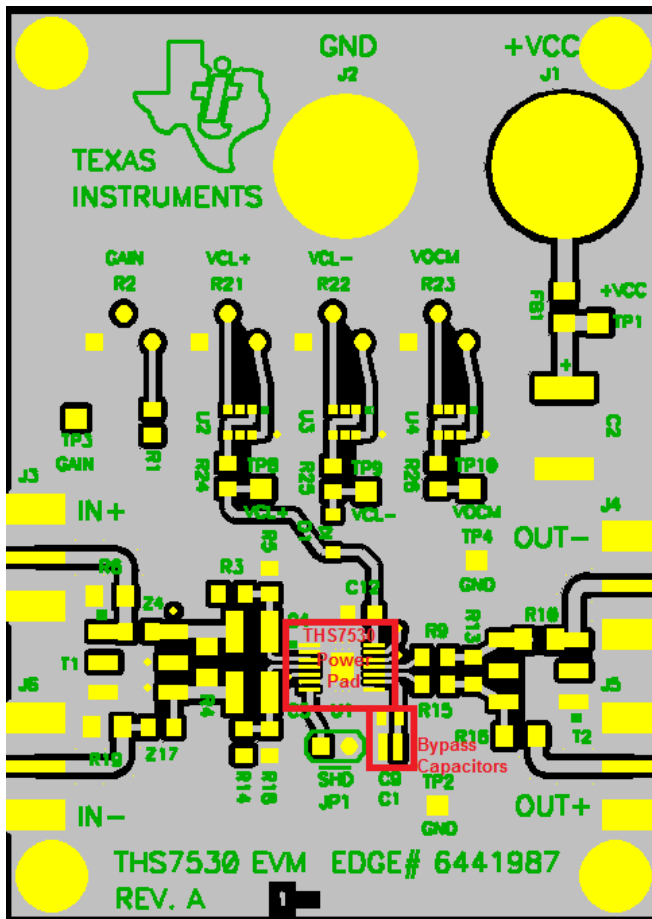


Figure 28. Layout Diagram (Top)

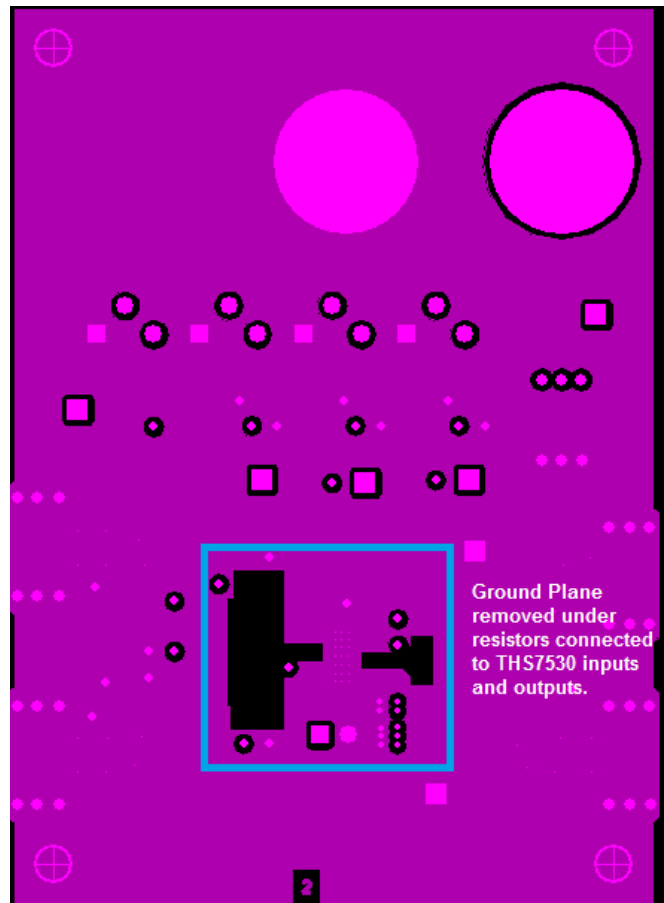


Figure 29. Layout Diagram (Ground)

## Layout Examples (continued)

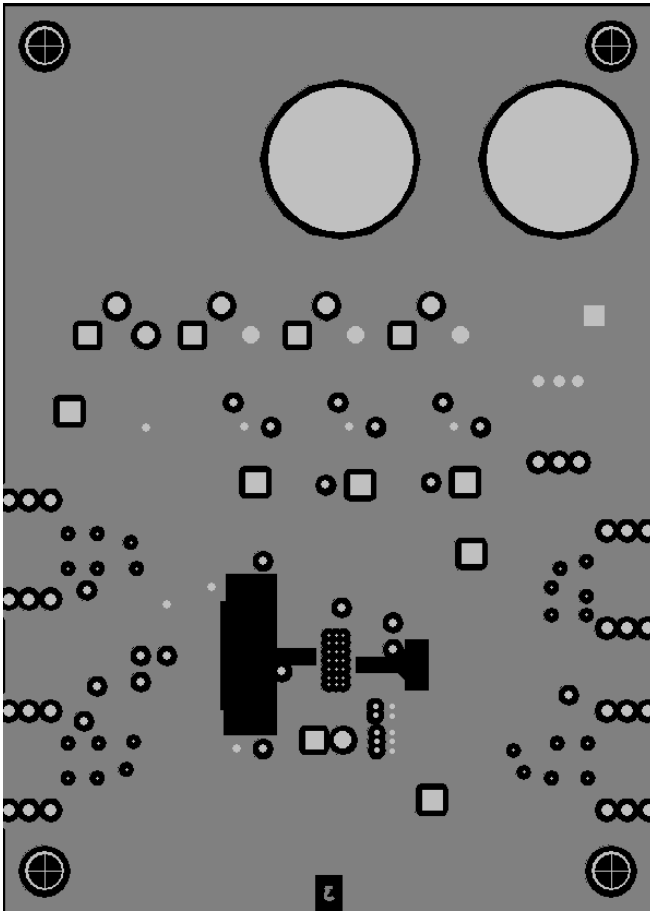


Figure 30. Layout Diagram (Power)

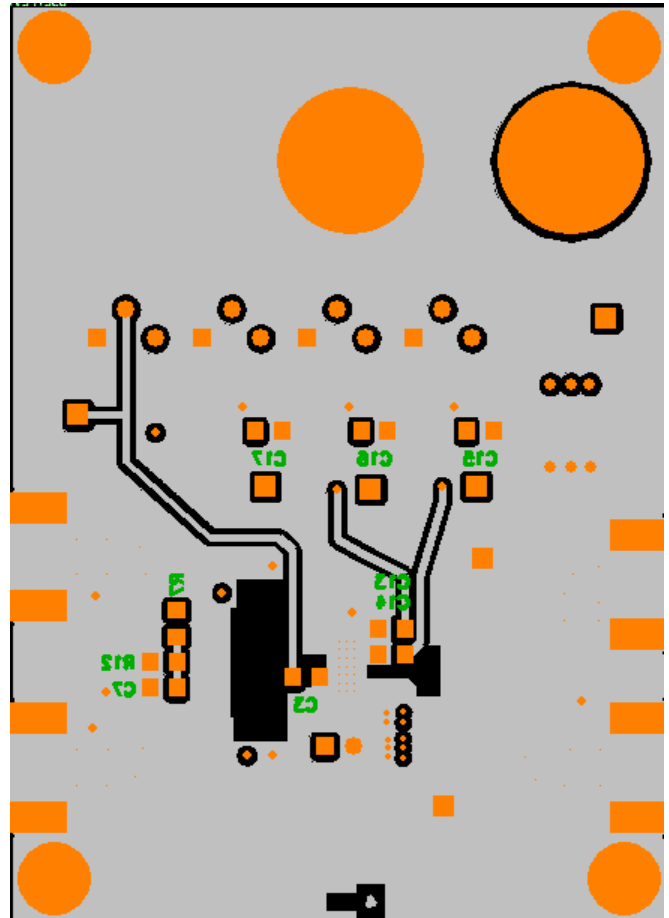


Figure 31. Layout Diagram (Bottom)

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 Third-Party Products Disclaimer

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#### 12.1.2 开发支持

有关 THS7530 PSPICE 模型, 请参见 [SLOJ139](#)。

有关 THS7530 TINA-TI SPICE 模型, 请参见 [SLAM020](#)。

有关 THS7530 TINA-TI 参考设计, 请参见 [SLAC091](#)。

### 12.2 文档支持

#### 12.2.1 相关文档

相关文档如下:

- 《THS7530 EVM 用户指南》, [SLOU161](#)
- 《高速运算放大器噪声分析》, [SBOA066](#)
- 《TI 模拟信号链指南》, [SLYB174](#)
- 《PowerPAD™ 耐热增强型封装》, [SLMA002](#)
- 《PowerPAD™ 速成》, [SLMA004](#)

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本, 请查阅左侧的导航栏。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7530QPWPRQ1	ACTIVE	HTSSOP	PWP	14	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	T7530Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## GENERIC PACKAGE VIEW

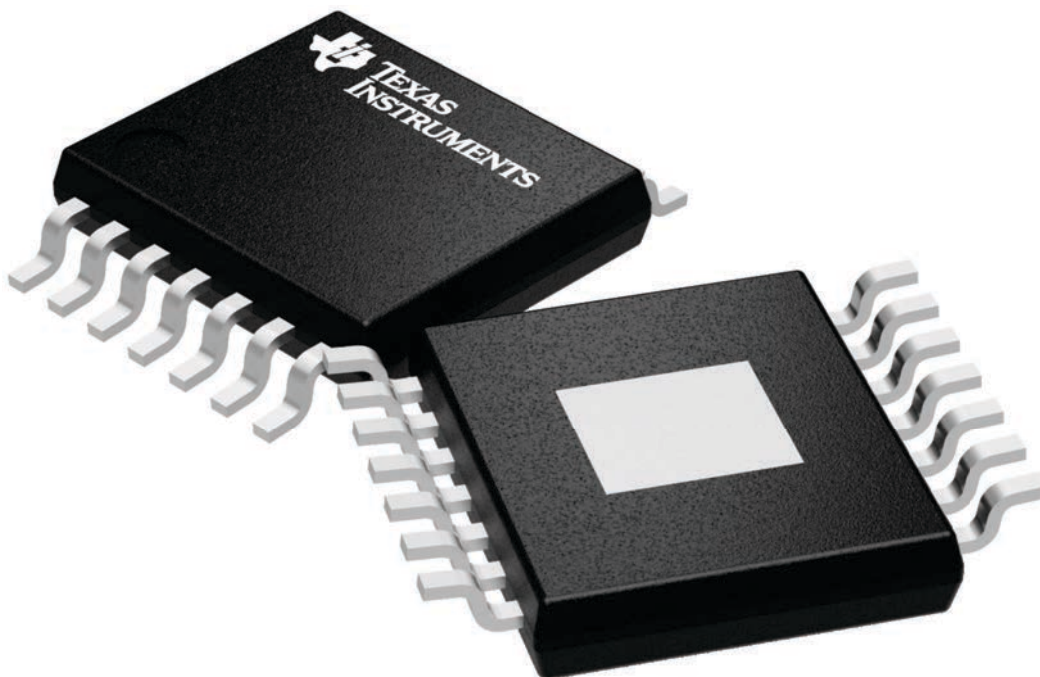
**PWP 14**

**PowerPAD TSSOP - 1.2 mm max height**

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

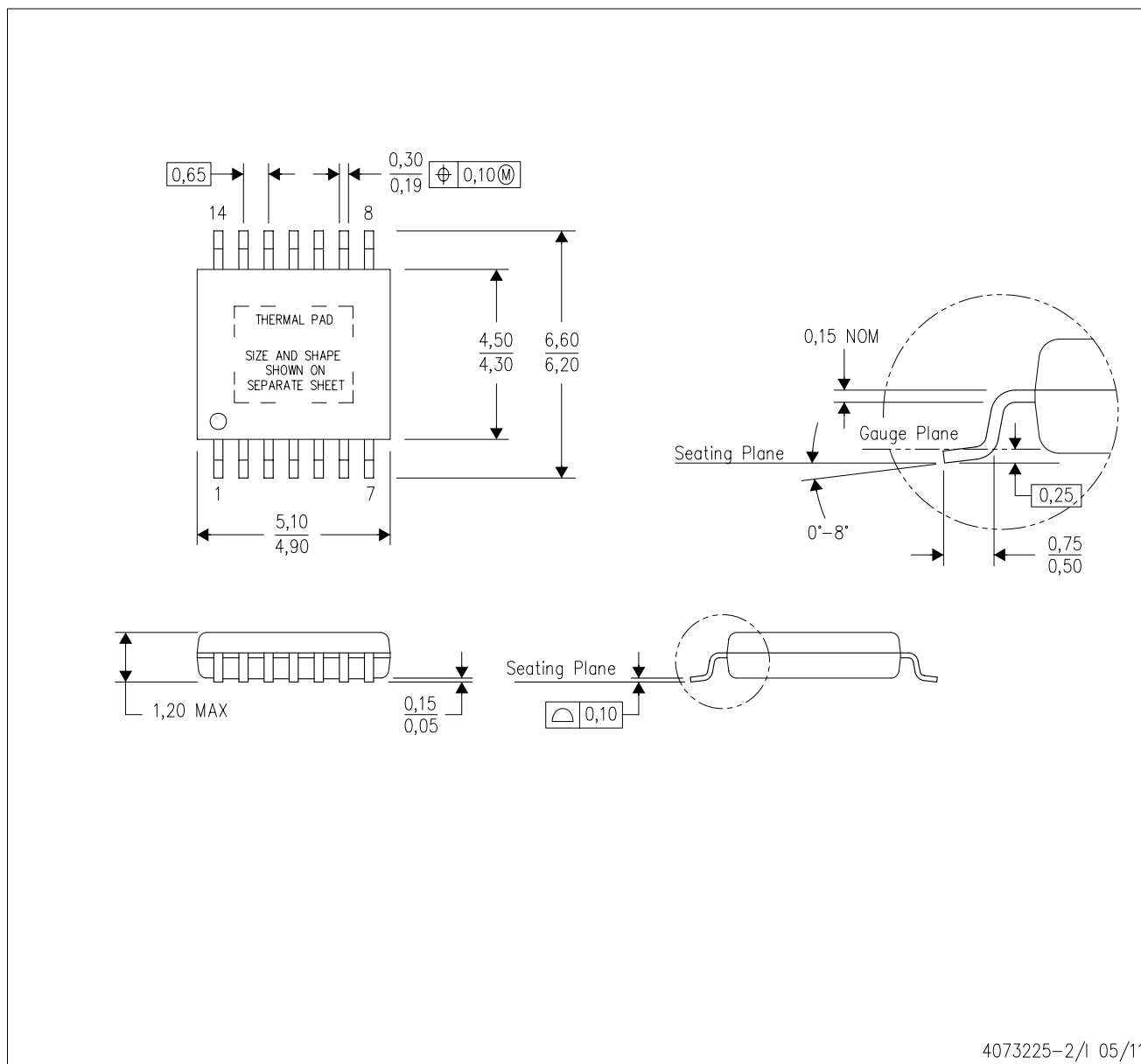


4224995/A



PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

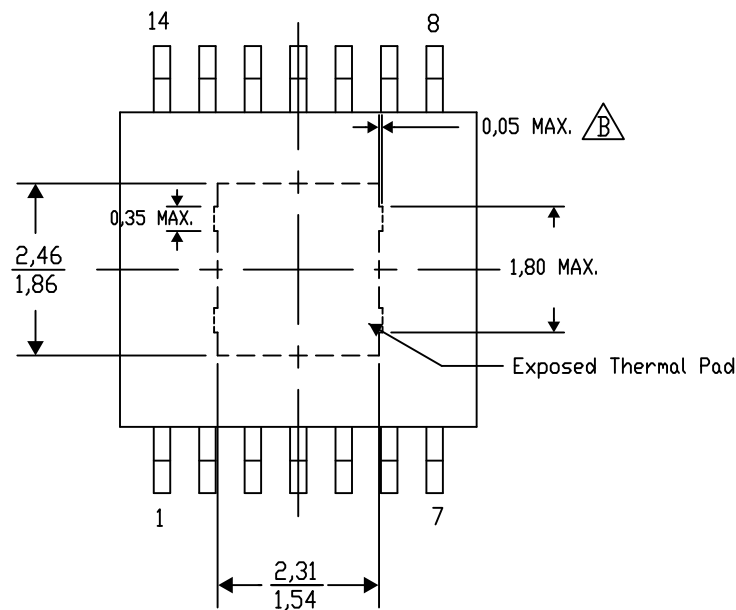
## PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).


For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



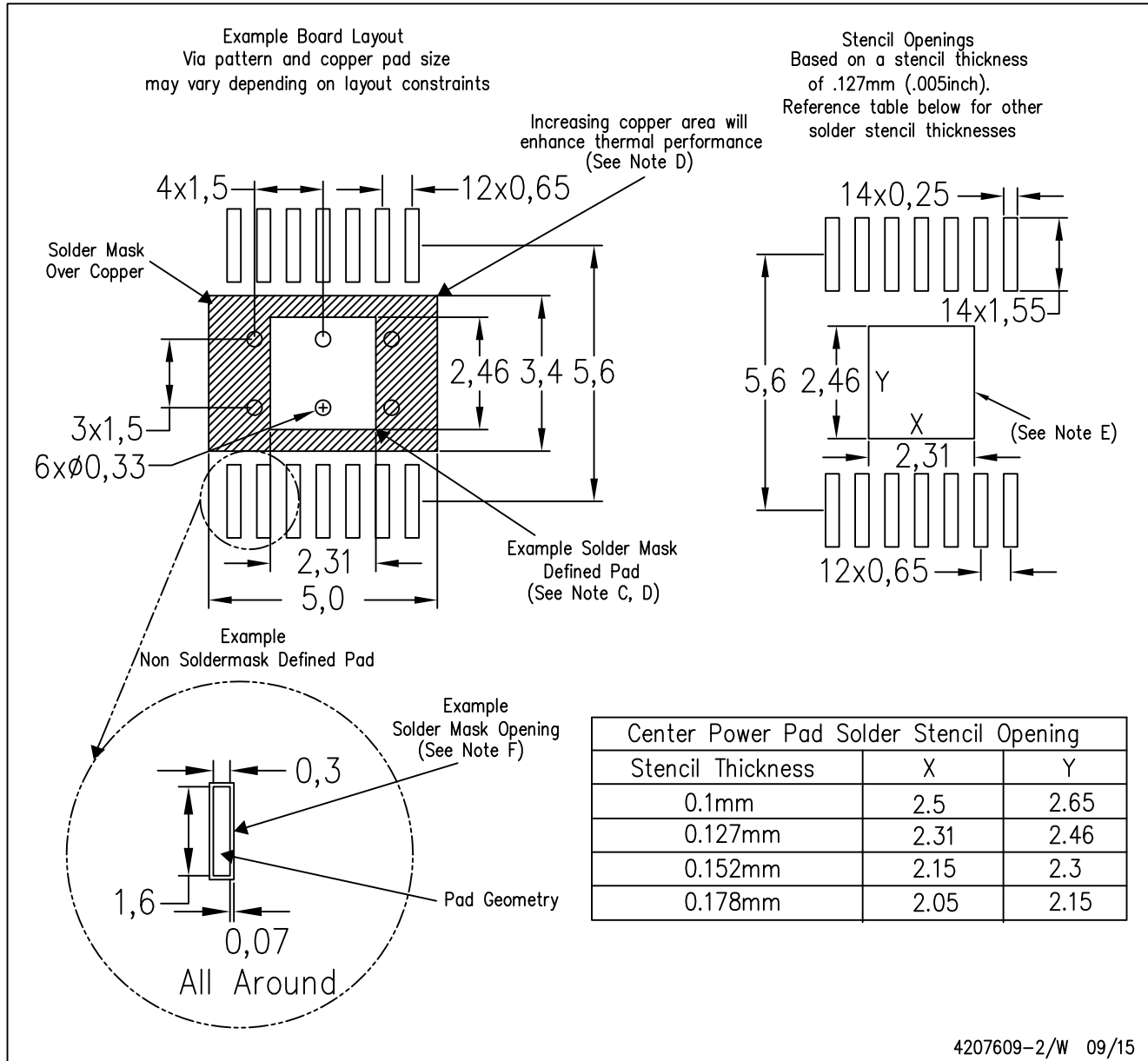
4206332-44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

## PWP (R-PDSO-G14)

## PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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