STRUCTURE	Silicon Monolithic Integrated Circuit		
TYPE	B A 5 9 1 2 B F P		
PRODUCT SERIES	BTL DRIVER for CD-ROM		
PACKAGE OUTLINES	Figure 1 (Plastic Mold)	POWER DISSIPATION	Figure 2
BLOCK DIAGRAM	Figure 3	APPLICATION	Figure 4
TEST CIRCUIT	Figure 5	SWITCH TABLE	Table 1

FUNCTIONS

① 2ch BTL Driver.
② Available in a HSOP25 package
③ Wide dynamic range.
④ Built-in thermal shutdown circuit.
⑤ Includes two general purpose operational amplifiers.
⑥ Built-in mute (ch1, 2) circuit and stand by mode(by muting both channel).
⑦ Voltage supply (Pre Vcc, CH1 Pow Vcc, CH2 Pow Vcc) are separated.

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{cc}	13.5	V
Power dissipation	P_d	1.45 *1	W
Operating temperature	T_{opr}	-40 to +85	℃
Storage temperature	T_{stg}	-55 to +150	℃

*1 Reduce power by 11.6 mW for each degree above 25℃, on a glass epoxy PCB (70×70×1.6mm thick).

GUARANTEED OPERATING RANGES

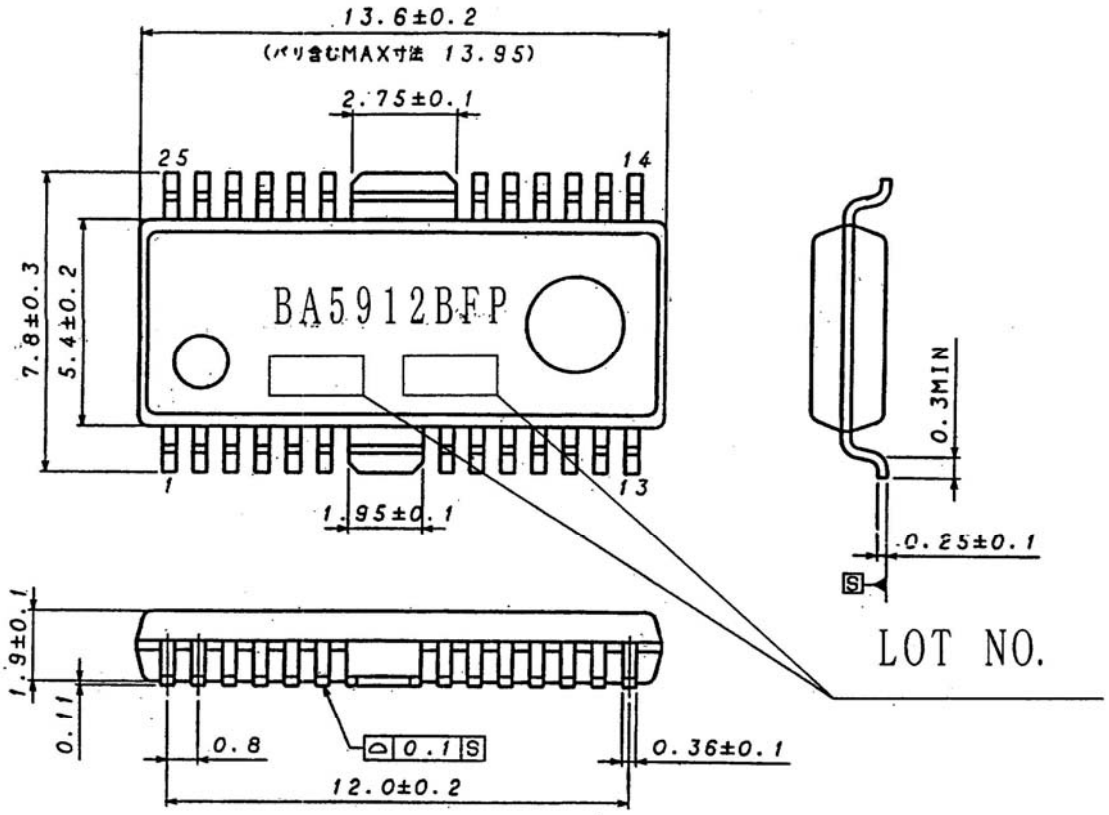
Parameter	Symbol	Limits	Unit
Vcc for pre-block	Pre Vcc	4.5 ～ 13.2	V
Vcc for power-block	Pow Vcc1, 2	4.5～Pre Vcc	V

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_a=25℃ , Pre, Pow Vcc=5V, BIAS=2.5V , R_L=8Ω)

Parameter	Symbol	Test cir -cuit	Conditions	Limits			Unit
				Min.	Typ.	Max.	
Quiescent current	Icc	Fig 5	No load , REF1, 2≧2.0V	—	9.0	14.0	mA
Stand-by quiescent current	Iscc	Fig 5	No load, ref1, 2≦0.5V	—	0	100	μA
DRIVER							
Output voltage offset	Voo	Fig 5		-50	—	50	mV
Output amplitude 1	Vom1	Fig 5		3.2	3.5	—	V
Output amplitude 2	Vom2	Fig 5		3.7	4.0	—	
Gain (close circuit)	Gvc	Fig 5	BIAS=2.5V, V_{IN}=BIAS±0.5V	10.0	11.5	13.0	dB
Mute-on voltage	Vmon	Fig 5		—	—	0.5	V
Mute-off voltage	Vmoff	Fig 5		2.0	—	—	V
Vref-change voltage 1	VREF1	Fig 5		—	—	0.5	V
Vref-change voltage 2	VREF2	Fig 5		2.0	—	—	V
Operational amplifier							
Offset voltage	Vofop	Fig 5		-5	0	5	mV
Input bias current	Vbop	Fig 5		—	—	300	nA
High level output voltage	Vohop	Fig 5		4.0	4.36	—	V
Low level output voltage	Volop	Fig 5		—	0.74	1.1	V
Output drive current (sink)	Isink	Fig 5	50Ω, at Vcc	10	50	—	mA
Output drive current (source)	Isource	Fig 5	50Ω, at ground	10	40	—	mA
Slew rate	SRop	Fig 5	100KHz square wave, 2Vpk-pk	—	1	—	V/us

◎This product is not designed for protection against radioactive rays.

PACKAGE OUTLINES (mm)

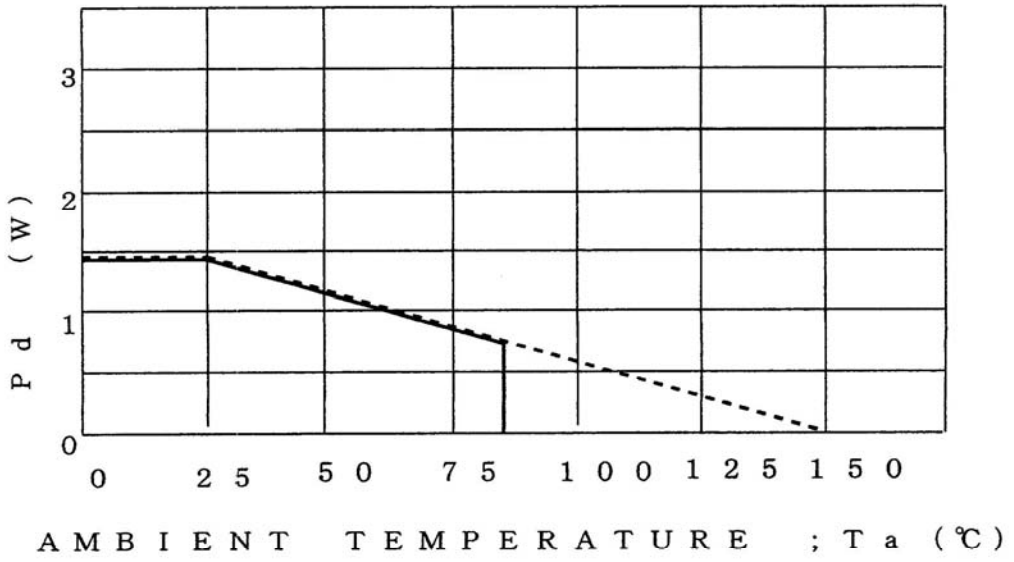


(UNIT : mm)

Figure 1

図番: EX139-5001

POWER DISSIPATION

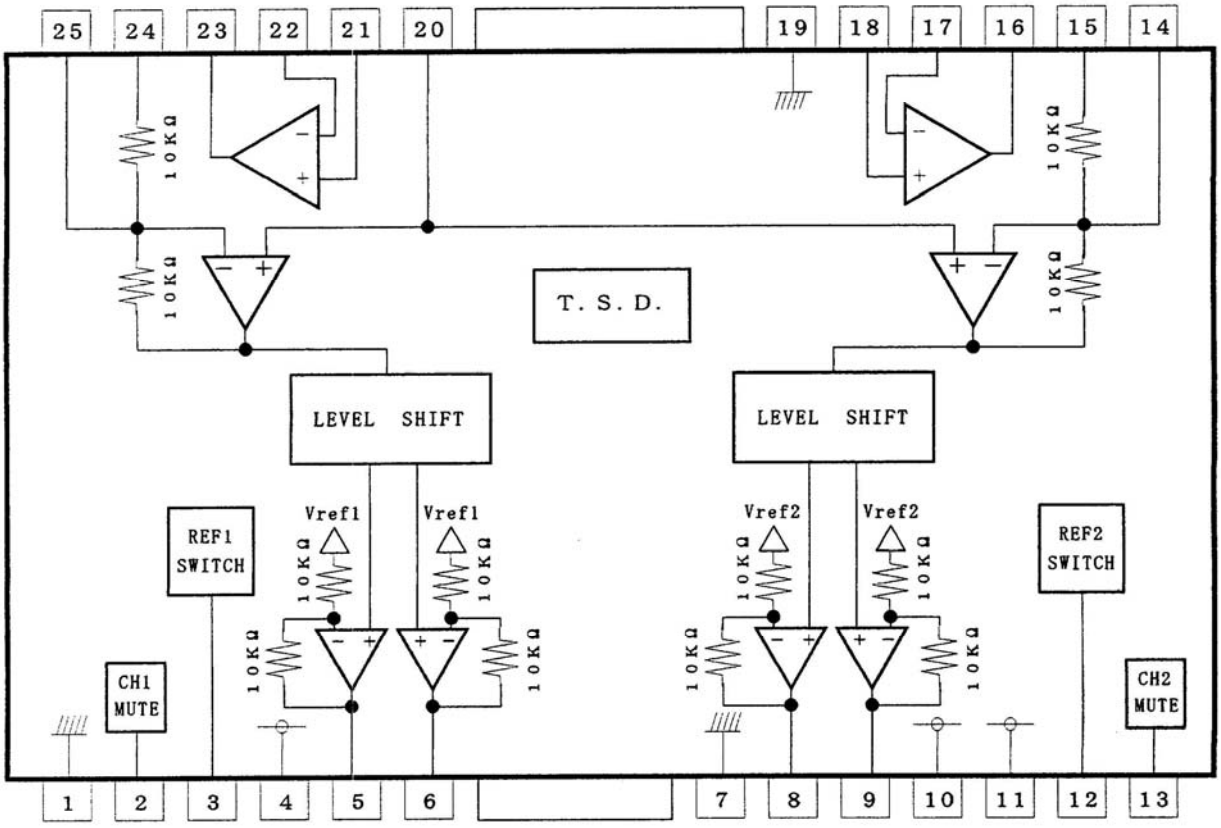


Pd ; power dissipation

Condition : On less than 3% (percentage occupied by copper foil), 70×70mm², T=1.6mm, glass epoxy mounting

Figure2 Power dissipation curve

BLOCK DIAGRAM



T.S.D. ; Thermal shut down circuit

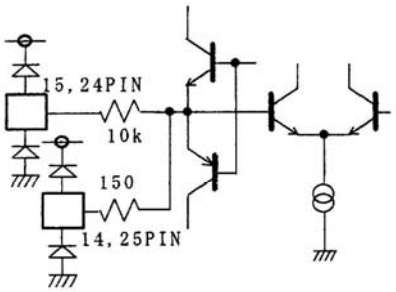
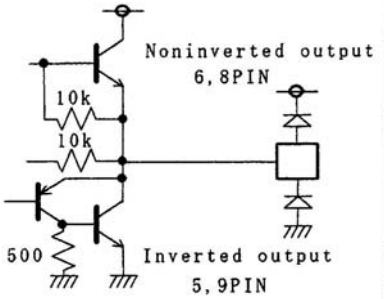
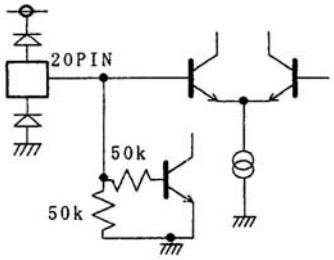
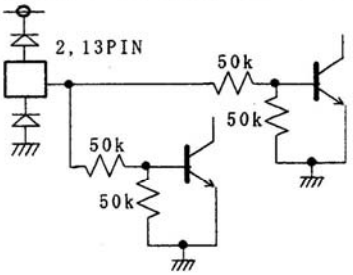
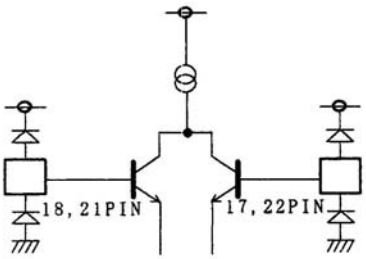
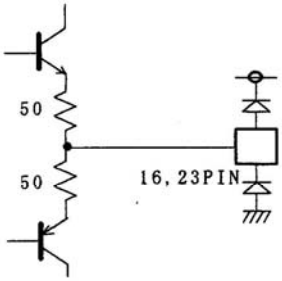
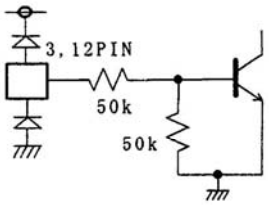
Limits for resistance value:(Ω)

Figure 3

●PIN DESCRIPTION

NO	SYMBOL	Description	NO	SYMBOL	Description
1	GND	Ground	14	IN2'	Driver CH2 input, gain adjustment pin
2	MUTE1	Mute control pin of CH1	15	IN2	Driver CH2 input
3	REF1	Vref control pin of CH1	16	OP1-OUT	Op-amp1 output
4	Pow Vcc1	Pow Vcc for CH1	17	OP1-IN-	Op-amp1 input, negative
5	OUT1-	Driver CH1 inverted output	18	OP1-IN+	Op-amp1 input, positive
6	OUT1+	Driver CH1 noninverted output	19	GND	Ground
7	GND	Ground	20	BIAS	Bias input
8	OUT2+	Driver CH2 noninverted output	21	OP2-IN+	Op-amp2 input, positive
9	OUT2-	Driver CH2 inverted output	22	OP2-IN-	Op-amp2 input, negative
10	Pow Vcc2	Pow Vcc for CH2	23	OP2-OUT	Op-amp2 output
11	Pre Vcc	Pre Vcc	24	IN1	Driver CH11 input
12	REF2	Vref control pin of CH2	25	IN1'	Driver CH1 input, gain adjustment pin
13	MUTE2	Mute control pin of CH2			

●Equivalent circuits of terminals

INPUT OF DRIVER	OUTPUT OF DRIVER
	
BIAS	**MUTE**
	
INPUT OF OP-AMP	**OUT PUT OF OP-AMP**
	
Vref CONTROL	
	

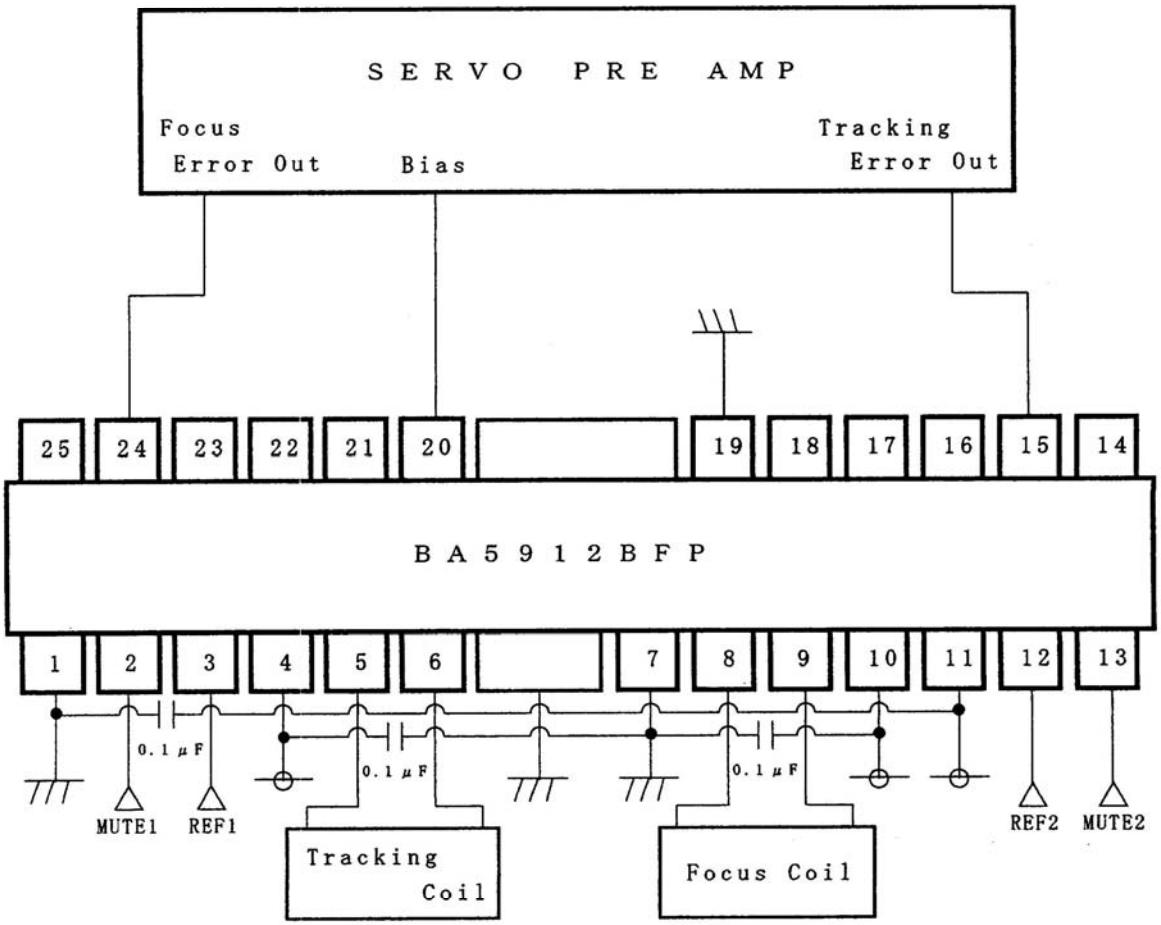
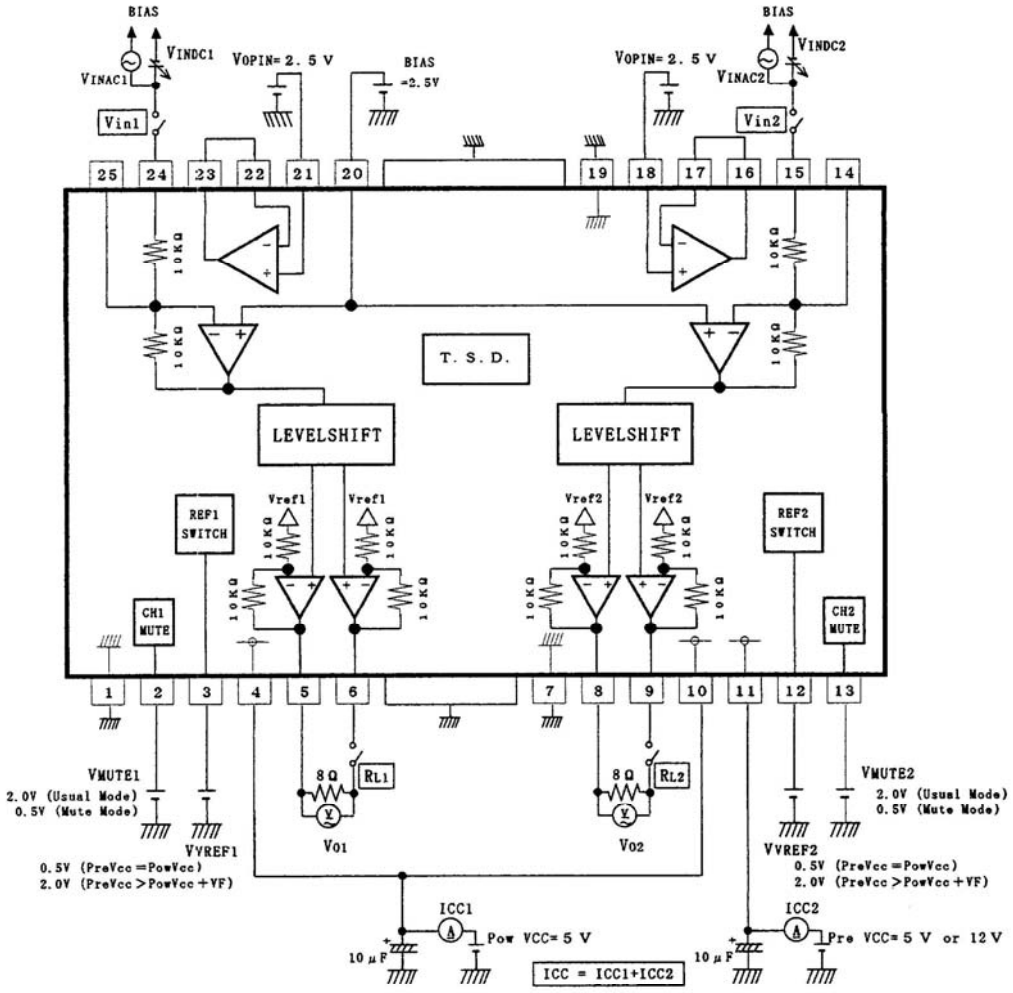

SERVO PRE AMP
Focus
Error Out
Bias
Tracking
Error Out
25
24
23
22
21
20
19
18
17
16
15
14
BA5912BFP
1
2
3
4
5
6
7
8
9
10
11
12
13
0.1μF
0.1μF
0.1μF
MUTE1
REF1
Tracking
Coil
Focus Coil
REF2
MUTE2

Figure 4

TEST CIRCUIT

〈DRIVER BLOCK〉



〈OP-AMP BLOCK〉

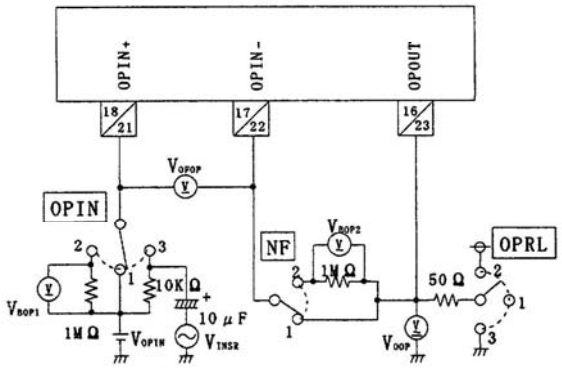


Figure 5

SWITCH TABLE

Table 1

I) DRIVER BLOCK (OPIN→1, NF→1, OPRL→1, VOPIN=2.5V)

Symbol	Switch		Input				Conditions	Measurement point
	Vin1,2	RL1,2	VINDC	VMUTE	VVREF	PREVCC		
Icc	OFF	OFF	----------	2V	2V	5V		ICC
Iscc	↓	↓	----------	0V	↓	↓	VMUTE1,2 0V	ICC
Voo	ON	ON	2.5V	2V	↓	↓		VO1-4
Vom1	↓	↓	0V,5V	↓	↓	↓		VO1-4
Vom2	↓	↓	0V,5V	↓	0V	12V		
Gvc	↓	↓	2.2V,2.8V	↓	2V	5V		VO1-4

II) OP-AMP BLOCK (RL→OFF)

Symbol	Switch			Input		Conditions	Measurement point
	OPIN	NF	OPRL	VOPIN	VINSR		
VOFOP	1	1	1	2.5V	------		VOFOP
IBOP	2	2	1	2.5V	------		VBOP1-2
VOHOP	1	1	1	5V	------		VOOP
VOLOP	1	1	1	0V	------		VOOP
ISINK	1	1	2	2.5V	------		VOOP
ISOURCE	1	1	3	2.5V	------		VOOP
SROP	3	1	1	-----		100KHz Square wave,2Vp-p	VOOP

◎ PRECAUTIONS FOR USE

1. A thermal shutdown circuit is built into the BA5912BFP. When the temperature of the chip reaches 175℃ (typically), the output current is muted. Next time IC chip temperature falls below 150℃ (typ), the driver blocks start.

2. When mute terminal (Pin 2 and 13) voltage is set open or below 0.5V, output current (CH1 and CH2) can be muted independently for each.
In normal use, increase the pin2 and 13 full above 2.0V. When both mute terminal (pin2 and 13) voltages are set open or below 0.5V, standby mode is automatically established.

3. If the bias pin (pin20) drops below 0.7V, The output is muted. Make sure that under normal operating conditions, this pin is at 1.0V or above.

4. The output is muted in the event of a thermal shut down, mute-on, or a bias and Pre-Vcc voltage drop.
Only the drivers are muted.
When muted, the internal bias voltage of the output pin becomes roughly (Pow V_{CC}-V_F)/2 or Pow Vcc/2.

5. Make sure to connect a 0.1μF capacitor to the dc supplied power main input to filter out voltage ripples.

6. Heat dissipation fins are attached to the GND on the inside of the package. Make sure to connect these to the external GND.

7. If Pre Vcc drops below 3.5V (typ), the drivers are turned off. When the voltage exceeds 4.0V (typ), the drivers return to their previous state.

8. When Pre Vcc=Pow Vcc, set Vref switching terminal open or below 0.5V (internal bias voltage=(Pow VCC -VF)/2) , and when Pre Vcc＞Pow Vcc+VF, increase the Vref switching terminnal full above 2.0V (internal bias voltage=Pow VCC/2).

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