2.7 V to 16.5 V Hot Swap Controller with Power-Fail Comparator

Data Sheet

ADM1172

FEATURES

- Controls supply rails from 2.7 V to 16.5 V
- Allows protected board removal and insertion to a live backplane
- External sense resistor provides adjustable analog current limit with circuit breaker
- Peak fault current limited with fast response
- Charge pumped gate drive for external N-FET switch
- Power-fail comparator
- Automatic retry or latch-off during current fault
- Undervoltage lockout
- 8-lead, TSOT package

APPLICATIONS

- Hot swap board insertion: line cards, raid systems
- Industrial high-side switches/circuit breakers
- Electronic circuit breakers

GENERAL DESCRIPTION

The ADM1172 is a hot swap controller that safely enables a printed circuit board to be removed and inserted to a live backplane. This is achieved using an external N-channel power MOSFET with a current control loop that monitors the load current through a sense resistor. An internal charge pump is used to enhance the gate of the N-channel FET. When an overcurrent condition is detected, the gate voltage of the FET is reduced to limit the current flowing through the sense resistor. During an overcurrent condition, the TIMER pin capacitor determines the amount of time the FET remains at a current limiting mode of operation until it is shut down. The ON (ON-$\overline{\text{CLR}}$) pin is the enable input for the device and can be used to monitor the input supply voltage. The ADM1172 operates with a supply voltage ranging from 2.7 V to 16.5 V.

The ADM1172 also features a power-fail comparator. The voltage on the PFI pin is compared with an internal 0.6 V reference, and the output of this comparator is presented on the PFO pin. This device is available in two options: the ADM1172-1 with automatic retry for overcurrent fault and the ADM1172-2 with latch-off for an overcurrent fault. Toggling the ON (ON-$\overline{\text{CLR}}$) pin resets a latched fault. The ADM1172 is packaged in an 8-lead TSOT.

FUNCTIONAL BLOCK DIAGRAM

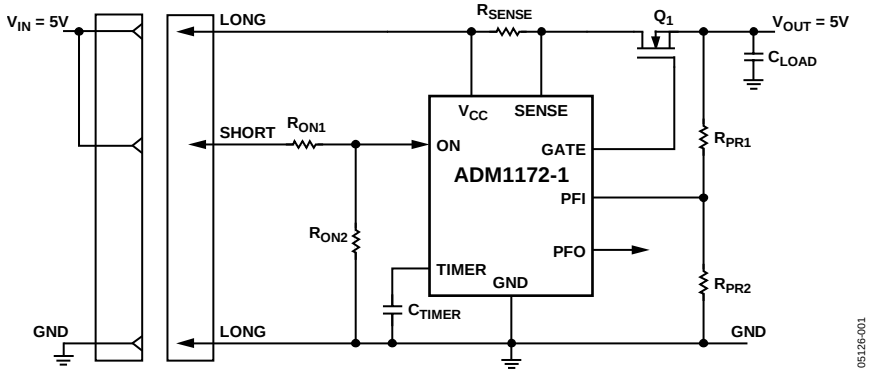


Figure 1.

Document Feedback

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REVISION HISTORY

3/14—Rev. 0 to Rev. A

Changes to Figure 41 ... 14
Changes to Ordering Guide ... 15

7/06—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.7 V to 16.5 V, T_A = −40°C to +85°C, typical values at T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
V_{CC} PIN						
Operating Voltage Range	V_{CC}	2.7		16.5	V	
Supply Current	I_{CC}		0.65	0.8	mA	
Undervoltage Lockout	V_{UVLO}	2.4	2.525	2.65	V	V_{CC} rising
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$		40		mV	
ON (ON-$\overline{CLR}$) PIN						
Input Current	I_{INON}	−1	0	+1	µA	
Threshold	V_{ON}	1.22	1.3	1.38	V	ON rising
Threshold Hysteresis	V_{ONHYST}		50		mV	
SENSE PIN						
Hot Swap Operating Range		2.7		16.5	V	
Input Current	$I_{INSENSE}$	5	10	15	µA	
Circuit Breaker Limit Voltage	V_{CB}	44	50	56	mV	$V_{CB} = (V_{CC} - V_{SENSE})$
GATE PIN						
Drive Voltage	V_{GATE}	4.6	7.5	10	V	$V_{GATE} - V_{CC}$, V_{CC} = 3.0 V
		6.0	8	12	V	$V_{GATE} - V_{CC}$, V_{CC} = 3.3 V
		8.75	10	12	V	$V_{GATE} - V_{CC}$, V_{CC} = 5 V
		7.5	9	12	V	$V_{GATE} - V_{CC}$, V_{CC} = 12 V
		5.56	8	12	V	$V_{GATE} - V_{CC}$, V_{CC} = 15 V
Pull-Up Current		−6.5	−12	−14.5	µA	V_{GATE} = 0 V
Pull-Down Current			4		mA	V_{GATE} = 3 V, V_{CC} = 5 V, ON (ON-$\overline{CLR}$) = low
Pull-Down Current			25		mA	V_{GATE} = 3 V, V_{CC} < UVLO
TIMER PIN						
Pull-Up Current	$I_{TIMERUP}$	−2	−5	−8.5	µA	Initial cycle, V_{TIMER} = 1 V
		−25	−60	−100	µA	During current fault, V_{TIMER} = 1 V
Pull-Down Current	$I_{TIMERDN}$		2	3.5	µA	After Cct breaker tip, V_{TIMER} = 1 V
			100		µA	Normal operation, V_{TIMER} = 1 V
Threshold High	V_{TIMERH}	1.22	1.3	1.38	V	TIMER rising
Threshold Low	V_{TIMERL}	0.15	0.2	0.25	V	TIMER falling
PFI PIN						
Threshold Rising		0.58	0.6	0.62	V	
Threshold Hysteresis			10		mV	
Input Current		−1	0	+1	µA	
PFO PIN						
Pull-Up Current			−5		µA	
Output Low Voltage				0.4	V	I_{LOAD} = 200 µA
t_{OFF}						
Turn-Off Time (TIMER Rise to GATE Fall)			2		µs	V_{TIMER} = 0 V to 2 V step, V_{CC} = V_{ON} = 5 V
Turn-Off Time (ON Fall to GATE Fall)			40		µs	V_{ON} = 5 V to 0 V step, V_{CC} = 5 V
Turn-Off Time (V_{CC} Fall to IC Reset)			40		µs	V_{CC} = 5 V to 2 V step, V_{ON} = 5 V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} Pin	−0.3 V to +20 V
SENSE Pin	−0.3 V to +20 V
V_{CC} − SENSE	±5 V
TIMER Pin	−0.3 V to (V_{CC} + 0.3 V)
ON (ON-$\overline{CLR}$) Pin	−0.3 V to +20 V
PFI Pin	−0.3 V to +20 V
PFO Pin	−0.3 V to +20 V
GATE Pin	−0.3 V to (V_{CC} + 11 V)
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead TSOT	152.9	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

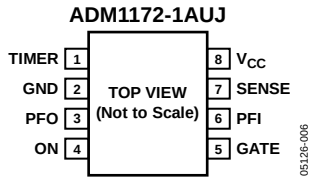


Figure 2. Pin Configuration, 1AUJ Model

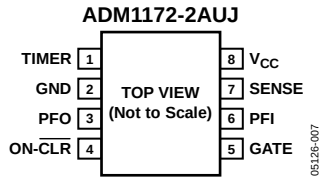


Figure 3. Pin Configuration, 2AUJ Model

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TIMER	Timer Input Pin. The initial and circuit breaker timing cycles are set by this external capacitor. The initial timing delay is 272.9 ms/µF, and 21.7 ms/µF for a circuit breaker delay. When the TIMER pin is pulled beyond the upper threshold, the GATE turns off.
2	GND	Chip Ground Pin.
3	PFO	Power-Fail Comparator Output. Digital output from the power-fail comparator.
4	ON (ON-$\overline{\text{CLR}}$)	Input Pin. The ON (ON-$\overline{\text{CLR}}$) pin is an input to a comparator that has a low-to-high threshold of 1.3 V with 80 mV hysteresis and a glitch filter. The ADM1172 is reset when the ON (ON-$\overline{\text{CLR}}$) pin is low. When the ON (ON-$\overline{\text{CLR}}$) pin is high, the ADM1172 is enabled. A rising edge on this pin has the added function of clearing a fault and restarting the device on the latched off model, the ADM1172-2.
5	GATE	Gate Output Pin. An internal charge pump provides a 12 µA pull-up current to drive the gate of an N-channel MOSFET. In an overcurrent condition, the ADM1172 controls the external FET to maintain a constant load current.
6	PFI	Power-Fail Comparator Input. Comparator threshold = 0.6 V.
7	SENSE	Current Limit Sense Input Pin. The current limit is set via a sense resistor between the V_{CC} and SENSE pins. In an overcurrent condition, the gate of the FET is controlled to maintain the SENSE voltage at 50 mV. When this limit is reached, the TIMER circuit breaker mode is activated. The circuit breaker limit can be disabled by connecting the V_{CC} pin and SENSE pin together.
8	V_{CC}	Positive Supply Input Pin. The ADM1172 operates between 2.7 V to 16.5 V. An undervoltage lockout (UVLO) circuit with a glitch filter resets the ADM1172 when the supply voltage drops below the specified UVLO limit.

TYPICAL PERFORMANCE CHARACTERISTICS

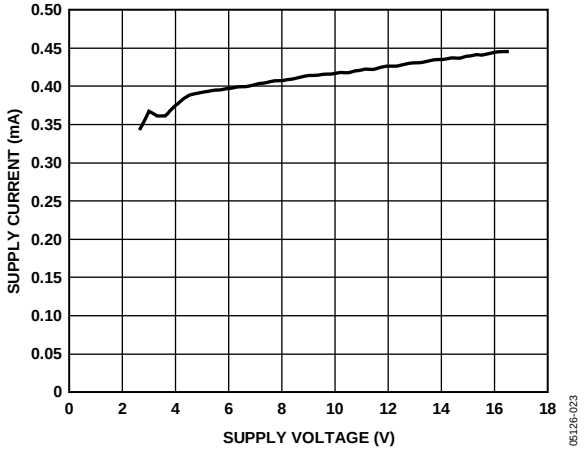


Figure 4. Supply Current vs. Supply Voltage (GATE Off)

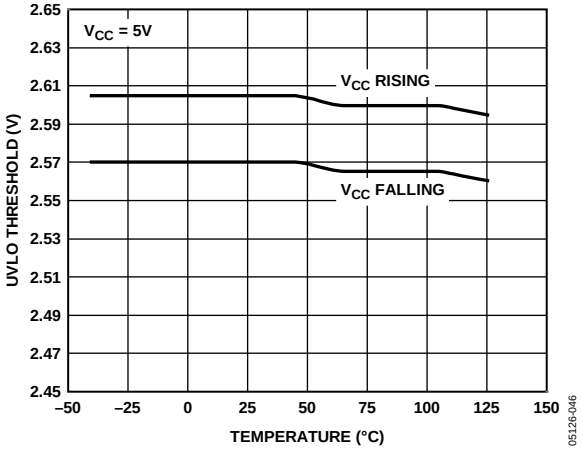


Figure 7. UVLO Threshold vs. Temperature

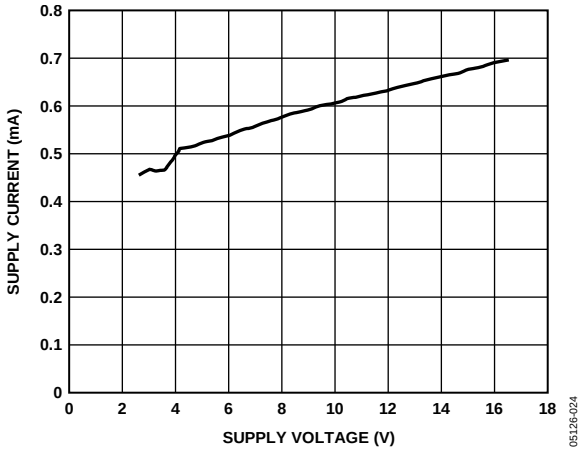


Figure 5. Supply Current vs. Supply Voltage (GATE On)

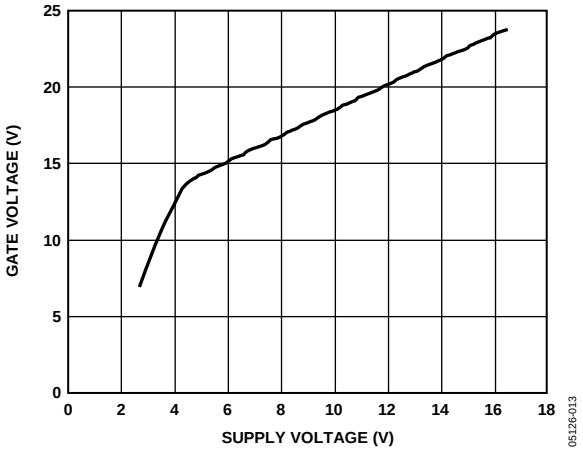


Figure 8. GATE Voltage vs. Supply Voltage

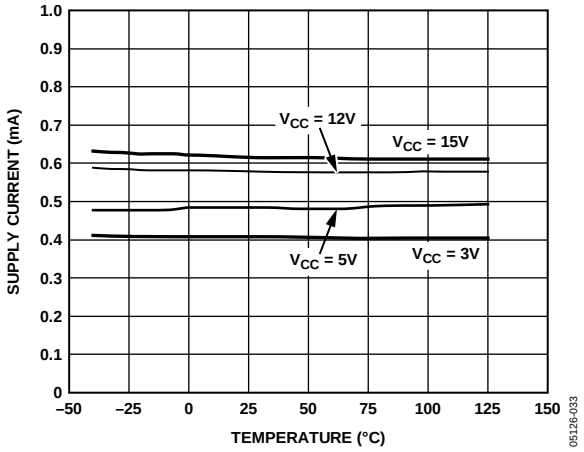


Figure 6. Supply Current vs. Temperature

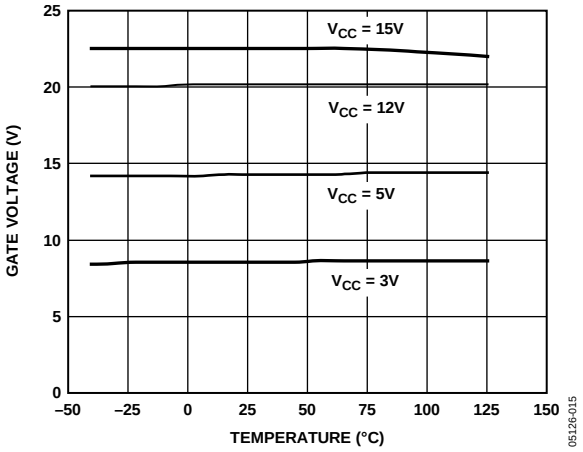


Figure 9. GATE Voltage vs. Temperature

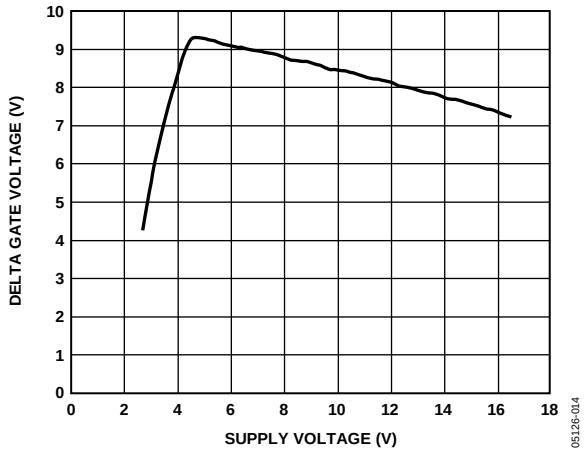


Figure 10. Delta GATE Voltage vs. Supply Voltage

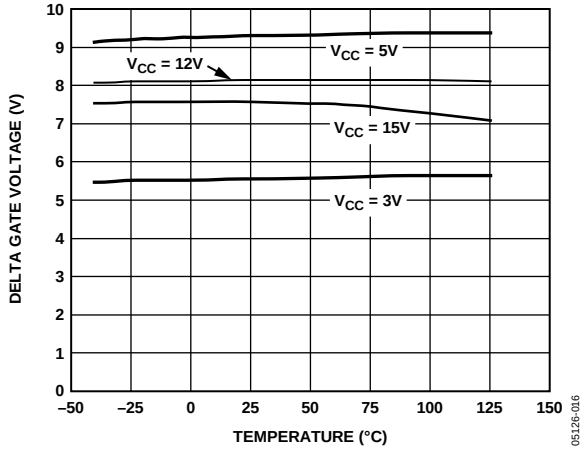


Figure 11. Delta GATE Voltage vs. Temperature

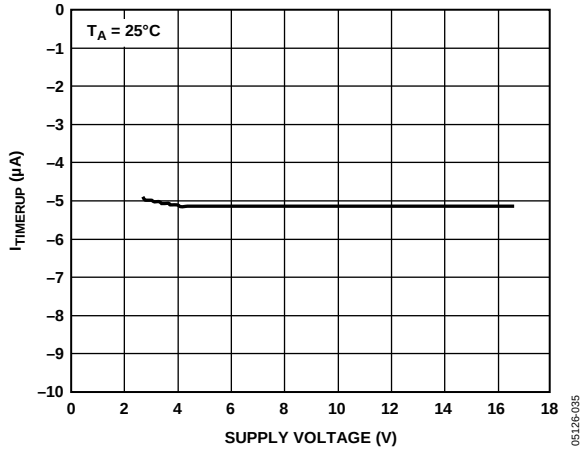


Figure 12. $I_{TIMERUP}$ (In Initial Cycle) vs. Supply Voltage

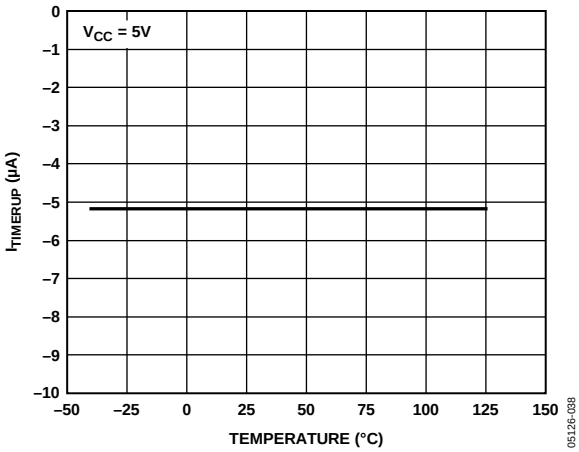


Figure 13. $I_{TIMERUP}$ (In Initial Cycle) vs. Temperature

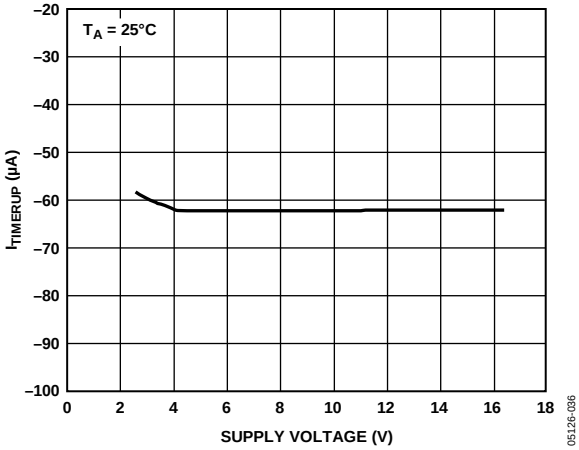


Figure 14. $I_{TIMERUP}$ (During Cct Breaker Delay) vs. Supply Voltage

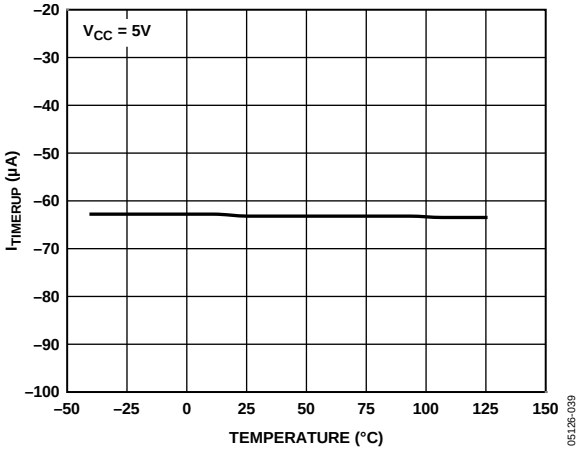


Figure 15. $I_{TIMERUP}$ (During Cct Breaker Delay) vs. Temperature

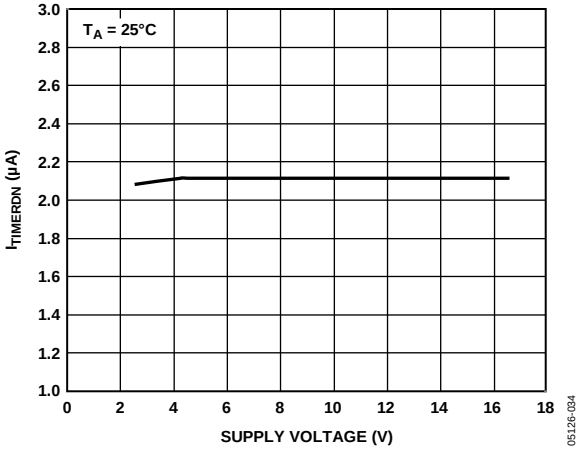


Figure 16. $I_{TIMERDN}$ (In Cool-Off Cycle) vs. Supply Voltage

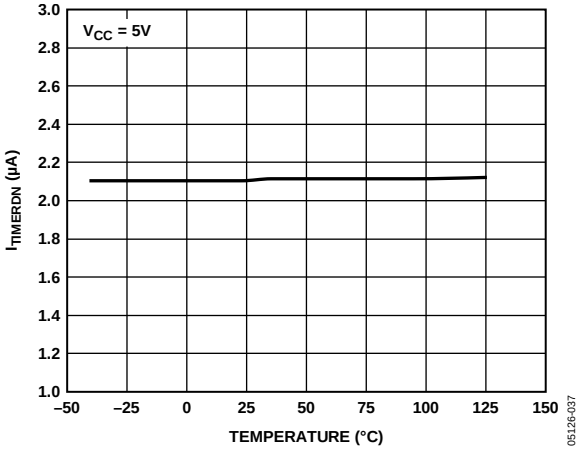


Figure 17. $I_{TIMERDN}$ (In Cool-Off Cycle) vs. Temperature

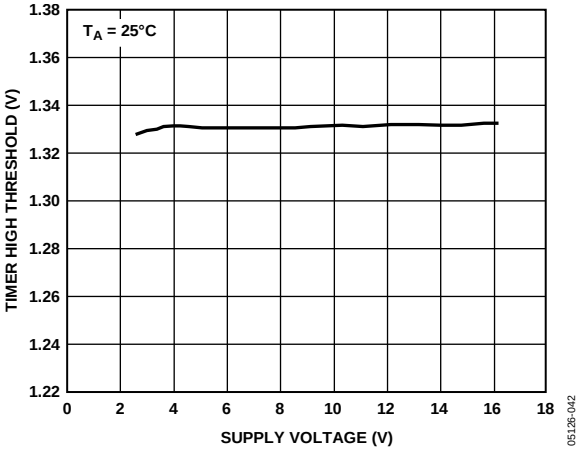


Figure 18. TIMER High Threshold vs. Supply Voltage

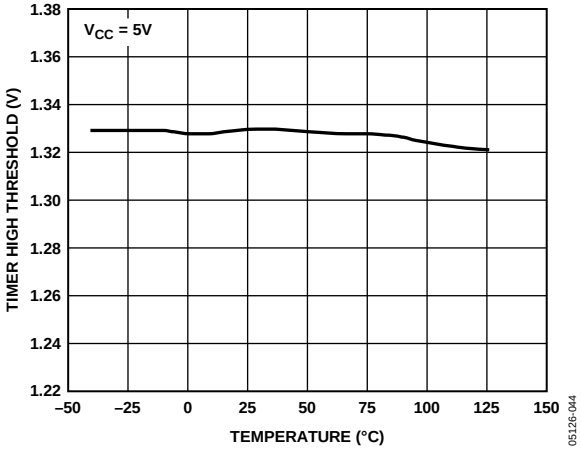


Figure 19. TIMER High Threshold vs. Temperature

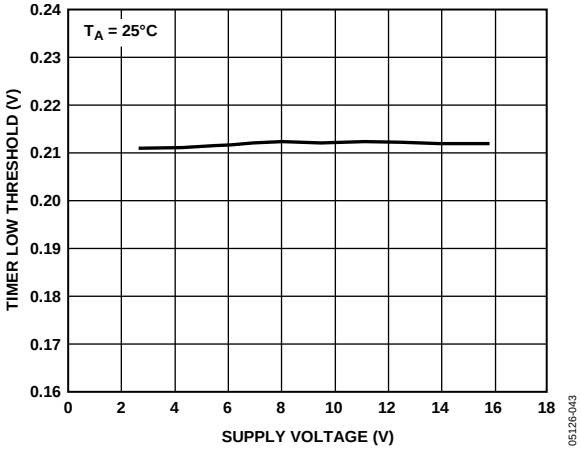


Figure 20. TIMER Low Threshold vs. Supply Voltage

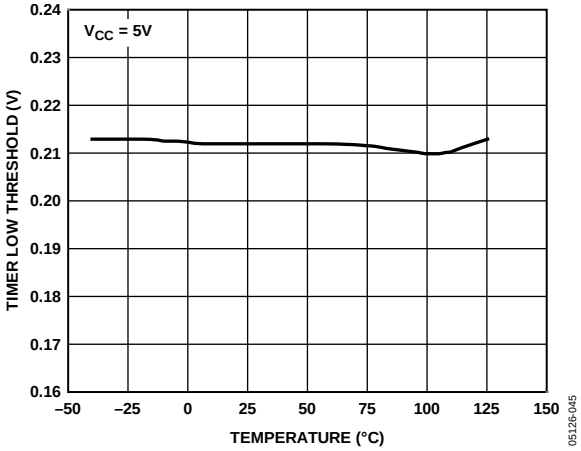


Figure 21. TIMER Low Threshold vs. Temperature

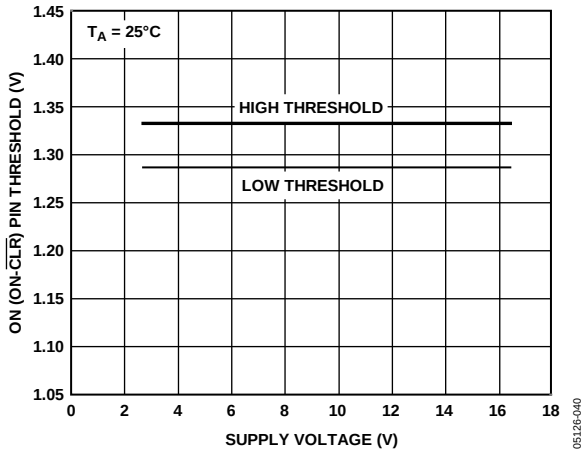


Figure 22. ON (ON-$\overline{CLR}$) Pin Threshold vs. Supply Voltage

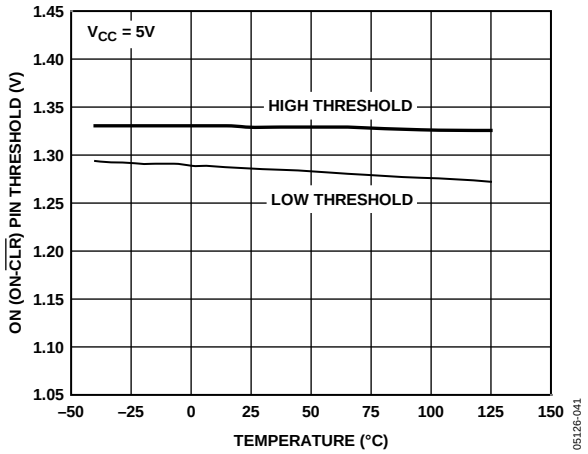


Figure 23. ON (ON-$\overline{CLR}$) Pin Threshold vs. Temperature

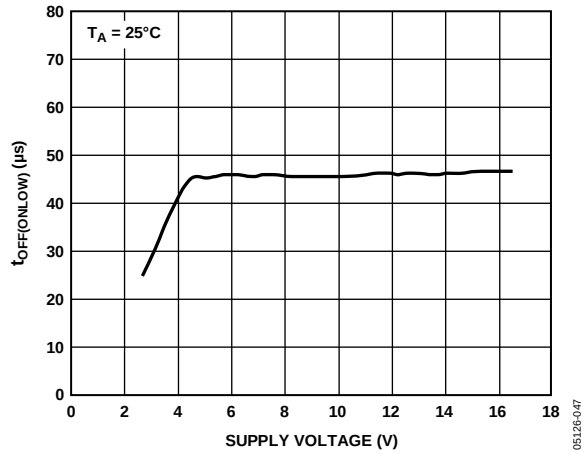


Figure 24. $t_{OFF(ONLOW)}$ vs. Supply Voltage

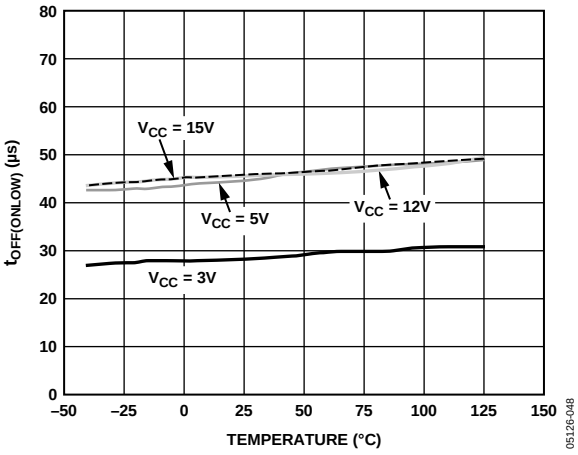


Figure 25. $t_{OFF(ONLOW)}$ vs. Temperature

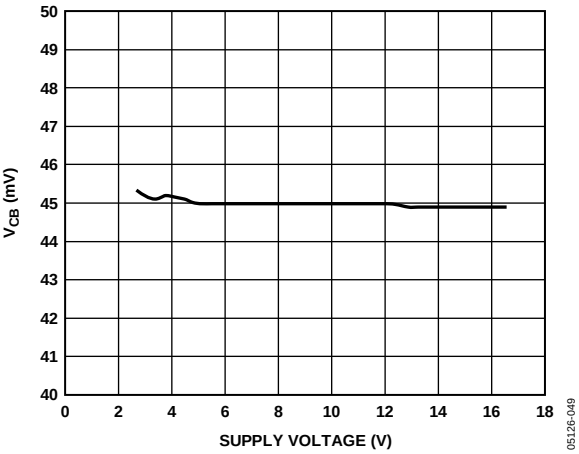


Figure 26. Cct Breaker Voltage vs. Supply Voltage

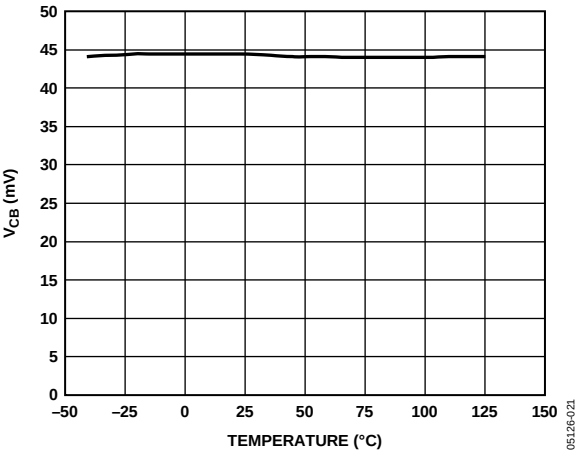


Figure 27. Cct Breaker Voltage vs. Temperature

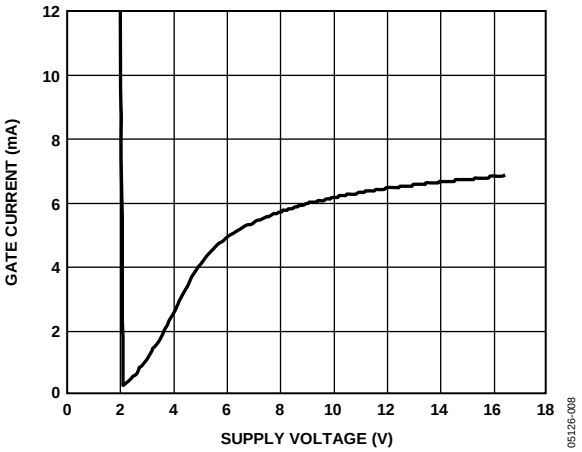


Figure 28. GATE Current (Down) vs. Supply Voltage

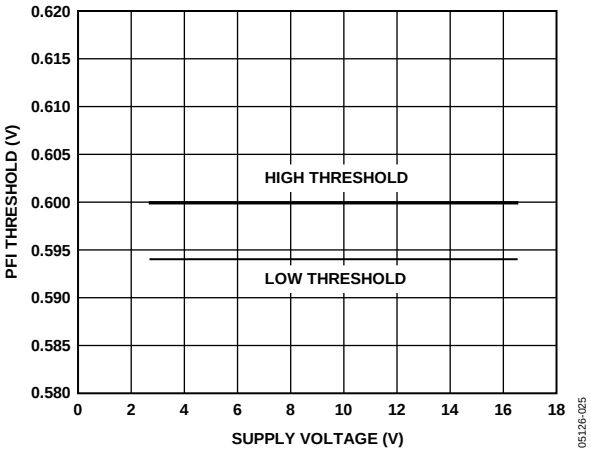


Figure 31. PFI Threshold vs. Supply Voltage

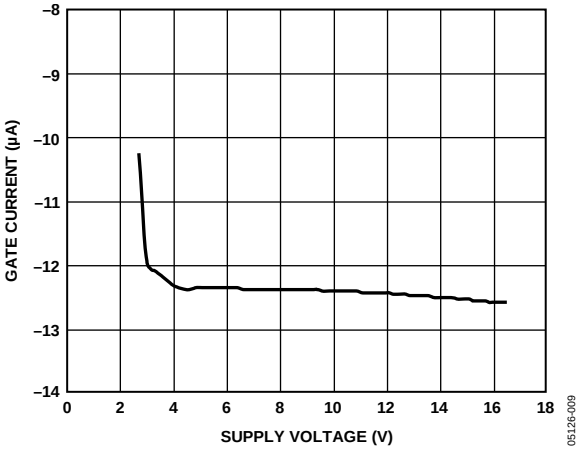


Figure 29. GATE Current (Up) vs. Supply Voltage

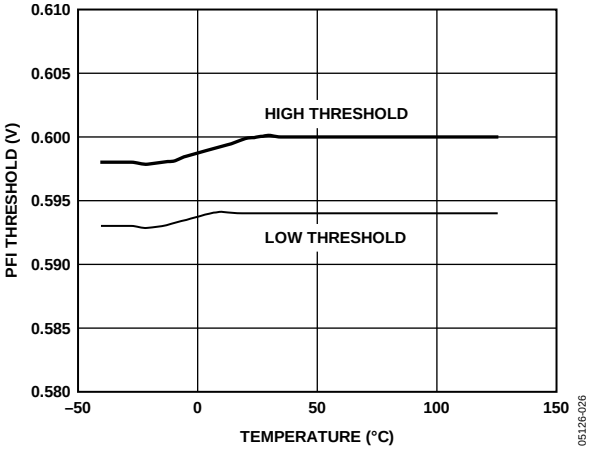


Figure 32. PFI Threshold vs. Temperature

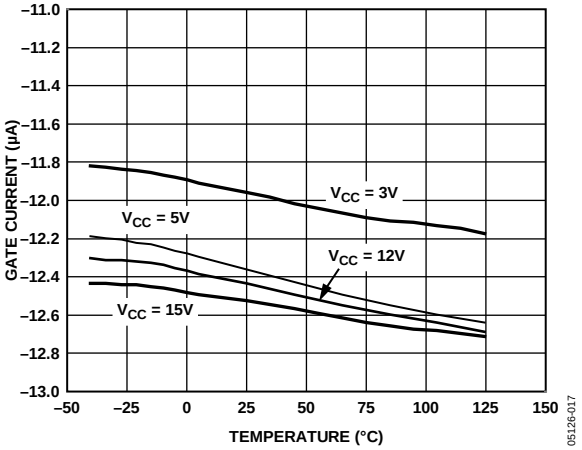


Figure 30. GATE Current (up) vs. Temperature

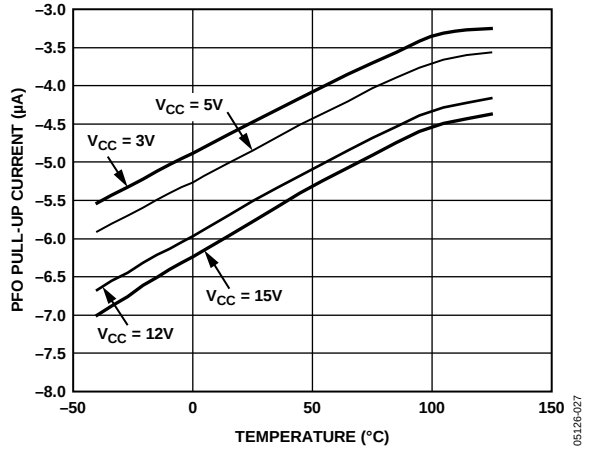


Figure 33. PFO Pull-Up Current vs. Temperature

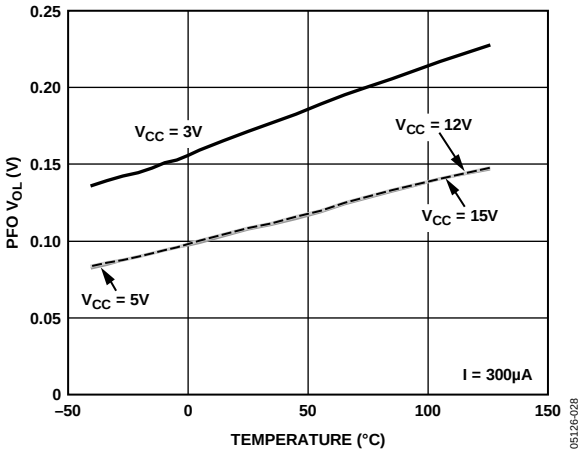


Figure 34. PFO Output Low Voltage vs. Temperature, I = 300 µA

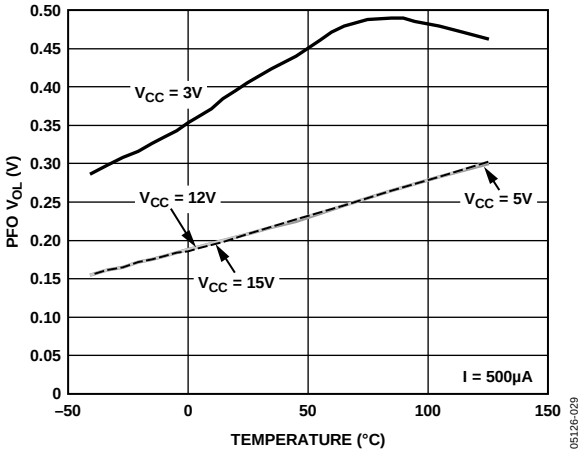


Figure 35. PFO Output Low Voltage vs. Temperature, I = 500 µA

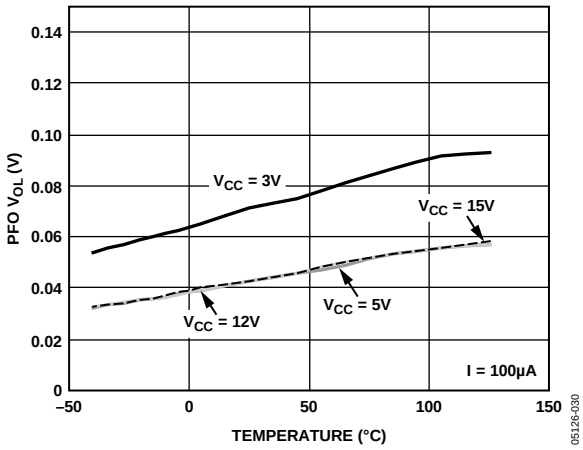


Figure 36. PFO Output Low Voltage vs. Temperature, I = 100 µA

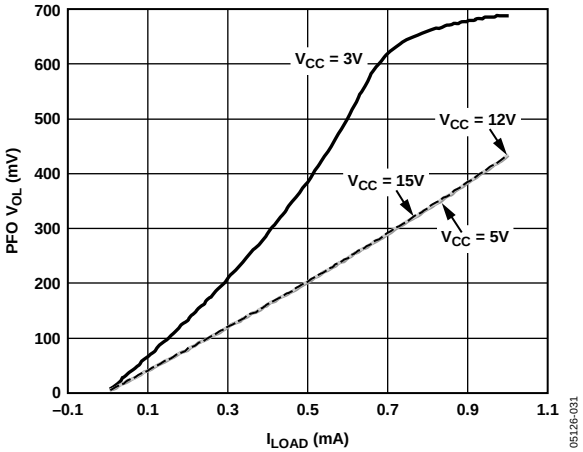


Figure 37. PFO Output Low Voltage vs. Load Current

THEORY OF OPERATION

Many systems require the insertion or removal of circuit boards to live backplanes. During this event, the supply bypass and hold-up capacitors can require substantial transient currents from the backplane power supply as they charge. These currents can cause permanent damage to connector pins or undesirable glitches and resets to the system.

The ADM1172 is intended to control the powering of a system (on and off) in a controlled manner, allowing the board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1172 can reside either on the backplane or on the removable board.

OVERVIEW

The ADM1172 operates over a supply range of 2.7 V to 16.5 V. As the supply voltage is coming up, an undervoltage lockout circuit checks if sufficient supply voltage is present for proper operation. During this period, the FET is held off by the GATE pin being held to GND. When the supply voltage reaches a level above UVLO and the ON (ON-$\overline{\text{CLR}}$) pin is high, an initial timing cycle ensures that the board is fully inserted in the backplane before turning on the FET. The TIMER pin capacitor sets the periods for all of the TIMER pin functions. After the initial timing cycle, the ADM1172 monitors the inrush current through an external sense resistor. Overcurrent conditions are actively limited to 50 mV/R_{SENSE} for the circuit breaker timer limit. The ADM1172-1 automatically retries after a current limit fault and the ADM1172-2 latches off. The retry duty cycle on the ADM1172-1 timer function is limited to 3.8% for FET cooling.

UVLO

If the V_{CC} supply is too low for normal operation, an under-voltage lockout circuit holds the ADM1172 in reset. The GATE pin is held to GND during this period. When the supply reaches this UVLO voltage, the ADM1172 starts when the ON (ON-$\overline{\text{CLR}}$) pin condition is satisfied.

ON (ON-$\overline{\text{CLR}}$) PIN

The ON (ON-$\overline{\text{CLR}}$) pin is the enable pin. It is connected to a comparator that has a low-to-high threshold of 1.3 V with 80 mV hysteresis and a glitch filter. The ADM1172 is reset when the ON (ON-$\overline{\text{CLR}}$) pin is low. When the ON (ON-$\overline{\text{CLR}}$) pin is high, the ADM1172 is enabled. A rising edge on this pin has the added function of clearing a fault and restarting the device on the latched off model, the ADM1172-2. A low input on the ON (ON-$\overline{\text{CLR}}$) pin turns off the external FET by pulling the GATE pin to ground and resets the timer. An external resistor divider at the ON (ON-$\overline{\text{CLR}}$) pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit. There is a glitch filter delay of approximately 3 µs on rising allowing the addition of an RC filter at the ON (ON-$\overline{\text{CLR}}$) pin to increase the delay time at card insertion. If using a short pin system to enable the device, a pull-down resistor should be used to hold the device prior to insertion.

GATE

Gate drive for the external N-channel MOSFET is achieved using an internal charge pump. The gate driver consists of a 12 µA pull-up from the internal charge pump. There are various pull-down devices on this pin. At a hotswap condition the board is hot inserted to the supply bus. During this event, it is possible for the external FET GATE capacitance to be charged up by the sudden presence of the supply voltage. This can cause uncontrolled inrush currents. An internal strong pull-down circuit holds GATE low while in UVLO. This reduces current surges at insertion. After the initial timing cycle, the GATE is then pulled high. During an overcurrent condition, the ADM1172 servos the GATE pin in an attempt to maintain a constant current to the load until the circuit breaker timeout completes. In the event of a timeout, the GATE pin abruptly shuts down using the 4 mA pull-down device. Care must be taken not to load the GATE pin resistively because this reduces the gate drive capability.

CURRENT LIMIT FUNCTION

The ADM1172 features a fast response current control loop that actively limits the current by reducing the gate voltage of the external FET. This current is measured by monitoring the voltage drop across an external sense resistor. The ADM1172 tries to regulate the gate of the FET to achieve a 50 mV voltage drop across the sense resistor.

CALCULATING THE CURRENT LIMIT

The sense resistor connected between V_{CC} and the SENSE pin is used to determine the nominal fault current limit. This is given by the following equation:

$$ILIMIT_{NOM} = VCB_{NOM}/RSENSE_{NOM} \quad (1)$$

The minimum load current is given by Equation 2

$$ILIMIT_{MIN} = VCB_{MIN}/RSENSE_{MAX} \quad (2)$$

The maximum load current is given by Equation 3.

$$ILIMIT_{MAX} = VCB_{MAX}/RSENSE_{MIN} \quad (3)$$

For proper operation, the minimum current limit must exceed the circuit maximum operating load current with margin. The sense resistor power rating must exceed

$$(VCB_{MAX})^2/RSENSE_{MIN}$$

CIRCUIT BREAKER FUNCTION

When the supply experiences a sudden current surge, such as a low impedance fault on load, the bus supply voltage can drop significantly to a point where the power to an adjacent card is affected, potentially causing system malfunctions. The ADM1172 limits the current drawn by the fault by reducing the

gate voltage of the external FET. This minimizes the bus supply voltage drop caused by the fault and protects neighboring cards.

As the voltage across the sense resistor approaches the current limit, a timer activates. This timer resets again if the sense voltage returns below this level. If the sense voltage is any voltage below 44 mV, the timer is guaranteed to be off. Should the current continue to increase, the ADM1172 tries to regulate the gate of the FET to achieve a limit of 50 mV across the sense resistor. However, if the device is unable to regulate the fault current and the sense voltage further increases, a larger pull-down, in the order of milliamperes, is enabled to compensate for fast current surges. If the sense voltage is any voltage greater than 56 mV, this pull-down is guaranteed to be on. When the timer expires, the GATE pin shuts down.

TIMER FUNCTION

The TIMER pin is responsible for several key functions on the ADM1172. A capacitor controls the initial power on reset time and the amount of time an overcurrent condition lasts before the FET shuts down. On the ADM1172-1, the timer pin also controls the time between auto retry pulses. There are pull-up and pull-down currents internally available to control the timer functions. The voltage on the TIMER pin is compared with two threshold voltages: COMP1 (0.2 V) and COMP2 (1.3 V). The four timing currents are listed in Table 5.

Table 5.

Timing Current	Level (µA)
Pull-up	5
Pull-up	60
Pull-down	2
Pull-down	100

POWER-UP TIMING CYCLE

The ADM1172 is in reset when the ON (ON-$\overline{\text{CLR}}$) pin is held low. The GATE pin is pulled low and the TIMER pin is pulled low with a 100 µA pull-down. At Time Point 2 in Figure 38, the ON (ON-$\overline{\text{CLR}}$) pin is pulled high. For the device to startup correctly, the supply voltage must be above UVLO, the ON (ON-$\overline{\text{CLR}}$) pin must be above 1.3 V, and the TIMER pin voltage must be less than 0.2 V. The initial timing cycle begins when these three conditions are met, and the TIMER pin is pulled high with 5 µA. At Time Point 3, the TIMER reaches the COMP2 threshold.

This is the end of the first section of the initial cycle. The 100 µA current source then pulls down the TIMER pin until it reaches 0.2 V at Time Point 4. The initial cycle delay (Time Point 2 to Time Point 4) relates to C_{TIMER} by equation

$$t_{INITIAL} = 1.3 \times C_{TIMER}/5\ \mu A \quad (4)$$

When the initial cycle ends, a start-up cycle activates and the GATE pin is pulled high; the TIMER pin continues to pull down.

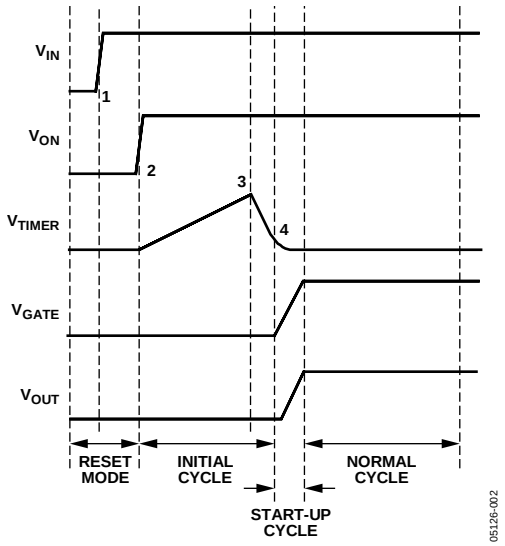


Figure 38. Power-Up Timing

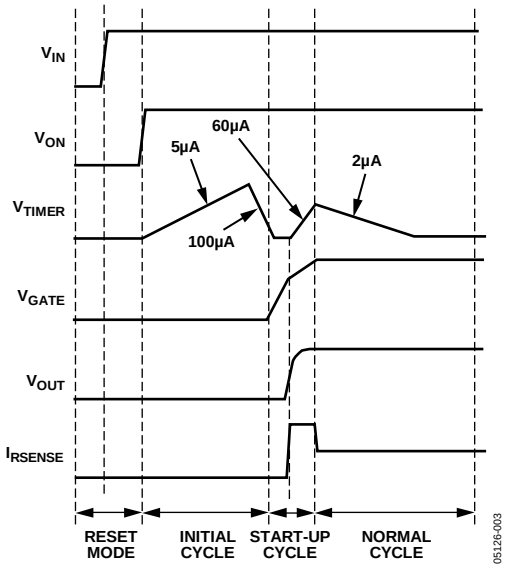


Figure 39. Power-Up into Capacitor

CIRCUIT BREAKER TIMING CYCLE

When the voltage across the sense resistor exceeds the circuit breaker trip voltage, the 60 µA timer pull-up current is activated. If the sense voltage falls below this level before the TIMER pin reaches 1.3 V, the 60 µA pull-up is disabled and the 2 µA pull-down is enabled. This is likely to happen if the overcurrent fault is only transient, such as an inrush current. This is shown in Figure 39. However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 µA pull-up remains active. This allows the TIMER pin to reach the high trip point of 1.3 V and initiate the GATE shutdown. On the ADM1172-2, the TIMER pin continues pulling up but switches to the 5 µA pull-up when it reaches the 1.3 V threshold. The device can be reset by toggling the ON-$\overline{\text{CLR}}$ pin or by manually pulling the TIMER pin low. On the ADM1172-1, the TIMER pin activates the 2 µA pull-down once the 1.3 V threshold is reached, and continues to pull down until it reaches the 0.2 V threshold. At this point, the 100 µA pull-down is activated and the GATE pin is enabled. The device keeps retrying in the manner as shown in Figure 40.

The duty cycle of this automatic retry cycle is set to the ratio of 2 µA/60 µA, which approximates 3.8% on. The value of the timer capacitor determines the on time of this cycle. This time is calculated as follows:

$$t_{ON} = 1.3 \times C_{TIMER}/60\ \mu A$$

$$t_{OFF} = 1.1 \times C_{TIMER}/2\ \mu A$$

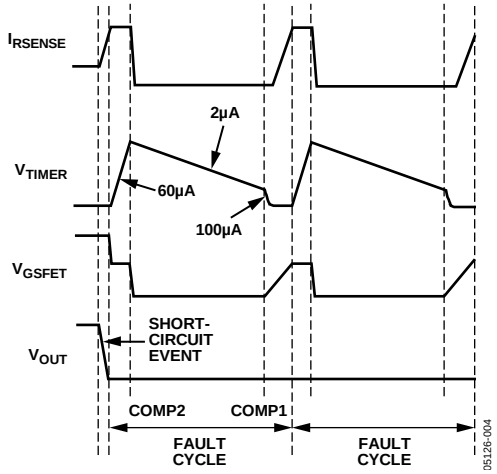


Figure 40. ADM1172-1 Automatic Retry During Overcurrent Fault

AUTOMATIC RETRY OR LATCHED OFF

The ADM1172 is available in two models. The ADM1172-1 has an automatic retry system whereby when a current fault is detected, the FET is shut down after a time determined by the timer capacitor, and it is switched on again in a controlled continuous cycle to determine if the fault remains (see Figure 40 for details). The period of this cycle is determined by the timer capacitor at a duty cycle of 3.8% on and 96.2% off.

The ADM1172-2 model has a latch off system whereby when a current fault is detected, the GATE is switched off after a time determined by the timer capacitor (see Figure 41 for details). Toggling the ON-$\overline{\text{CLR}}$ pin, or pulling the TIMER pin to GND for a brief period, resets this condition.

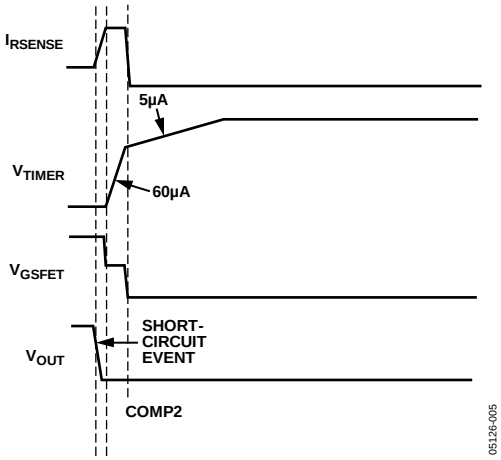
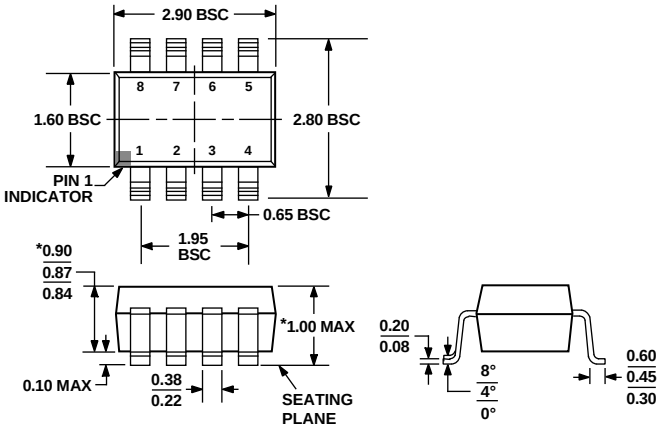


Figure 41. ADM1172-2 Latch Off After Overcurrent Fault

POWER-FAIL COMPARATOR

The ADM1172 has an integrated comparator that can be used as a power-fail/OV/UV detector. The comparator has a 0.6 V reference, and it is designed to be active high when the voltage on the PFI pin drops to below this threshold. The only action that results from the PFI pin tripping the comparator is the change of state on the PFO pin. The PFI pin can be used to monitor the supply on either side of the FET, for an OV or UV condition set by a resistor divider network. The PFO can then be sent to a control system and used as a power-good/power-fail signal. The PFO output has a 5 µA internal pull-up. A 10 kΩ resistor is recommended on the PFO pin to ensure that it is either pulled up or down during power-up. The pin is in high impedance while V_{CC} < UVLO and can result in invalid power-fail signals.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-BA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 42. 8-Lead Thin Small Outline Transistor Package [TSOT] (UJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADM1172-1AUJZ-RL7	−40°C to +85°C	8-Lead TSOT	UJ-8	M1M
ADM1172-2AUJZ-RL7	−40°C to +85°C	8-Lead TSOT	UJ-8	M1N
EVAL-ADM1172EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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