



MX23C3210

32M-BIT MASK ROM (8/16-BIT OUTPUT)

FEATURES

- Bit organization
 - 4M x 8 (byte mode)
 - 2M x 16 (word mode)
- Fast access time
 - Random access: 100ns (max.)
- Current
 - Operating: 60mA
 - Standby: 100uA
- Supply voltage
 - 5V±10%
- Package
 - 44 pin SOP (500mil)
 - 48 pin TSOP (20mm x 12mm)
 - 42 pin DIP (600 mil) (word mode)

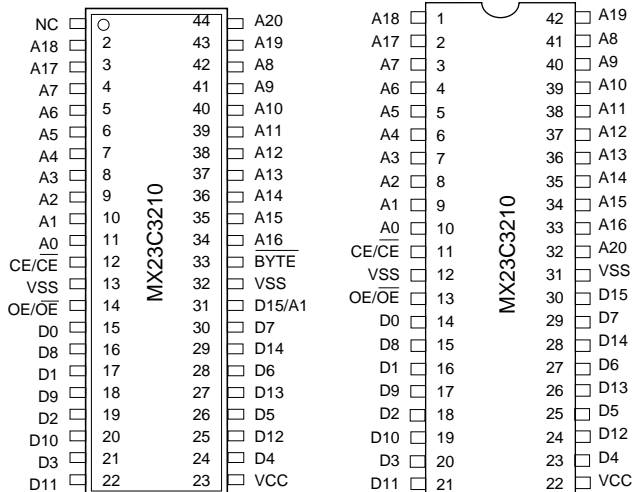
ORDER INFORMATION

| Part No. | Access Time | Package |
|----------------|-------------|-------------------------------|
| MX23C3210MC-10 | 100ns | 44 pin SOP |
| MX23C3210MC-12 | 120ns | 44 pin SOP |
| MX23C3210MC-15 | 150ns | 44 pin SOP |
| MX23C3210TC-10 | 100ns | 48 pin TSOP |
| MX23C3210TC-12 | 120ns | 48 pin TSOP |
| MX23C3210TC-15 | 150ns | 48 pin TSOP |
| MX23C3210RC-10 | 100ns | 48 pin TSOP (Reverse type) |
| MX23C3210RC-12 | 120ns | 48 pin TSOP (Reverse type) |
| MX23C3210RC-15 | 150ns | 48 pin TSOP (Reverse type) |
| MX23C3210PC-10 | 100ns | 42 pin DIP |
| MX23C3210PC-12 | 120ns | 42 pin DIP |
| MX23C3210PC-15 | 150ns | 42 pin DIP |

PIN CONFIGURATION

44 SOP

42 DIP (For Word Mode Only)



PIN DESCRIPTION

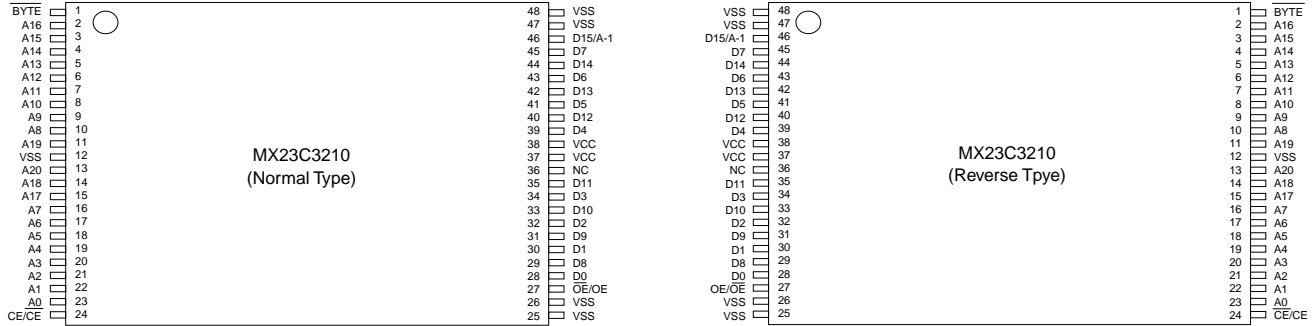
| Symbol | Pin Function |
|---------|---|
| A0~A20 | Address Inputs |
| D0~D14 | Data Outputs |
| D15/A-1 | D15 (Word Mode)/ LSB Address (Byte Mode) |
| CE/CE | Chip Enable Input |
| OEOE | Output Enable Input |
| Byte | Word/ Byte Mode Selection |
| VCC | Power Supply Pin |
| VSS | Ground Pin |
| NC | No Connection |

MODE SELECTION

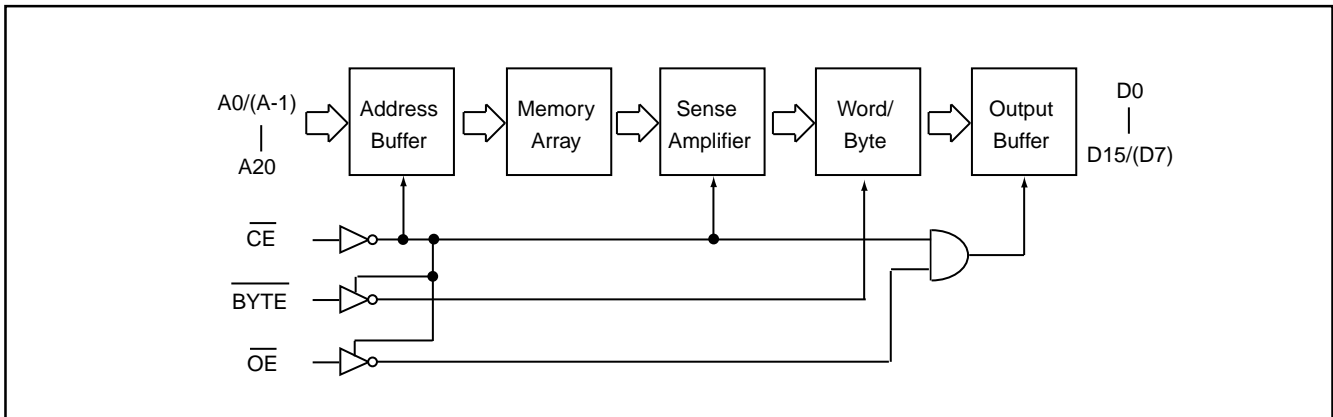
| CE/CE | OE/OE | Byte | D15/A-1 | D0~D7 | D8~D15 | Mode | Power |
|-------|-------|------|---------|--------|--------|------|----------|
| L/H | X | X | X | High Z | High Z | - | Stand-by |
| H/L | L/H | X | X | High Z | High Z | - | Active |
| H/L | H/L | H | Output | D0~D7 | D8~D15 | Word | Active |
| H/L | H/L | L | Input | D0~D7 | High Z | Byte | Active |

48 TSOP (Normal Type)

48 TSOP (Reverse Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings |
|------------------------------------|--------|----------------|
| Voltage on any Pin Relative to VSS | VIN | -0.5V to 7.0V |
| Ambient Operating Temperature | Topr | 0°C to 70°C |
| Storage Temperature | Tstg | -65°C to 125°C |



DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

| Item | Symbol | MIN. | MAX. | Conditions |
|------------------------|--------|-------|----------|------------------------------|
| Output High Voltage | VOH | 2.4V | - | IOH = -1.0mA |
| Output Low Voltage | VOL | - | 0.4V | IOL = 2.1mA |
| Input High Voltage | VIH | 2.2V | VCC+0.3V | |
| Input Low Voltage | VIL | -0.3V | 0.8V | |
| Input Leakage Current | ILI | - | 5uA | 0V, VCC |
| Output Leakage Current | ILO | - | 5uA | 0V, VCC |
| Operating Current | ICC1 | - | 60mA | tRC = 100ns, all output open |
| Standby Current (TTL) | ISTB1 | - | 1mA | \overline{CE} = VIH |
| Standby Current (cmos) | ISTB2 | - | 100uA | \overline{CE} > VCC-0.2V |
| Input Capacitance | CIN | - | 10pF | Ta = 25°C, f = 1MHZ |
| Output Capacitance | COUT | - | 10pF | Ta = 25°C, f = 1MHZ |

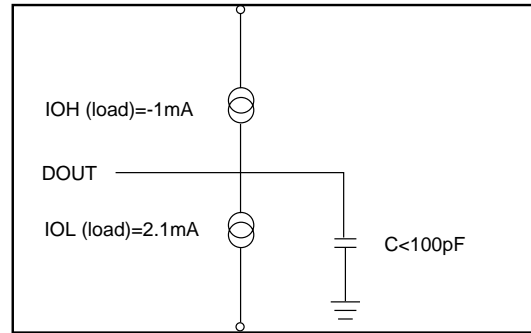
AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

| Item | Symbol | 23C3210-10 | | 23C3210-12 | | 23C3210-15 | |
|---------------------------|--------|------------|-------|------------|-------|------------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |
| Read Cycle Time | tRC | 100ns | - | 120ns | - | 150ns | - |
| Address Access Time | tAA | - | 100ns | - | 120ns | - | 150ns |
| Chip Enable Access Time | tACE | - | 100ns | - | 120ns | - | 150ns |
| Output Enable Time | tOE | - | 50ns | - | 60ns | - | 70ns |
| Output Hold After Address | tOH | 0ns | - | 0ns | - | 0ns | - |
| Output High Z Delay | tHZ | - | 20ns | - | 20ns | - | 20ns |

Note: Output high-impedance delay (tHZ) is measured from OE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

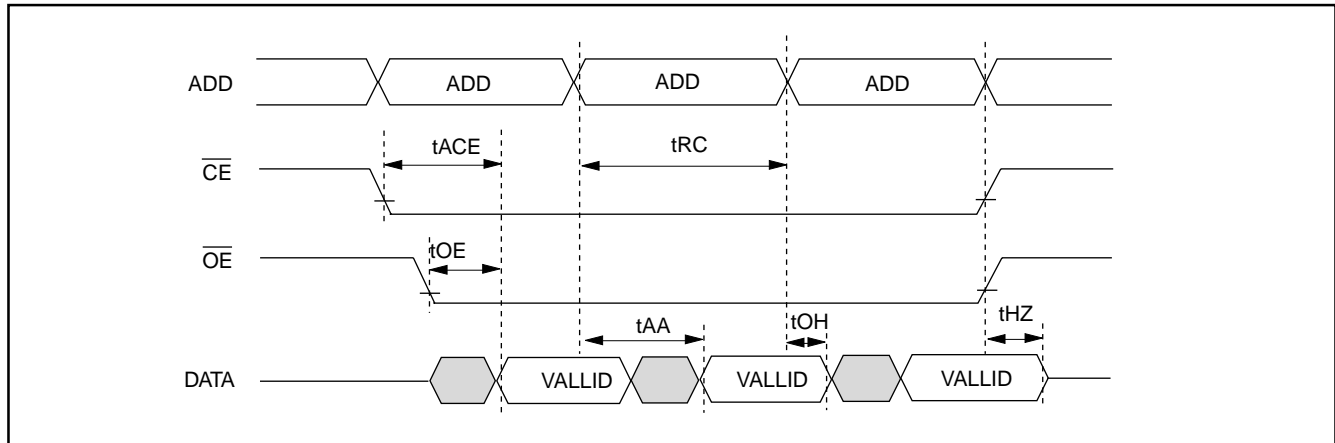
| | |
|---------------------------|---------------|
| Input Pulse Levels | 0.4V~2.4V |
| Input Rise and Fall Times | 10ns |
| Input Timing Level | 1.5V |
| Output Timing Level | 0.8V and 2.0V |
| Output Load | See Figure |



Note: No output loading is present in tester load board.
 Active loading is used and under software programming control.
 Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ

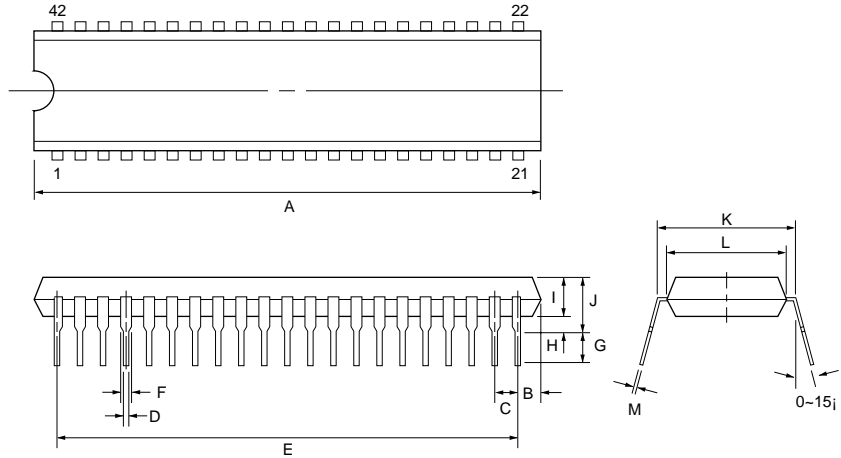


PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)

| ITEM | MILLIMETERS | INCHES |
|------|-------------|-------------|
| A | 52.54 max. | 2.070 max. |
| B | 0.76 [REF] | .030 [REF] |
| C | 2.54 [TP] | .100 [TP] |
| D | .46 [Typ.] | .018 [Typ.] |
| E | 50.76 | 2.000 |
| F | 1.27 [Typ.] | .050 [Typ.] |
| G | 3.30 ± .25 | .130 ± .010 |
| H | .51 [REF] | .020 [REF] |
| I | 3.94 ± .25 | .155 ± .010 |
| J | 5.33 max. | .210 max. |
| K | 15.22 ± .25 | .600 ± .010 |
| L | 13.97 ± .25 | .550 ± .010 |
| M | .25 [Typ.] | .010 [Typ.] |

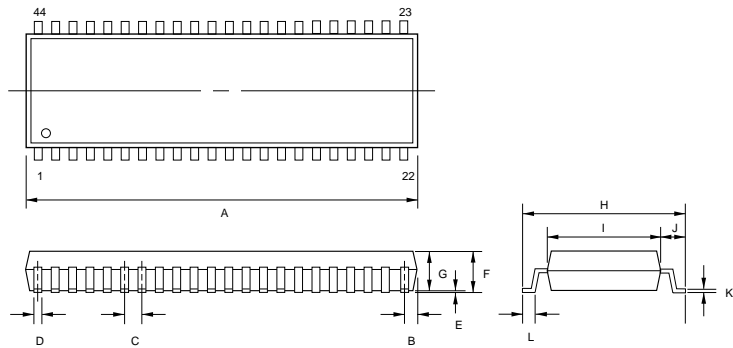
NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



44-PIN PLASTIC SOP

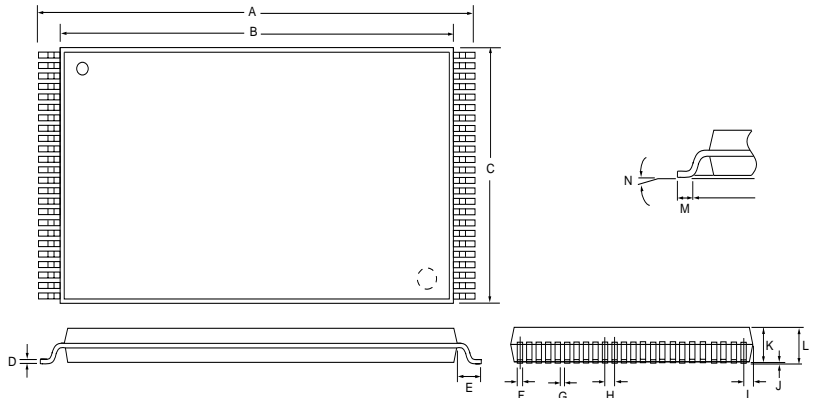
| ITEM | MILLIMETERS | INCHES |
|------|------------------|--------------------|
| A | 28.70 max. | 1.130 max. |
| B | 1.10 [REF] | .043 [REF] |
| C | 1.27 [TP] | .050 [TP] |
| D | .40 ± .10 [Typ.] | .016 ± .004 [Typ.] |
| E | .010 min. | .004 min. |
| F | 3.00 max. | .118 max. |
| G | 2.80 ± .13 | .110 ± .005 |
| H | 16.04 ± .30 | .631 ± .012 |
| I | 12.60 | .496 |
| J | 1.72 | .068 |
| K | .15 ± .10 [Typ.] | .006 ± .004 [Typ.] |
| L | .80 ± .20 | .031 ± .008 |

NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



48-PIN PLASTIC TSOP

| ITEM | MILLIMETERS | INCHES |
|------|-------------|-------------|
| A | 20.0 ± .20 | .787 ± .008 |
| B | 18.40 ± .10 | .724 ± .004 |
| C | 12.20 max. | .480 max. |
| D | 0.15 [Typ.] | .006 [Typ.] |
| E | .80 [Typ.] | .031 [Typ.] |
| F | .20 ± .10 | .008 ± .004 |
| G | .30 ± .10 | .012 ± .004 |
| H | .50 [Typ.] | .020 [Typ.] |
| I | .45 max. | .018 max. |
| J | 0 ~ .20 | 0 ~ .008 |
| K | 1.00 ± .10 | .039 ± .004 |
| L | 1.27 max. | .050 max. |
| M | .50 | .020 |
| N | 0 ~ 5° | .500 |



NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

| Revision | Description | Page | Date |
|----------|---|------|-------------|
| 2.6 | DC Characteristics: The input leakage current (ILI) is changed as 5uA instead of 10uA. The output leakage current (ILO) is changed as 5uA instead 10uA. The power down supply current (ISTB2) is changed as 100uA instead of 5uA. | | |
| 2.7 | AC Characteristics: Added 100ns grade item, deleted 200ns grade item. The output enable time (tOE) is changed as 60ns instead of 70ns in 120ns grade item, and 70ns instead of 80ns grade item. The output high Z delay is changed as 20ns instead of 70ns. | | MAR/25/1998 |
| 2.8 | AC Characteristics: tOH 10ns --> 0ns | P3 | FEB/01/1999 |



MX23C3210

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