P3P8163A

3.3V, LVCMOS Spread Spectrum Peak EMI Reduction Device

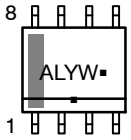
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MARKING DIAGRAM



SOIC−8
D SUFFIX
CASE 751



xx	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Product Description

P3P8163A is a 3.3 V, spread spectrum frequency modulator that generates a 1x, LVCMOS low EMI spread spectrum clock and two reference clock outputs.

The P3P8163A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The P3P8163A can generate an EMI reduced clock from a fundamental Crystal or from an external reference clock.

P3P8163A has a SEL pin to turn off CLK2 when ‘1’.
Refer Output Table.

P3P8163A operates over 3.3 V ±5% supply voltage range and is available in 8 pin SOIC package.

Features

- Input Clock: 12 MHz from Fundamental XTAL or External Reference Clock
- Output Clocks:
  CLK0: 12 MHz ±0.4%
  CLK1, CLK2: 12 MHz (REFOUT)
- SEL Pin to Turn Off CLK2
- Low Inherent Cycle−to−Cycle Jitter
- Supply Voltage: 3.3 V ±5%
- LVCMOS Input and Output
- Operating Temperature Range: 0°C to 70°C
- 8−pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Application

- The P3P8163A is targeted towards EMI management in consumer electronics applications including MFPs.

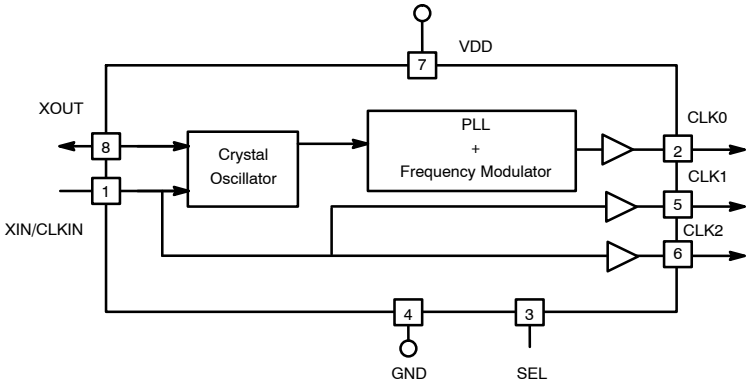


Figure 1. Simplified Block Diagram

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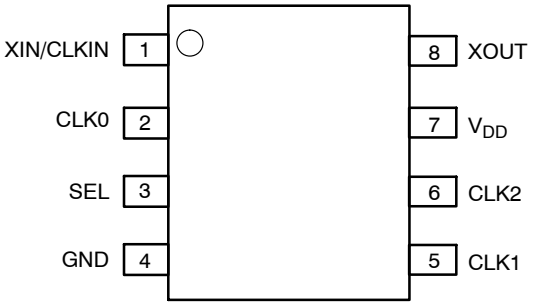


Figure 2. Pin Configuration

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	XIN / CLKIN	Input	Crystal connection or External Clock input.
2	CLK0	Output	Spread Spectrum Clock output.
3	SEL	Input	2 level logic input. When '0' CLK2 is enabled. When '1' CLK2 is turned off. Has a Pull−down resistor.
4	GND	Power	Ground to entire chip.
5	CLK1	Output	Reference clock Output.
6	CLK2	Output	Reference clock Output. Has a Pull−down resistor when OFF.
7	V_{DD}	Power	Power supply for the entire chip
8	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.

Table 2. OUTPUT TABLE

SEL	CLK0	CLK1	CLK2
0	Spread Spectrum Clock output	Reference clock Output	Reference clock Output
1	Spread Spectrum Clock output	Reference clock Output	OFF

Table 3. OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
V_{DD}	Voltage on any pin with respect to GND	3.135	3.465	V
T_A	Operating temperature	0	+70	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage(As per JEDEC STD 22− A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS

(NOTE − Unless otherwise stated V_{DD} = 3.3 V ± 5%, C_L = 15 pF and Ambient Temperature range 0°C to +70°C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Dynamic supply current (C_L = 15 pF, V_{DD} = 3.465 V, Temp = +70°C)				17	mA
V_{IL}	Input low voltage (XIN/CLKIN, SEL Inputs)		0		0.8	V
V_{IH}	Input high voltage (XIN/CLKIN, SEL Inputs)		0.9 * V_{DD}		V_{DD}	V
V_{OL}	Output low voltage (CLK[0:2])	I_{OL} = 12 mA			0.4	V
V_{OH}	Output high voltage (CLK[0:2])	I_{OH} = −12 mA	2.4			V
C_{IN1}	Input Capacitance (XIN/CLKIN and XOUT)			6		pF
C_{IN2}	Input capacitance (SEL Input)				7	pF
R_{PD}	Internal Pull down Resistor (CLK2)			200		kΩ
Z_0	Output Impedance			25		Ω

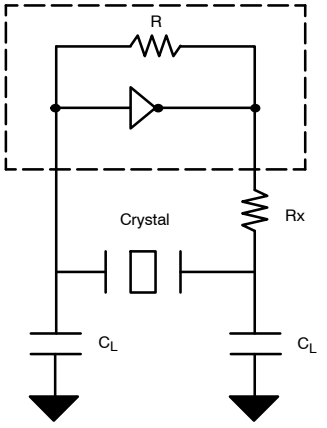
NOTE: The voltage on any input or I/O pin cannot exceed the power pin during power up.

Table 6. AC ELECTRICAL CHARACTERISTICS

(NOTE − Unless otherwise stated V_{DD} = 3.3 V ± 5%, C_L = 15 pF and Ambient Temperature range 0°C to +70°C)

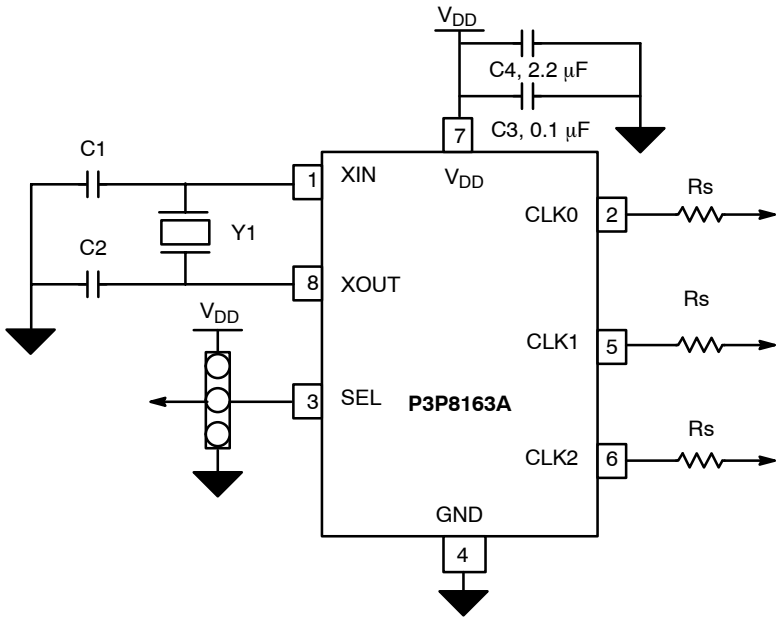
Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Clock frequency		12		MHz
f_{OUT}	CLK0, Modulated output Clock, ±0.4%		12		MHz
	CLK1, CLK2 Reference clock output		12		
t_{LH}, t_{HL} (Notes 1 and 2)	CLK0, Rise and Fall time (Measured between 20% to 80%)		1.25	2.0	ns
t_{LH}, t_{HL} (Notes 1 and 2)	CLK1, CLK2, Rise and Fall time (Measured between 20% to 80%)		1.25	2.0	ns
TDCOUT (Notes 1 and 2)	Output Clock Duty Cycle	45	50	55	%
T_{JC} (Note 2)	Cycle−Cycle Jitter, Peak (1000 cycles) (For CLK0)		150		pS
T_{JP} (Note 2)	Period Jitter, Peak (10000 cycles) (For CLK1, CLK2)		125		pS
t_{ON} (Notes 1 and 2)	Power Up Time (Stable power supply, valid input clock to valid clock on CLK0).			4	ms
f_{dvar}	Frequency Deviation (CLK0)		±0.4	±0.52	%

1. Parameters are specified with 15 pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production



$C_L = 2*(C_P - C_S)$,
Where C_P = Load capacitance of crystal specified in a Crystal Datasheet
CS = Stray capacitance due to CIN, PCB, Trace etc
C_L =Load capacitance to be used
Rx is used to reduce power dissipation in the Crystal

Figure 3. Typical Crystal Interface Circuit



Rs = Trace Impedance of PCB − Output Impedance of Device (Z0)

Figure 4. Typical Application Schematic

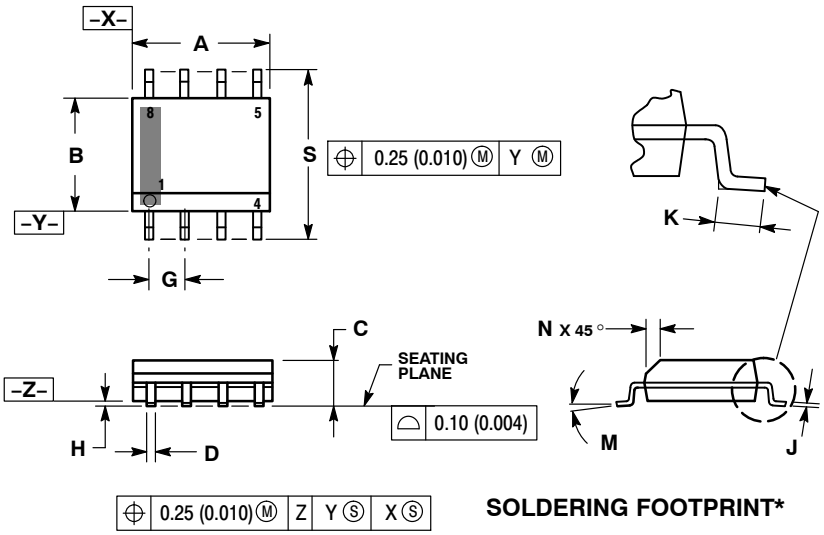
ORDERING INFORMATION

Device	Top Marking	Temperature	Package	Shipping†
P3P8163AG−08SR	CUL	0°C to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AK

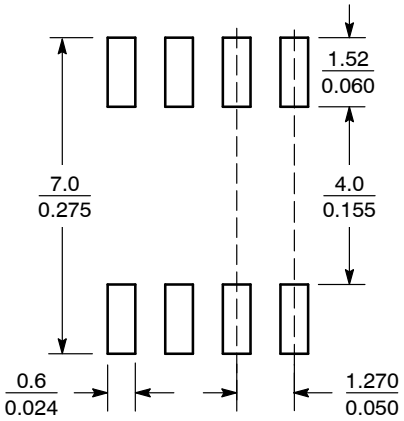


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0.25 (0.010) M Z Y S X S

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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