ML2280*, ML2283**

Serial I/O 8-Bit A/D Converters

GENERAL DESCRIPTION

The ML2280 and ML2283 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 4 input channels.

All errors of the sample-and-hold incorporated on the ML2280 and ML2283 are accounted for in the analog-to-digital converters accuracy specification.

The voltage reference can be externally set to any value between GND and V_{CC}, thus allowing a full conversion over a relatively small voltage span if desired.

The ML2283 is an enhanced double polysilicon, CMOS, pin-compatible second source for the ADC0833 A/D converter. All parameters are guaranteed over temperature with a power supply voltage of 5V ±10%.

FEATURES

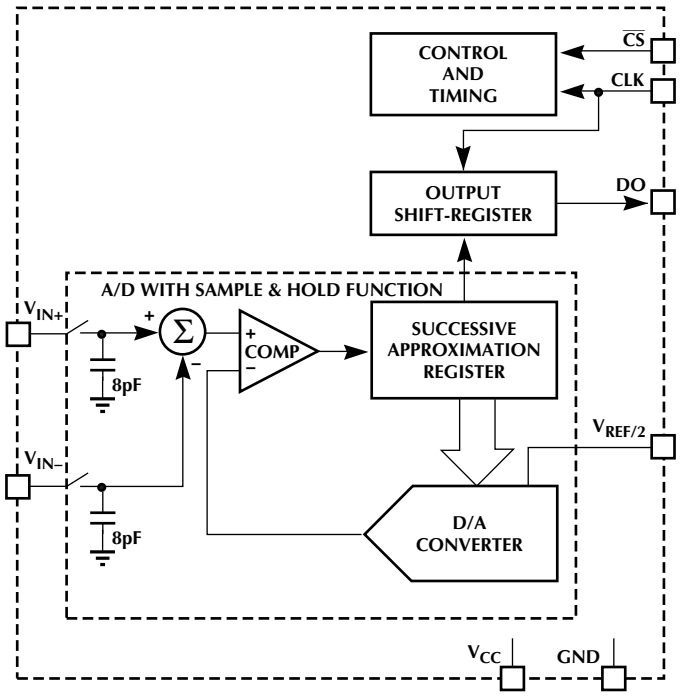
- Conversion time: 6µs
- ML2280 capable of digitizing a 5V, 40kHz sine wave
- Total unadjusted error with external reference: ±1/2LSB or ±1LSB
- Sample-and-hold: 375ns acquisition
- 0 to 5V analog input range with single 5V power supply
- 2.5V reference provides 0 to 5V analog input range
- No zero- or full-scale adjust required
- Low power: 12.5mW MAX
- Analog input protection: 25mA (min) per input
- Differential analog voltage inputs (ML2280)
- Programmable multiplexer with differential or single ended analog inputs (ML2283)
- 0.3" width 8- or 14-pin DIP, or 8-Pin SOIC (ML2280)
- Superior pin-compatible replacement for ADC0833

* This Part Is Obsolete

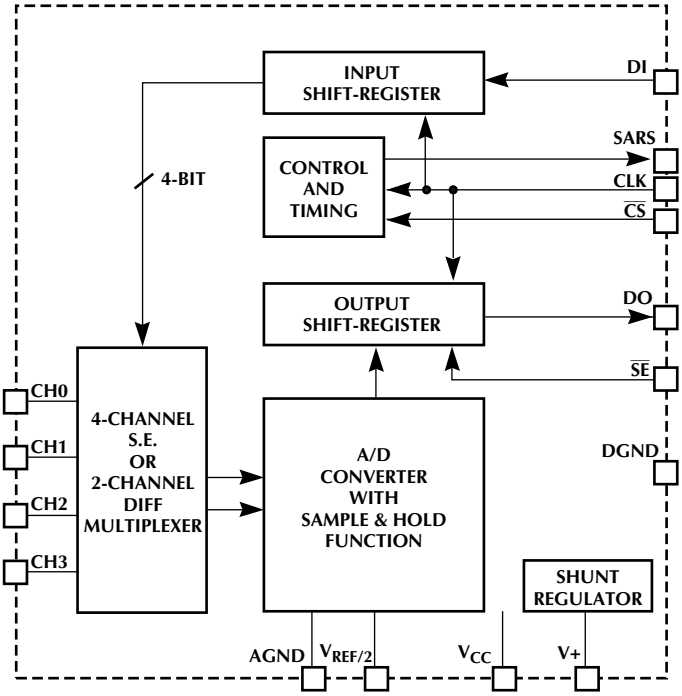
** This Part Is End Of Life As Of August 1, 2000

BLOCK DIAGRAM

ML2281

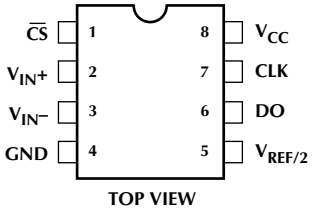


ML2283



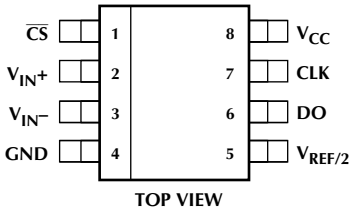
PIN CONFIGURATION

ML2280
Single Differential Input
8-Pin PDIP



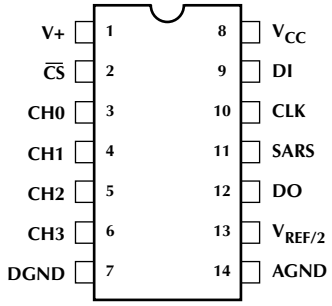
TOP VIEW

ML2280
Single Differential Input
8-Pin SOIC



TOP VIEW

ML2283
4-Channel MUX
14-Pin PDIP



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	Positive supply. 5V ± 10%
DGND	Digital ground. 0 volts. All digital inputs and outputs are referenced to this point.
AGND	Analog ground. The negative reference voltage for A/D converter.
GND	Combined analog and digital ground.
CH0, $V_{IN}+$, $V_{IN}-$	Analog inputs. Digitally selected to be single ended (V_{IN}) or; $V_{IN}+$ or $V_{IN}-$ of a differential input. Analog range = GND - V_{IN} - V_{CC}.
$V_{REF/2}$	Reference. The analog input range is twice the positive reference voltage value applied to this pin.
V+	Input to the Shunt Regulator.
DO	Data out. Digital output which contains result of A/D conversion. The serial data is clocked out on falling edges of CLK.
SARS	Successive approximation register status. Digital output which indicates that a conversion is in progress. When SARS goes to 1, the sampling window is closed and conversion begins. When SARS goes to 0, conversion is completed. When $\overline{CS}$ = 1, SARS is in high impedance state.
CLK	Clock. Digital input which clocks data in on DI on rising edges and out on DO on falling edges. Also used to generate clocks for A/D conversion.
DI	Data input. Digital input which contains serial data to program the MUX and channel assignments.
$\overline{CS}$	Chip select. Selects the chip for multiplexer and channel assignment and A/D conversion. When $\overline{CS}$ = 1, all digital outputs are in high impedance state. When $\overline{CS}$ = 0, normal A/D conversion takes place.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Current into V+ 15mA
Supply Voltage, V_{CC} 6.5V
Voltage
  Logic Inputs ..... –7 to V_{CC} +7V
  Analog Inputs ..... –0.3V to V_{CC} +0.3V
Input Current per Pin (Note 1) ..... ±25mA
Storage Temperature ..... –65°C to 150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 800mW

Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Dual-In-Line Package (Ceramic) ..... 300°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 4.5V_{DC} to 6.3V_{DC}
Temperature Range (Note 2) ..... T_{MIN} - T_A - T_{MAX}
  ML2280 BIP, ML2283 BIP ..... –40°C to 85°C
  ML2280 CIP, ML2283 CIP
  ML2280 BCP, ML2283 BCP ..... 0°C to 70°C
  ML2280 CCP, ML2283 CCP

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±10%, f_{CLK} = 1.333MHz, and $V_{REF/2}$ = 2.5V.

			ML228XB			ML228XC			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 3	MAX	MIN	TYP NOTE 3	MAX	UNITS
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
	Total Unadjusted Error	$V_{REF/2}$ = 2.5V $V_{REF/2}$ not connected (Notes 4, 6)			±1/2 ±2			±1 ±2	LSB LSB
	Reference Input Resistance	(Note 4)	10	15	20	10	15	20	kΩ
	Common-Mode Input Range	(Notes 4, 7)	GND –0.05		V_{CC} +0.05	GND –0.05		V_{CC} +0.05	V
	DC Common-Mode Error	Common mode voltage voltage GND to $V_{CC/2}$ (Note 5)		±1/16	±1/4		±1/16	±1/4	LSB
	AC Common-Mode Error	Common mode voltage GND to V_{CC}, 0 to 50kHz (Note 5)			±1/4			±1/4	LSB
	DC Power Supply Sensitivity	V_{CC} = 5V ±10% V_{REF} - V_{CC} +0.1V (Note 5)		±1/32	±1/4		±1/32	±1/4	LSB
	AC Power Supply Sensitivity	100mV_{P-P}, 25kHz sine on V_{CC} (Note 5)			±1/4			±1/4	LSB
	Change in Zero Error from V_{CC}=5V to Internal Zener Operation	15mA into V+ V_{CC} = N.C. $V_{REF/2}$ = 2.5V (Note 5)		±1/2			±1/2		LSB
V_Z	Internal Diode Regulated Break-down (at V+)	15mA into V+		6.9			6.9		V
V+	Input Resistance	(Note 4)	20	35		20	35		kΩ

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	ML228XB			ML228XC			UNITS
			MIN	TYP NOTE 3	MAX	MIN	TYP NOTE 3	MAX	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)									
I_{OFF}	Off Channel Leakage Current	On channel = V_{CC} Off channel = 0V (Notes 4, 8)	–1			–1			µA
		On channel = 0V Off channel = V_{CC} (Notes 4, 8)			+1			+1	µA
I_{ON}	On Channel Leakage Current	On channel = 0V Off channel = V_{CC} (Notes 4, 8)	–1			–1			µA
		On channel = V_{CC} Off channel = 0V (Notes 4, 8)			+1			+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage	(Note 4)	2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	(Note 4)			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = V_{CC}$ (Note 4)			1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V (Note 4)	–1			µA
$V_{OUT(1}$	Logical "1" Output Voltage	I_{OUT} = –2mA (Note 4)	4.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 2mA (Note 4)			0.4	V
I_{OUT}	HI-Z Output Current	V_{OUT} = 0V (Note 4) $V_{OUT} = V_{CC}$	–1		 1	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V (Note 4)	–6.5			mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$ (Note 4)			8.0	mA
I_{CC}	Supply Current	(Note 4)		1.3	2.5	mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
f_{CLK}	Clock Frequency	(Note 4)	10		1333	kHz
t_{ACQ}	Sample-and-Hold Acquisition			1/2		$1/f_{CLK}$
t_C	Conversion Time	Not including MUX adddressing time		8		$1/f_{CLK}$
SNR	Signal to Noise Ratio ML2280	V_{IN} = 40kHz, 5V sine. f_{CLK} = 1.333MHz ($f_{SAMPLING} \cong$ 120kHz). Noise is sum of all nonfundamental components up to 1/2 of $f_{SAMPLING}$ (Note 11)		47		dB
THD	Total Harmonic Distortion ML2280	V_{IN} = 40kHz, 5V sine. f_{CLK} = 1.333MHz ($f_{SAMPLING} \cong$ 120kHz). THD is sum of 2, 3, 4, 5 harmonics relative to fundamental (Note 11)		–60		dB
IMD	Intermodulation Distortion ML2280	$V_{IN} = f_A + f_B$. f_A = 40kHz, 2.5V sine. f_B = 39.8kHz, 2.5V Sine, f_{CLK} = 1.333MHz ($f_{SAMPLING} \cong$ 120kHz). IMD is $(f_A + f_B)$, $(f_A - f_B)$, $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, $(f_A - 2f_B)$ relative to fundamental (Note 11)		–60		dB
	Clock Duty Cycle	(Notes 4, 9)	40		60	%
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge	(Note 4)	130			ns
t_{HOLD}	Data Input Valid after CLK Rising Edge	(Note 4)	80			ns
t_{PD1}, t_{PD0}	CLK Falling Edge to Output Data Valid	C_L = 100pF (Note 4 & 10) Data MSB first Data LSB first		 90 50	 200 110	 ns ns
t_{1H}, t_{0H}	Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10pF, R_L = 10kΩ (see high impedance test circuits) (Note 5)		40	90	ns
		C_L = 100pF, R_L = 2kΩ (Note 5)		80	160	ns
C_{IN}	Capacitance of Logic Input			5		pF
C_{OUT}	Capacitance of Logic Outputs			5		pF

Note 1: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND < or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 2: 0°C to 70°C and –40°C to 85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% tested.

Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 6: Total unadjusted error includes offset, full-scale, linearity, multiplexer and sample-and-hold errors.

Note 7: For $V_{IN}-$ • $V_{IN}+$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of $4.950V_{DC}$ over temperature variations, initial tolerance and loading.

Note 8: Leakage current is measured with the clock not switching.

Note 9: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 300ns. The maximum time the clock can be high or low is 60µs.

Note 10: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time..

Note 11: Because of multiplexer addressing, test conditions for the ML2283 is V_{IN} = 30kHz, 5V sine ($f_{SAMPLING}$ ♠ 89kHz)

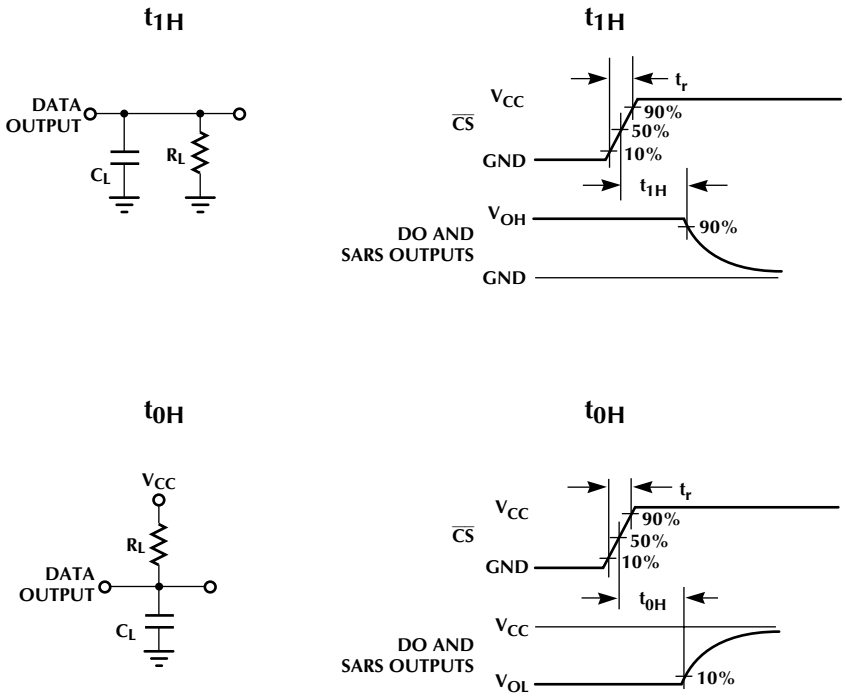


Figure 1. High Impedance Test Circuits and Waveforms

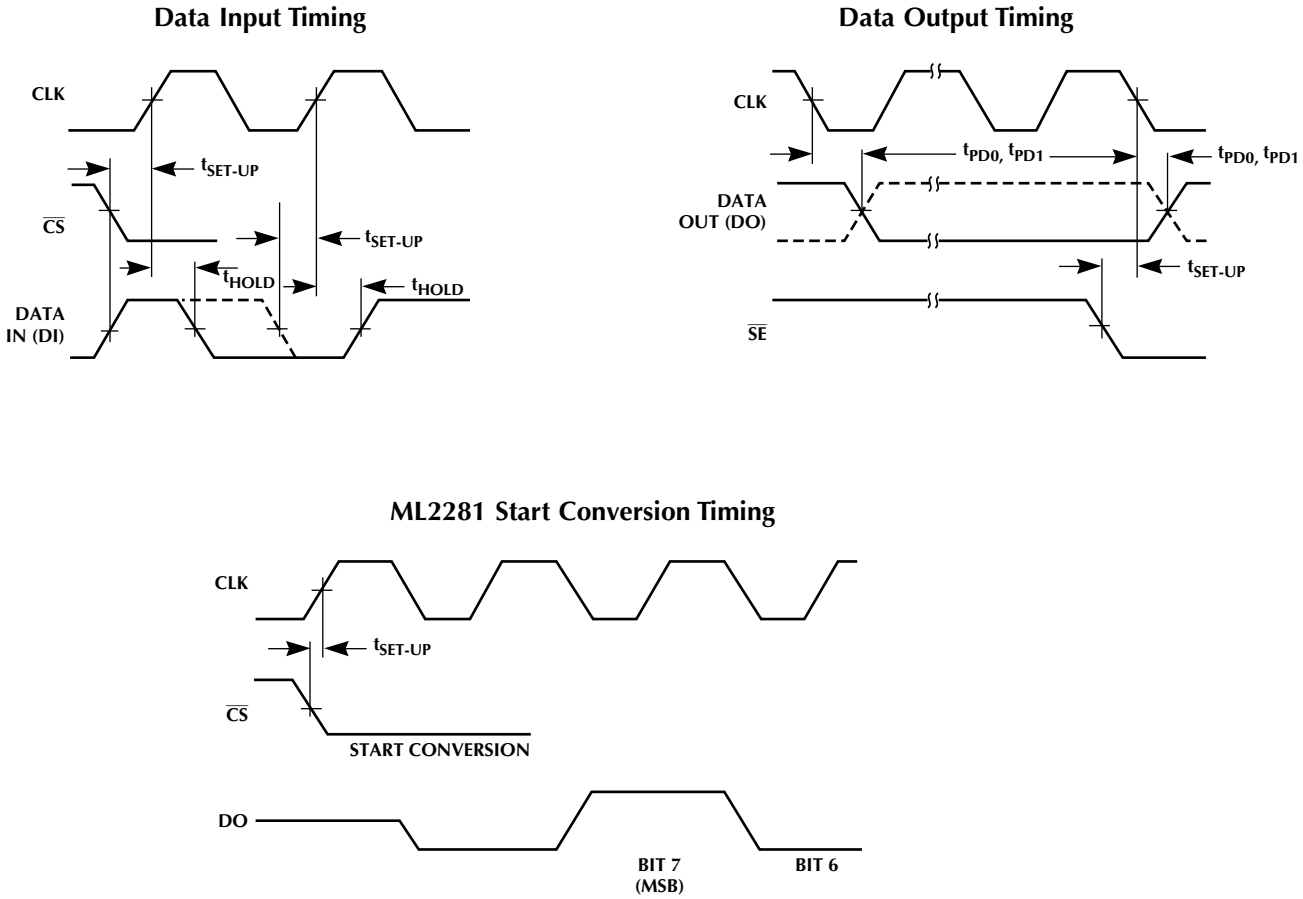
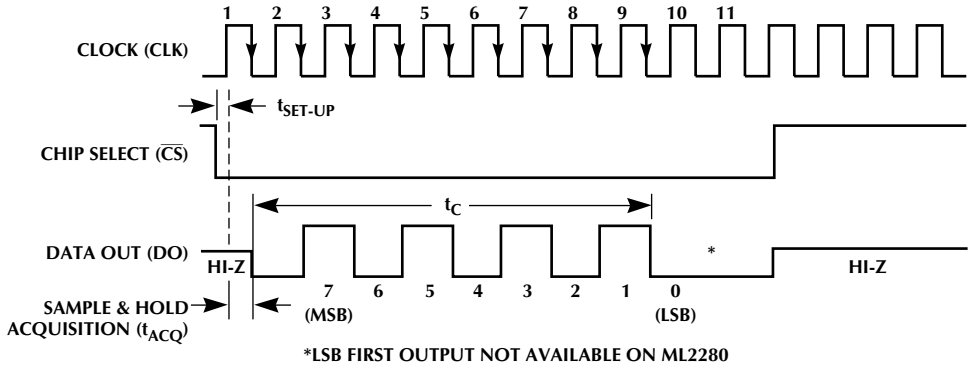


Figure 2. Timing Diagrams

ML2280 Timing



*LSB FIRST OUTPUT NOT AVAILABLE ON ML2280

ML2283 Timing

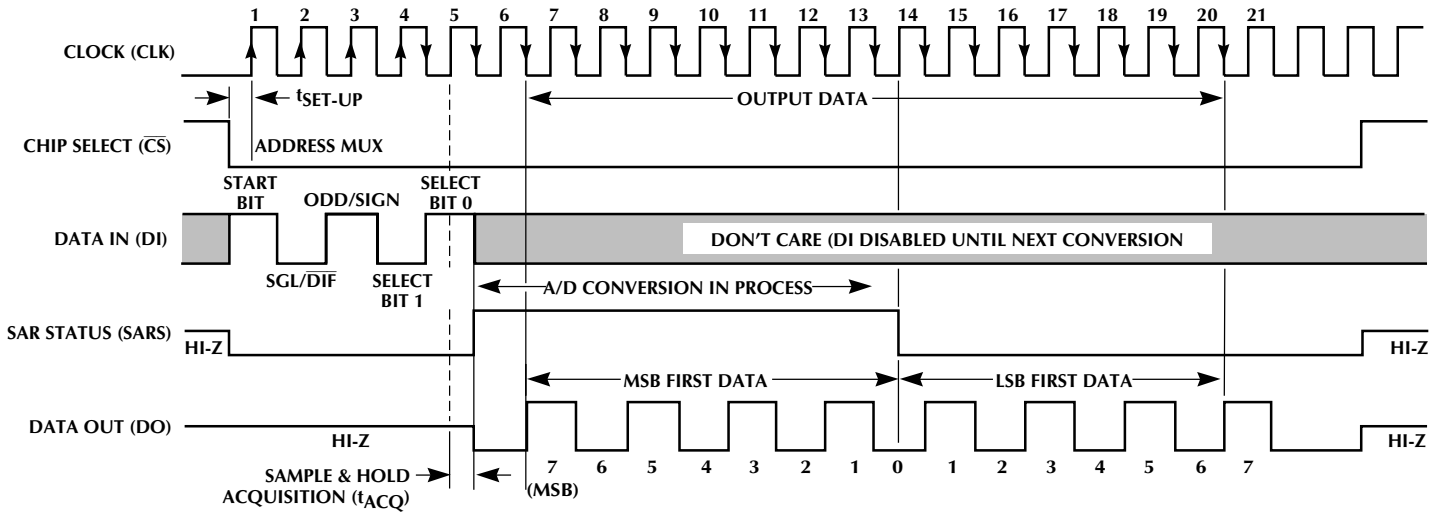


Figure 2. Timing Diagrams (Continued)

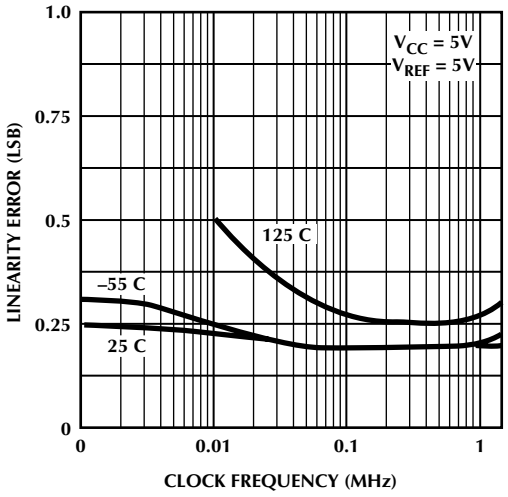


Figure 3. Linearity Error vs f_{CLK}

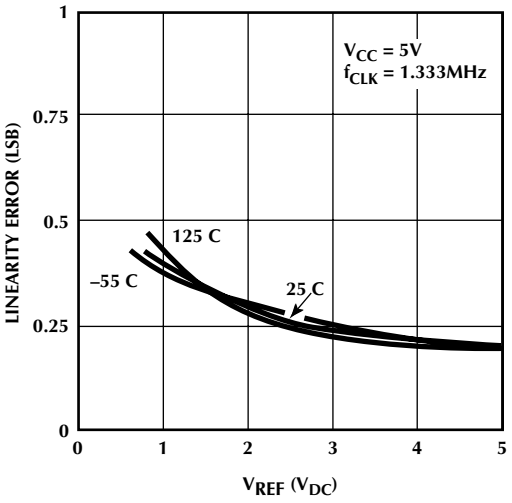


Figure 4. Linearity Error vs V_{REF} Voltage

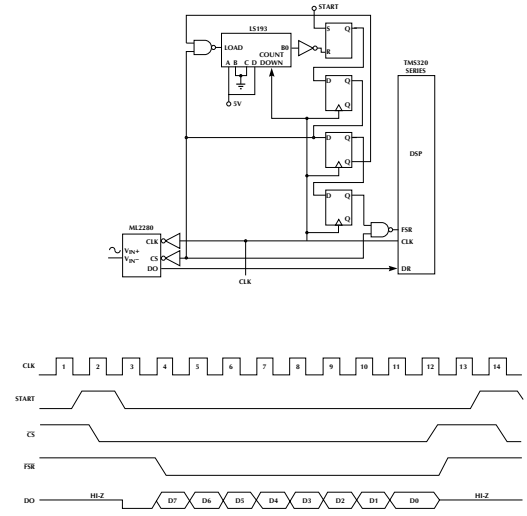


Figure 5. Unadjusted Offset Error vs V_{REF} Voltage

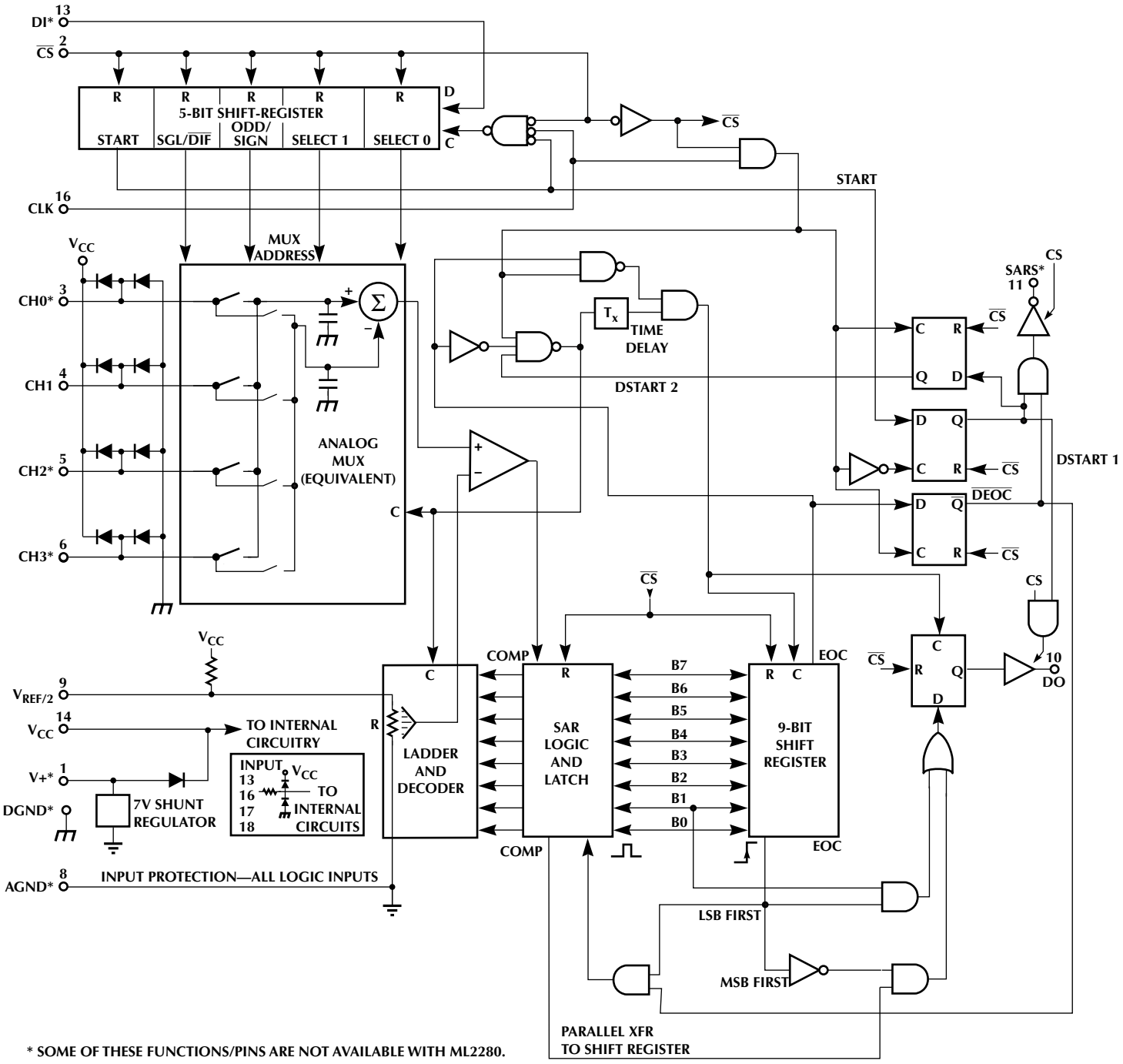


Figure 6. ML2288 Functional Block Diagram

FUNCTIONAL DESCRIPTION

MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "–" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "–" input, the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software configurable single ended, differential, or pseudo differential options.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single ended or differential. In the differential case, it also assigns the polarity of the analog channels. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a different pair but channel 0 or channel 1 cannot act differentially with any other channel. In addition to selecting the differential mode, the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is illustrated by the MUX addressing codes shown in Table 1.

The MUX address is shifted into the converter via the DI input. Since the ML2280 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. Figure 7 illustrates these different input modes.

DIGITAL INTERFACE

The block diagram and timing diagrams in Figures 2-5 illustrate how a conversion sequence is performed.

A conversion is initiated when $\overline{CS}$ is pulsed low. This line must me held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

A clock is applied to the CLK input. On each rising edge of the clock, the data on DI is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on the DI input (all leading edge zeros are ignored). After the start bit, the device clocks in the next 2 to 4 bits for the MUX assignment word.

SINGLE-ENDED MUX MODE

MUX ADDRESS			CHANNEL#			
SGL/$\overline{DIF}$	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to AGND

DIFFERENTIAL MUX MODE

MUX ADDRESS			CHANNEL#			
SGL/$\overline{DIF}$	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	–		
0	0	1			+	–
0	1	0	–	+		
0	1	1			–	+

Table 1. ML2283 MUX Addressing 4 Single-Ended or 2 Differential Channel

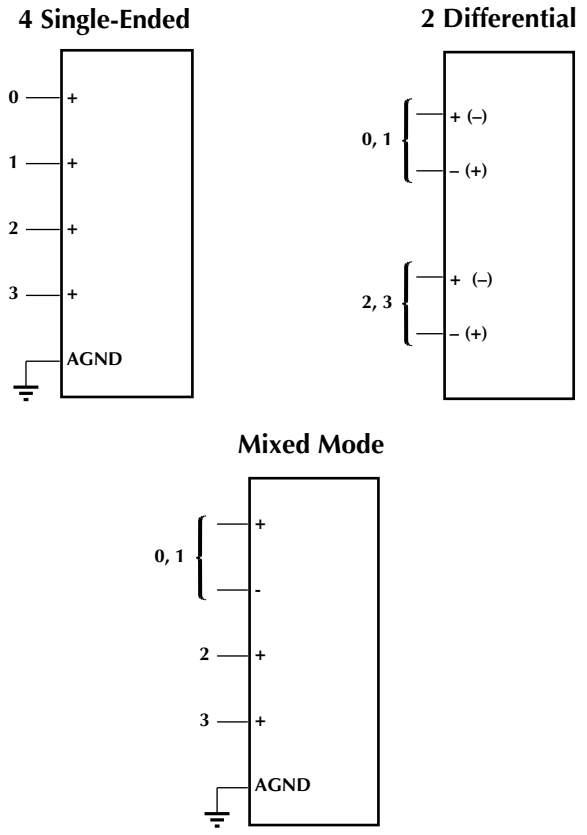


Figure 7. Analog Input Multiplexer Functional Options for ML2288

When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1/2 clock period is used for sample & hold settling through the selected MUX channels. The SAR status output goes high at this time to signal that a conversion is now in progress and the DI input is ignored.

The DO output comes out of High impedance and provides a leading zero for this one clock period.

When the conversion begins, the output of the comparator, which indicates whether the analog input is greater than or less than each successive voltage from the internal DAC, appears at the DO output on each falling edge of the clock. This data is the result of the conversion being shifted out (with MSB coming first) and can be read by external logic or µP immediately.

After 8 clock periods, the conversion is completed. The SAR status line returns low to indicate this 1/2 clock cycle later.

The serial data is always shifted out MSB first during the conversion. After the conversion has been completed, the data can be shifted out a second time with LSB first. The 2280 data is shifted out only once, MSB first.

All internal registers are cleared when the $\overline{CS}$ input is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI input and DO output can be tied together and controlled through a bidirectional µP I/O bit with one connection. This is possible because the DI input is only latched in during the MUX addressing interval while the DO output is still in the high impedance state.

REFERENCE

The ML2280 and ML2283 are intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, see the ML2281 and ML2284 which have a V_{REF} input that can be tied to V_{CC}.

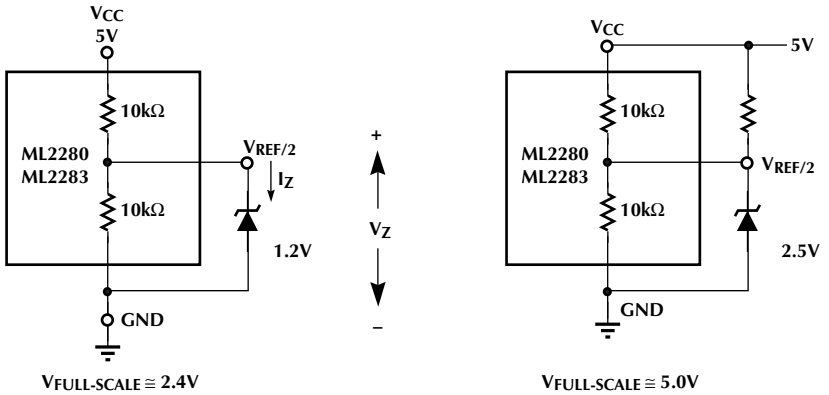
The voltage applied to the $V_{REF/2}$ pin defines the voltage span of the analog input (the difference between VIN+ and VI_{N-}) over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+"input and "–" input is approximately twice the voltage at the $V_{REF/2}$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256\left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF/2})}\right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF/2}$ is the voltage to ground.

The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 10kΩ) connected from V_{CC} to ground. Total ladder input resistance is the parallel combination of these two equal resist. As show in Figure 8, a reference diode requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF/2}$ can be quite small (See Typical Performance Curves) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1LSB equals $V_{REF/256}$).



NOTE: NO EXTERNAL BIASING RESISTOR NEENED IF: $V_Z < \frac{V_{CC}}{2}$ AND I_Z min. $< \frac{V_{CC/2} - V_Z}{5k\Omega}$

Figure 8. Reference Biasing

ANALOG INPUTS AND SAMPLE/HOLD

An important feature of the ML2280 and ML2283 is that they can be located at the source of the analog signal and then communicate with a controlling µP with just a few wires. This avoids bussing the analog inputs long distances and thus reduces noise pickup on these analog lines. However, in some cases, the analog inputs have a large common mode voltage or even some noise present along with the valid analog signal.

The differential input of these converters reduces the effects of common mode input noise. Thus, if a common mode voltage is present on both "+" and "–" inputs, such as 60Hz, the converter will reject this common mode voltage since it only converts the difference between "+" and "–" inputs.

The ML2280 and ML2283 have a true sample and hold circuit which samples both "+" and "–" inputs simultaneously. This simultaneous sampling with a true S/H will give common mode rejection and AC linearity performance that is superior to devices where the two input terminals are not sampled at the same instant and where true sample and hold capability does not exist. Thus, these A/D converters can reject AC common mode signals from DC-50kHz as well as maintain linearity for signals from DC-50kHz.

The signal at the analog input is sampled during the interval when the sampling switch is closed prior to conversion start. The sampling window (S/H acquisition time) is 1/2 CLK period wide and occurs 1/2 CLK period before DO goes from high impedance to active low state. When the sampling switch closes at the start of the S/H acquisition time, 8pF of capacitance is thrown onto the analog input. 1/2 CLK period later, the sampling switch is opened and the signal present at the analog input is stored. Any error on the analog input at the end of the S/H acquisition time will cause additional conversion error. Care should be taken to allow adequate charging or settling time from the source. If more charging or settling time is needed to reduce these analog input errors, a longer CLK period can be used.

For latchup immunity each analog input has dual diodes to the supply rails, and a minimum of ±25mA (±100mA typically) can be injected into each analog input without causing latchup.

ZERO ERROR ADJUSTMENT

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN\ MIN}$ is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing any V_{IN}– input at this $V_{IN\ MIN}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN}– input and applying a small magnitude positive voltage to the V_{IN}+ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal 1/2 LSB value (1/2 LSB = 9.8mV for V_{REF} = 5.000V_{DC}).

FULL-SCALE ADJUSTMENT

The full-scale adjustment can be made by applying a differential input voltage which is 1-1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 11111110 to 11111111.

ADJUSTMENT FOR AN ARBITRARY ANALOG INPUT VOLTAGE RANGE

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN}+ voltage which equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "–" input should then be adjusted to just obtain the 00000000 to 00000001 code transition.

The full-scale adjustment should be made by forcing a voltage to the V_{IN}+ input which is given be:

$$V_{IN} + \text{fs adjust} = V_{MAX} - 1.5 \times \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where V_{MAX} = high end of the analog input range
V_{MIN} = low end (offset zero) of the analog range
The V_{REF} or V_{CC} voltage is then adjusted to provide a code change from 11111110 to 11111111.

SHUNT REGULATOR

A unique feature of the ML2283 is the inclusion of a shunt regulator connected from V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode as shown in Figure 8. When the regulator is turned on, the V+ voltage is clamped at $11V_{BE}$ set by the internal resistor ratio. The typical I-V of the shunt regulator is shown in Figure 9.

It should be noted that before V+ voltage is high enough to turn on the shunt regulator (which occurs at about 5.5V), 35kΩ resistance is observed between V+ and GND. When the shunt regulator is not used, V+ pin should be either left floating or tied to GND. The temperature coefficient of the regulator is –22mV/°C.

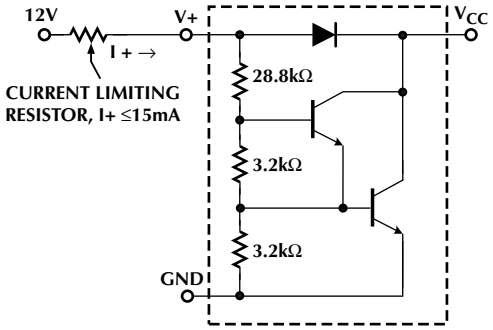


Figure 9. Shunt Regulator

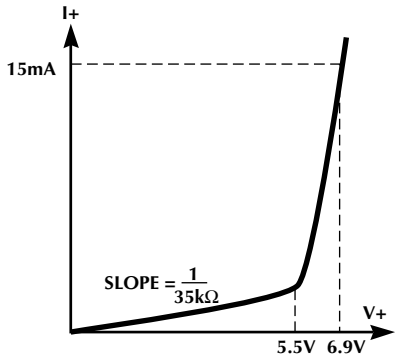
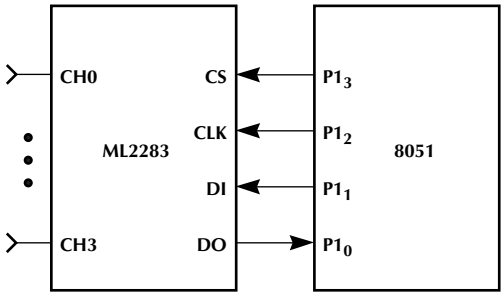


Figure 10. I-V Characteristic of the Shunt Regulator

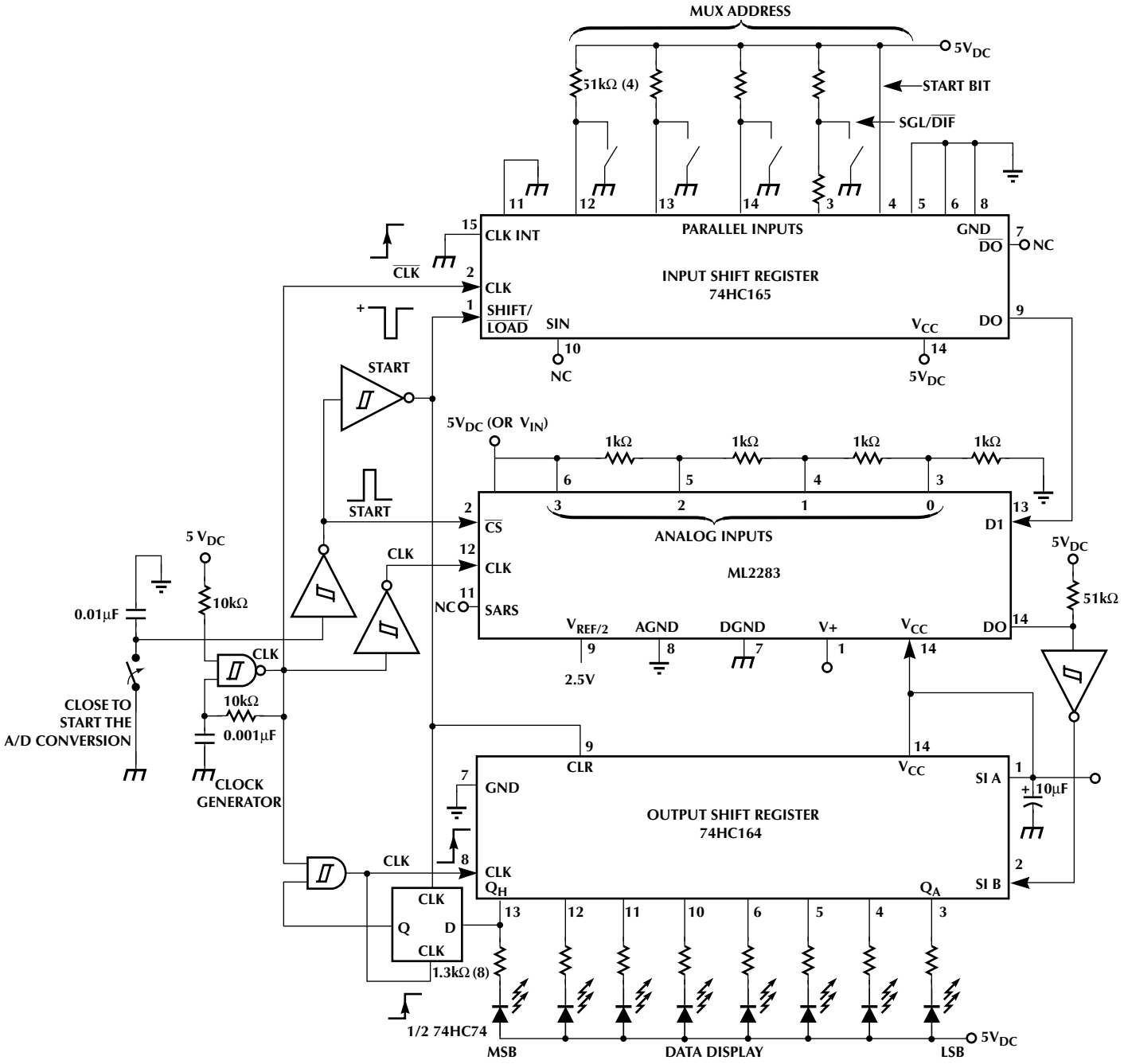
APPLICATIONS



8051 Interface and Controlling Software

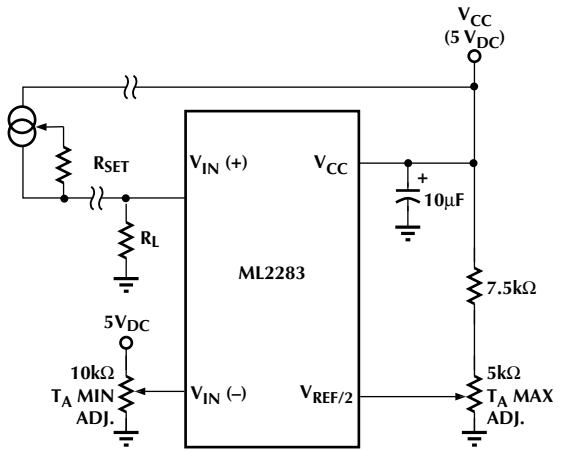
MNEMONIC			INSTRUCTION
START:	ANL	P1, #0F7H	;SELECT A/D (CS = 0)
	MOV	B, #5	;BIT COUNTER ♦ 5
	MOV	A, #ADDR	;A ♦ MUX BIT
LOOP 1:	RRC	A	;CY ♦ ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ♦ 0
	SJMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;D1 ♦ 1
CONT:	ACALL	PULSE	;PULSE SK 0 ∅ 1 ∅ 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	ACALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ♦ 8
LOOP 2:	ACALL	PULSE	;PULSE SK 0 ∅ 1 ∅ 0
	MOV	A, P1	;CY ♦ DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ♦ RESULT
	RLC	A	;A(0) BIT ♦ AND SHIFT
	MOV	C, A	;C ♦ RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETI			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ♦ 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ♦ 0
	RET		

APPLICATIONS (Continued)

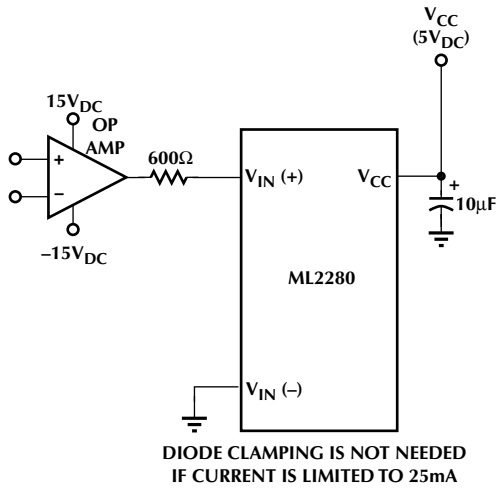


ML2283 "Stand-Alone" or Evaluation Circuit

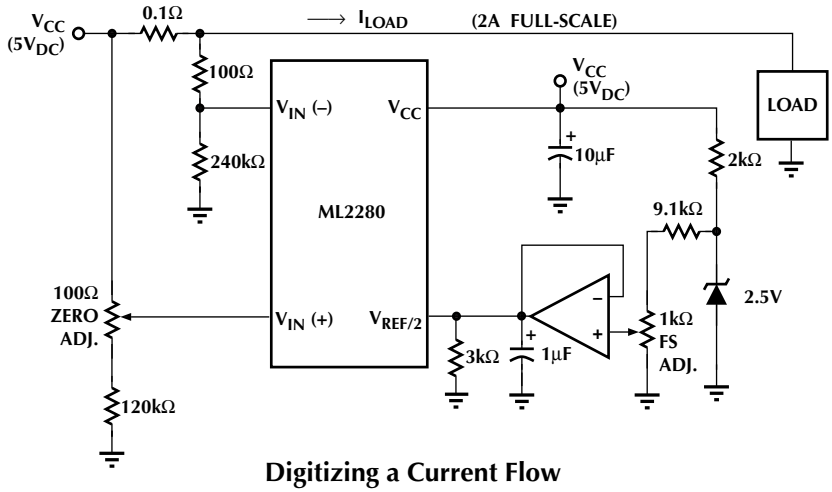
APPLICATIONS (Continued)



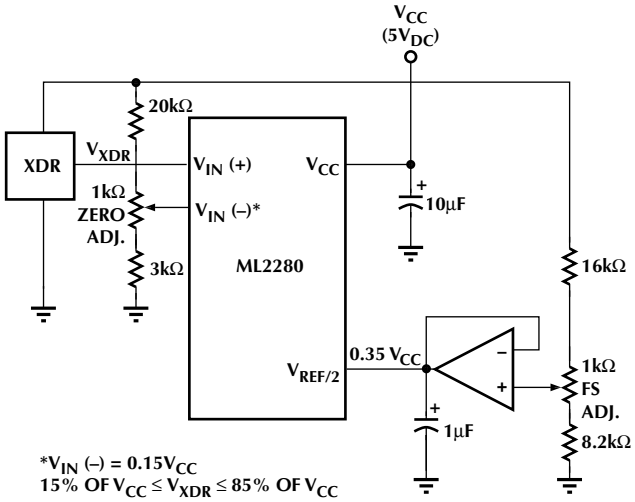
Low-Cost Remote Temperature Sensor



Protecting the Input

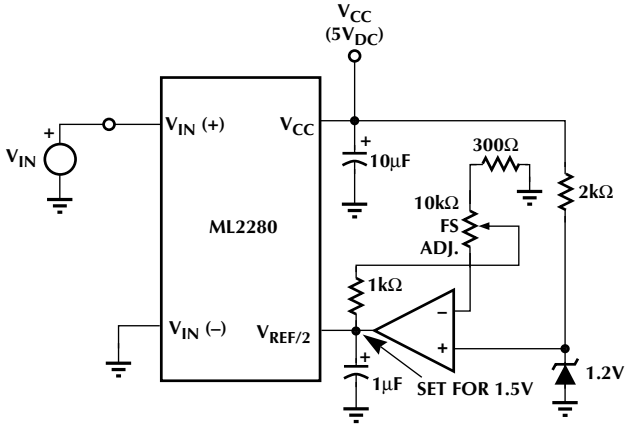


Digitizing a Current Flow

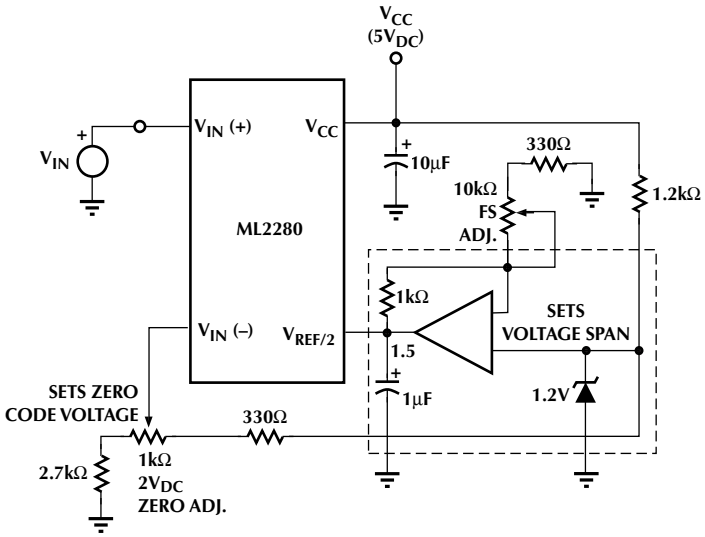


Operating with Ratiometric Transducers

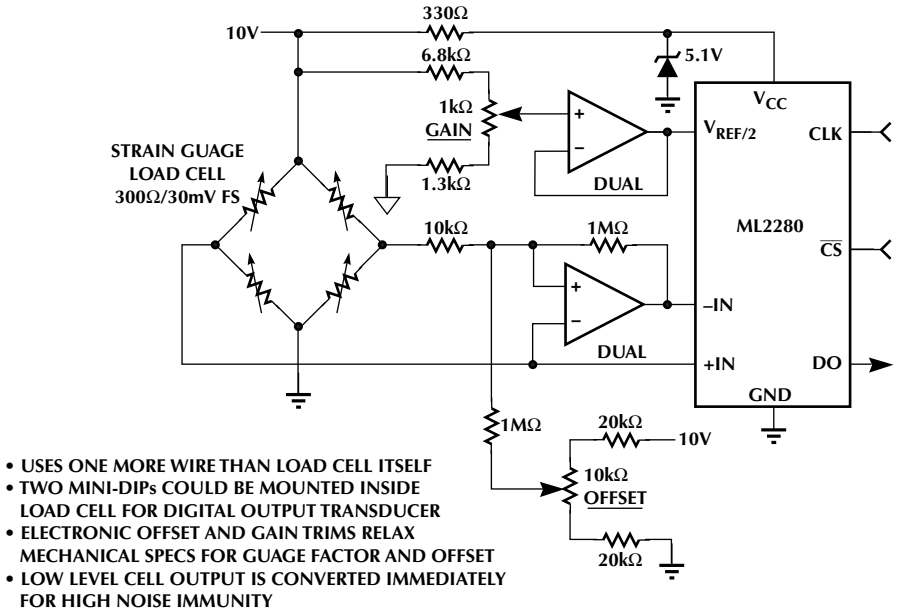
APPLICATIONS (Continued)



Span Adjust: 0V - V_{IN} - 3V



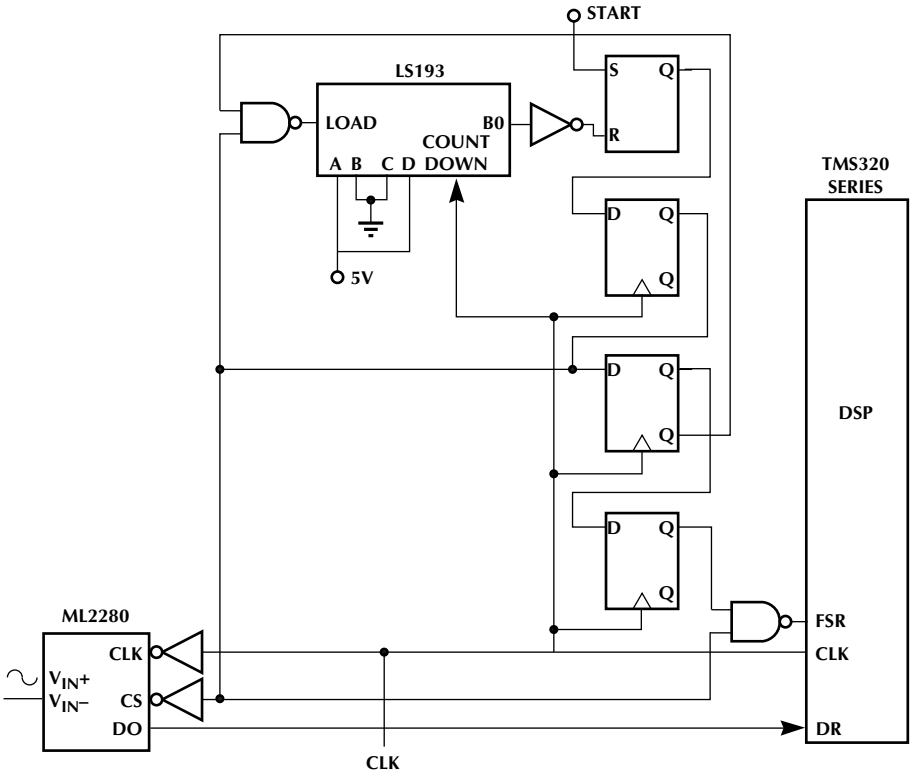
Zero-Shift and Span Adjust: 2V - V_{IN} - 5V



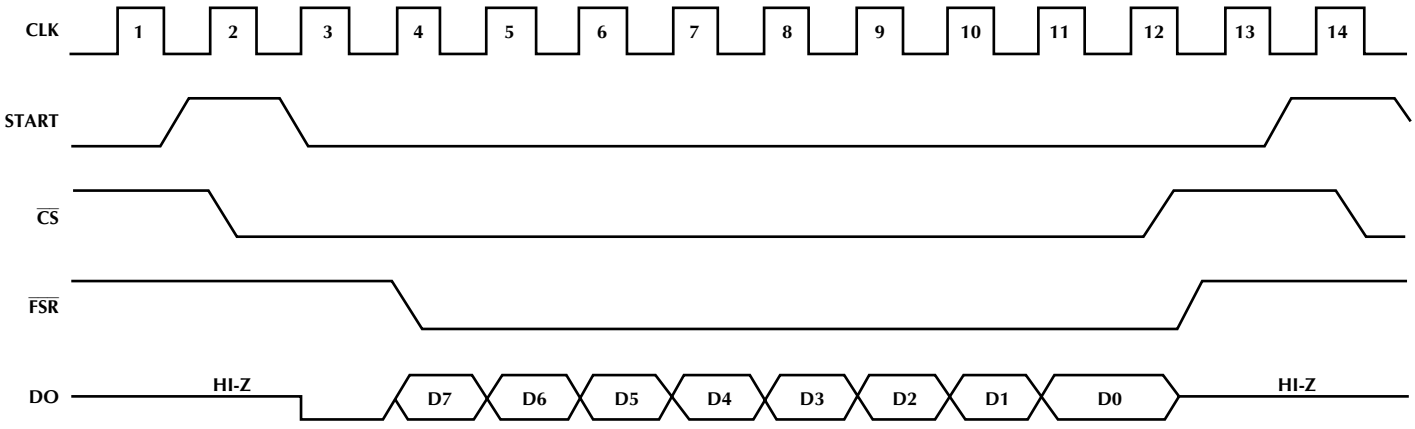
- USES ONE MORE WIRE THAN LOAD CELL ITSELF
- TWO MINI-DIPs COULD BE MOUNTED INSIDE LOAD CELL FOR DIGITAL OUTPUT TRANSDUCER
- ELECTRONIC OFFSET AND GAIN TRIMS RELAX MECHANICAL SPECS FOR GUAGE FACTOR AND OFFSET
- LOW LEVEL CELL OUTPUT IS CONVERTED IMMEDIATELY FOR HIGH NOISE IMMUNITY

Digital Load Cell

APPLICATIONS (Continued)



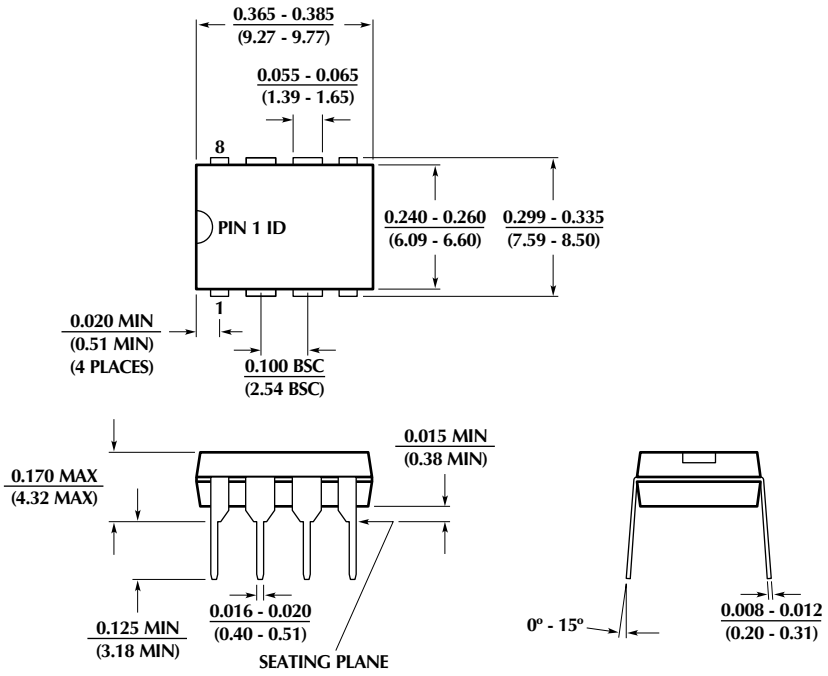
Sampling Rate 111kHz, Data Rate 1.33MHz



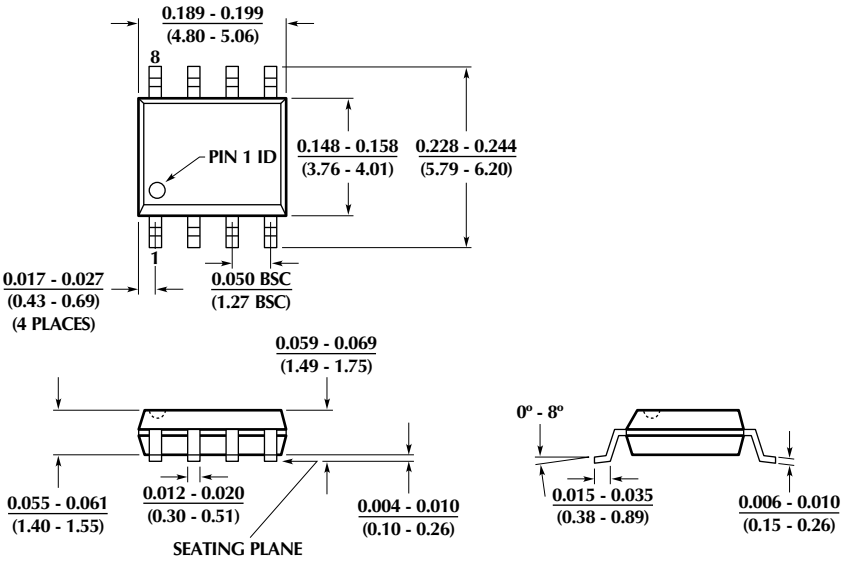
Interfacing ML2280 to TMS320 Series

PHYSICAL DIMMENSIONS inches (millimeters)

Package: P08
8-Pin PDIP

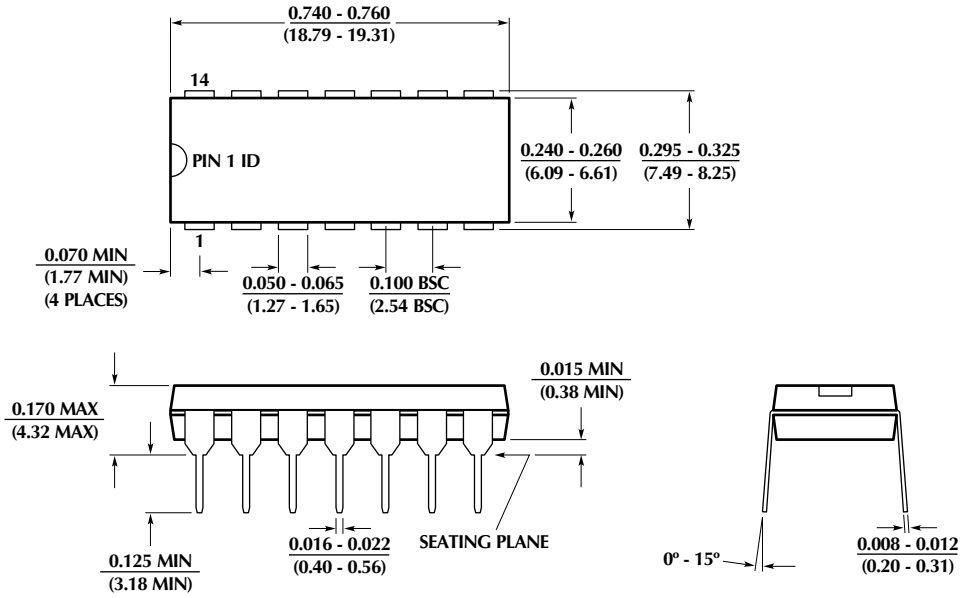


Package: S08
8-Pin SOIC



PHYSICAL DIMMENSIONS inches (millimeters)

Package: P14
14-Pin PDIP



ORDERING INFORMATION

PART NUMBER	ALTERNATE PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
SINGLE ANALOG INPUT, 8-PIN PACKAGE				
ML2280BIP (Obs)		±1/2 LSB	–40°C to 85°C	8-Pin DIP (P08)
ML2280BIS (Obs)			–40°C to 85°C	8-Pin SOIC (S08)
ML2280BCP (Obs)			0°C to 70°C	8-Pin DIP (P08)
ML2280BCS (Obs)			0°C to 70°C	8-Pin SOIC (S08)
ML2280CIP (Obs)		±1 LSB	–40°C to 85°C	8-Pin DIP (P08)
ML2280CIS (Obs)			–40°C to 85°CQ	8-Pin SOIC (S08)
ML2280CCP (Obs)			0°C to 70°C	8-Pin DIP (P08)
ML2280CCS (Obs)			0°C to 70°C	8-Pin SOIC (S08)
TWO ANALOG INPUTS, 14-PIN PACKAGE				
ML2283BIP (Obs)	ADC0833CCN	±1/2 LSB	–40°C to 85°C	14-Pin DIP (P014)
ML2283BCP (Obs)	ADC0833BCN		0°C to 70°C	14-Pin DIP (P014)
ML2283CIP (Obs)	ADC0833BCN	±1 LSB	–40°C to 85°C	14-Pin DIP (S014)
ML2283CCP (EOL)	ADC0833CCN		0°C to 70°C	14-Pin DIP (P014)

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2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295