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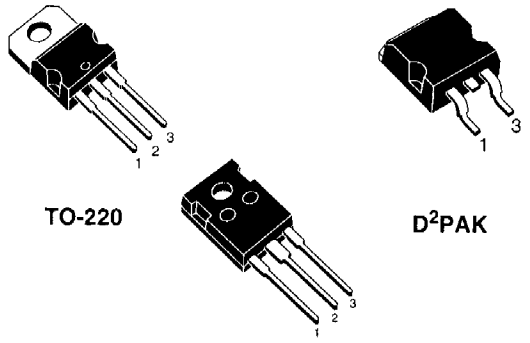
STP12NK80Z - STB12NK80Z
STW12NK80Z

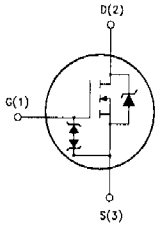
N-CHANNEL 800V - 0.65Ω - 10.5A TO-220 / D²PAK / TO-247
Zener-Protected SuperMESH™Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W
STB12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W
STW12NK80Z	800 V	< 0.75 Ω	10.5 A	190 W

- TYPICAL $R_{DS}(on)$ = 0.65 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY



INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS
- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	800	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	10.5	A
I_D	Drain Current (continuous) at T_C = 100°C	6.6	A
I_{DM} (•)	Drain Current (pulsed)	42	A
P_{TOT}	Total Dissipation at T_C = 25°C	190	W
	Derating Factor	1.51	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \leq 10.5A$, di/dt ≤200A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220/ D²PAK	TO-247	
Rthj-case	Thermal Resistance Junction-case Max	0.66		°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	50	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	10.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	400	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 5.25 A		0.65	0.75	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 5.25 A		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2620 250 53		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 640V		100		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 400 V, I_D = 5.25 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		30 18		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 640V, I_D = 10.5 A, V_{GS} = 10V		87 14 44		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 400 V, I_D = 5.25 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		70 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 640 V, I_D = 10.5 A, R_G = 4.7Ω, V_{GS} = 10V (Inductive Load see, Figure 5)		16 15 28		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				10.5 42	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 10.5 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 10.5 A, di/dt = 100A/µs V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 5)		635 5.9 18.5		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.