AN2871
Application note

SPC560Pxx/SPC56APxx HW design guideline

Introduction

This application note is intended for hardware designers. It gives hardware design references on SPC560Pxx/SPC56APxx microcontroller. Four topics are covered:

- Voltage Regulator (VREG)
- Main oscillator
- Supply pins
- Reference Reset circuit

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1 Overview

SPC560Pxx/SPC56APxx microcontrollers are members of a family of microcontrollers built on Power Architecture® technology. The device is supplied externally with a single voltage supply, which can be either 5 V or 3.3 V depending on application requirements. Internally, the chip operates with two supply voltages, namely the main supply (5 V or 3.3 V) and the core logic supply (1.2 V).

2 On-chip voltage regulator (VREG)

The SPC560Pxx device can be supplied with 5 V ±10% or 3.3 V ± 10 % (4.5 – 5.5 V or 3.0 – 3.6 V, respectively) to suit different applications. Additionally, the on-chip linear voltage regulator generates a reference voltage enabling the regulation of the 1.2 V via an external ballast transistor (with a specified tolerance 1.15 – 1.32 V) from the external 3.3 V/5 V voltage supply ($V_{DD_HV_REG}$ supply pin).

The on-chip voltage regulator module provides the following features:

- Uses external NPN (Negative-Positive-Negative) transistor
- Regulates external 3.3 V–5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2.1 VREG design guideline

2.1.1 Voltage regulator

The on-chip voltage regulator module regulates the external 3.3 V–5.0 V supply down to 1.2 V for the core logic. The nominal target output is 1.2 V. Due to variations the actual output will be in the range of 1.15–1.32 V in the full current load range (0–200 mA) after factory trimming.

The internal voltage regulator requires an external NPN ballast transistor, approved transistor list available in *Table 1*, to be connected as shown in *Figure 1* for SPC560P40xx, SPC560P60xx/SPC56AP60xx and *Figure 2* for SPC560P50xx. Capacitances, CDEC1, CDEC2,CDEC3, should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than LREG as described in the device datasheet.

The device cannot be used with an external 1.2 V supply. Always use the external ballast transistor to generate the 1.2 V supply to the core.

Figure 1. External NPN ballast connections configuration for SPC560P60xx/SPC56AP60xx/SPC560P40xx

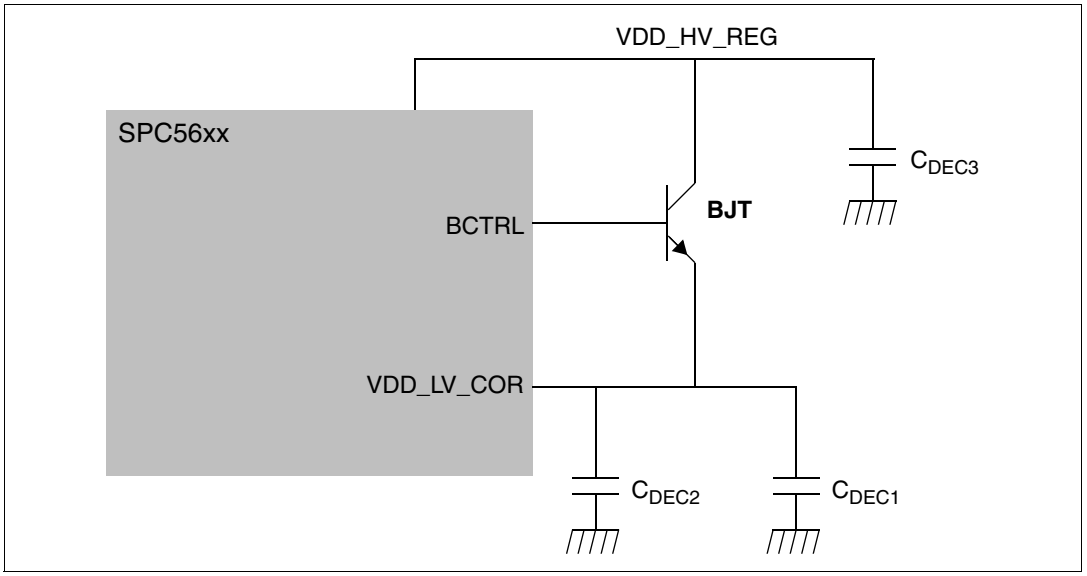
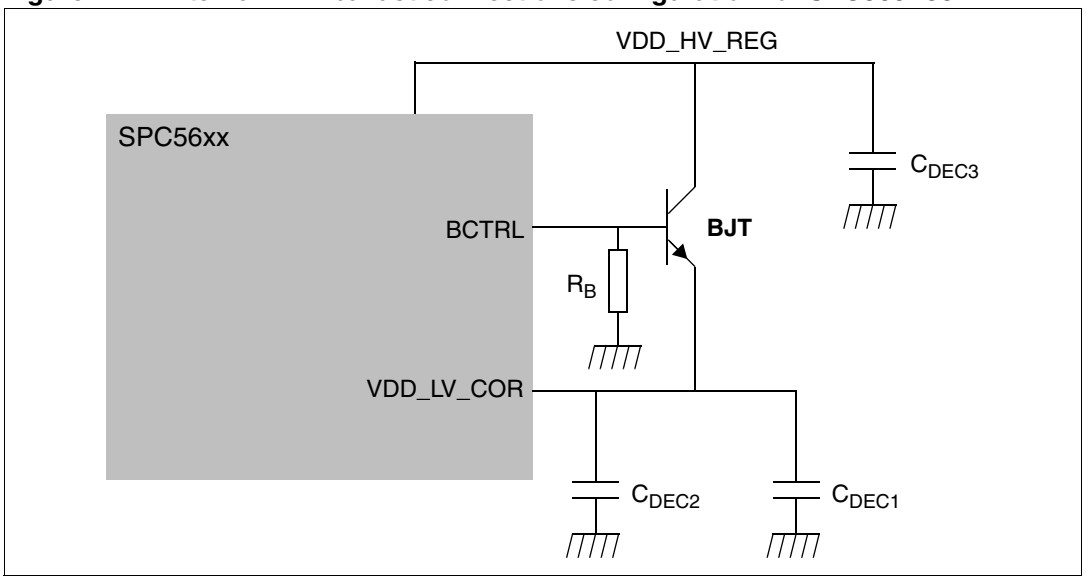


Figure 2. External NPN ballast connections configuration for SPC560P50xx



2.1.2 Circuit architecture

The VREG circuit is a classic emitter-follower configuration controlled voltage source. The stabilization of the output voltage is achieved using an external capacitance of several µF (see *Section 4*).

The BCTRL (voltage regulator external NPN ballast base control pin) controls the current on the base of the transistor. Current is increased to raise the voltage on V_{DD}. Current is decreased to lower the voltage. The gain of the transistor controls the maximum current available on V_{DD} from the supply.

The gain should be high enough to allow start-up and low enough to prevent the VREG becoming instable.

2.1.3 Recommended transistors

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Moreover, the datasheet values are usually given at room temperature.

The required gain should be calculated at cold temperature, because a bipolar transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor manufacturer or can be estimated using the graphs given in the transistor datasheet.

The *Table 1* lists the recommended ballast transistors.

Table 1. Approved NPN ballast transistor

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10;BCX68-16;BCX68-25
BC868	NXP	BC868
BC817	Infineon	BC817-16;BC817-25;BC817SU;
	NXP	BC817-16;BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10;BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10;BCP56-16

1. For automotive applications please check with the appropriate transistor vendor for automotive grade certification

In the following, as example, are shown parameters of BCP68 and BC817 transistors.

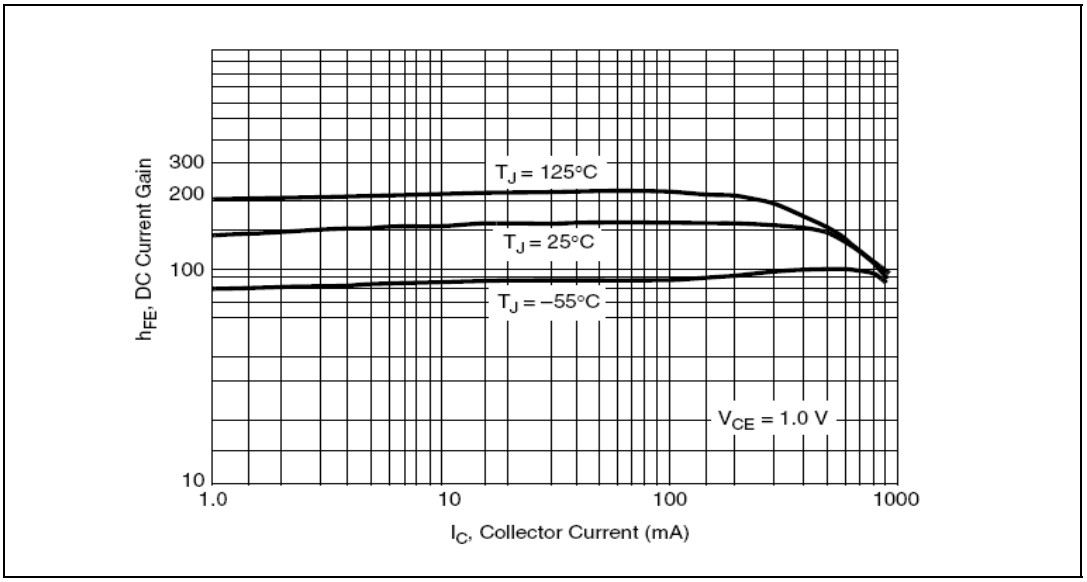
BCP68 NPN bipolar 1 A/1.5 W SOT223

This transistor is available from several semiconductor makers.

Table 2. ON Semiconductor datasheet: BCP68 electrical characteristics at 25 °C

Symbol		Parameter	Min	Typ	Max	Unit
h_{FE}	—	DC current gain I_C = 5.0 mA; V_{CE} = 10 V_{DC} I_C = 150 mA; V_{CE} = 1 V_{DC} I_C = 1.0 mA; V_{CE} = 1 V_{DC}	 50 85 60	 — — —	 — 375 —	—

Figure 3. ON Semiconductor BCP68 datasheet: example of temperature response



For the example datasheet, the minimum gain at room temperature is 85. At –40 °C, the transistor has an estimated gain of 54.

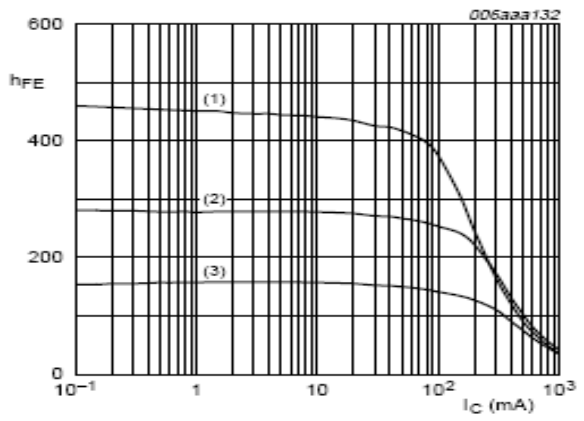
BC817-25 NPN bipolar 0.5A SOT23

This transistor is available from several semiconductor maker.

Table 3. NXP datasheet: BC817-25 electrical characteristics at 25 °C

Symbol		Parameter	Min	Typ	Max	Unit
h_{FE}	—	DC current gain I_C = 100 mA; V_{CE} = 1 V_{DC} I_C = 500 mA; V_{CE} = 1 V_{DC}	 160 40	 — —	 400 —	 —

Figure 4. Example of temperature response from NXP BC817-25



V_{CE} = 1 V.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –55 °C.

Note: The BC817-16 variant is also compatible with the SPC560Px voltage regulator.

BCX68-25 NPN bipolar 0.5 A SOT89

This transistor is available from several semiconductor makers.

Table 4. Zetex datasheet: BCX68-25 electrical characteristics at 25 °C

Symbol		Parameter	Min	Typ	Max	Unit
h_{FE}	—	DC current gain I_C = 500 mA; V_{CE} = 1 V_{DC}	160	—	400	—

Note: BCX68-16 and BCX68-10 variants are also compatible with the SPC560Px voltage regulator.

Summary of proposed ballast transistors

The transistors list of *Table 1* has been validated by simulations. To offer several options to ECU designers, various packages are proposed:

- SOT223 for BCP68
- SOT89 for BCX68-25, BCX68-16, and BCX68-10
- SOT23 for BC817-25 and BC817-16

Please note that the SOT23 package has a high thermal resistance and is not suited for the full automotive temperature range.

BC817-25 is also offered in the SC74 package, which has a better thermal resistance but that still does not allow using this transistor in the full temperature range.

The SOT23 and SC74 packages should be considered for applications such as airbags.

External transistor power dissipation

The power dissipation required by the bypass transistor is dependent upon the voltage drop across it, the core current and the selected supply range.

The worst case power dissipation of the ballast transistor is with a 5 V supply. Assuming the CPU draws 100 mA (please check figure according to your configuration in the latest SPC560Pxx/SPC56APxx datasheet), the worst case voltage drop with 5 V +10% supply is 4.35 V (that is, 5.5 V – 1.15 V = 4.35 V). This leads to about 0.435 W of power dissipation.

Ballast transistor junction temperature

The ballast transistor maximum junction temperature is typically 150 °C, although in some transistors it may be as high as 165 °C.

Depending on the maximum ambient temperature, the ballast transistor may have a limited allowed temperature rise and thus requires adequate heatsinking. Thermal characteristics of the board and heatsink are required for this calculation.

Ballast transistor VCEsat

To reduce the power dissipation in the transistor, it is permissible to add a series resistor that will drop the collector voltage. If this is used, the saturation voltage becomes significant; the transistor must remain out of saturation with the minimum expected supply (5.0 V or 3.3 V) and the maximum expected Vcore rail (that is, 1.32 V).

Ballast transistor inductance

The distance from the ballast transistor's heatsink rail to the microcontroller will lead to inductance in the system (the greater the distance, the higher the inductance). The location of the transistor will also affect the inductance, due to the lengths of the 1.2 V traces and of the BCTRL signal. Those inductances will reduce the phase margin. It is recommended that the inductance on BCTRL and on 1.2 V is kept below 15 nH.

Due to variations in board type, specific details on trace length specification cannot be provided; consequently, inductance values have been given.

Calculation examples

Note: The following examples demonstrate how ballast transistors can be selected and how chip junction temperature can be estimated. The data used in the examples are fictional and should not be taken as specifications for particular systems. For specific calculations, please refer to the device datasheet.

Example 1: SPC560P50, 64 MHz in motor control mode

- Power
  Maximum steady state MCU current: 100 mA
  Maximum collector voltage 5.0 V + 10% = 5.5 V
  Minimum emitter voltage: = 1.15 V
  Required power = (5.5 V – 1.15 V) * 0.1 = 435 mW
  Proposed transistor: BCP68 in SOT223
- Temperature
  Target system ambient = 125 °C
  SOT223 T_{JC} junction-to-case = 17 °C/W
  FR4 with thermal vias for SOT223 = 12 °C/W
  Heatsink to ambient + 3 °C (depends upon power loading in target system)
  Junction temperature = (125 °C + 3 °C) + (12 °C/W + 17 °C/W) * 0.442 W = 141 °C

Example 2: SPC560P50, 64 MHz in airbag mode

- Power
  Maximum steady state MCU current: 66 mA
  Maximum collector voltage 3.3 V + 10% = 3.6 V
  Minimum emitter voltage: = 1.15 V
  Required power = (3.6 V – 1.15 V) * 0.066 = 162 mW
  Proposed transistor: BCP68 in SOT223
- Temperature
  Target system ambient = 105 °C
  SOT223 T_{JC} junction-to-case = 17 °C/W
  FR4 with thermal vias for SOT223 = 12 °C/W
  Heatsink to ambient + 3 °C (depends upon power loading in target system)
  Junction temperature = (105 °C + 3 °C) + (12 °C/W + 17 °C/W) * 0.131 W = 112 °C

2.2 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz input clock. Furthermore, the FMPLL supports programmable frequency modulation of the system clock.

The PLL has the following major features:

- Input clock frequency from an 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation
- Input supply same as core supply: 1.2 V

FMPLL supply is shorted with core, without impact on jitter.

At least a couple of 470 pF and 440 nF ceramic capacitors should be placed between the $V_{DD_LV_COR3}/V_{SS_LV_COR3}$ pair ($V_{DD_LV_COR0}/V_{SS_LV_COR0}$ for SPC560P40xx).

3 Main oscillator

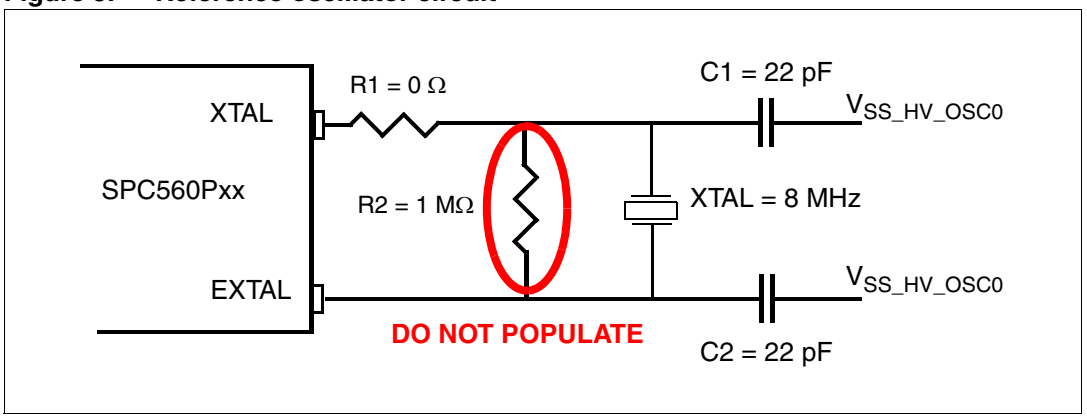
SPC560Pxx devices can run with an external oscillator used as input for the PLLs, and selected also as the system clock source. The main oscillator provides these features:

- Frequency range: 4–40 MHz
- Crystal input mode or Oscillator input mode
- PLL reference
- Oscillator supply: for noise immunity reasons, the oscillator supply uses dedicated supply pins $V_{DD_HV_OSC}/V_{SS_HV_OSC}$ instead of the 1.2 V supply

3.1 Reference oscillator circuit

Figure 5 provides a schematic of the on-chip oscillator. This section describes the key items.

Figure 5. Reference oscillator circuit



The oscillator circuit provides a reference clock signal to the on-chip PLL. The oscillator circuit consists of the following components:

- Bias resistor (R1)
- Crystal
- Two capacitors
- External bias resistor (R2)

Note: The external resistor (R2) is not recommended due to the fact that the oscillator has an internal bias resistor. However, it is recommended to leave room for an external bias resistor to allow the PCB design to accommodate different crystals.

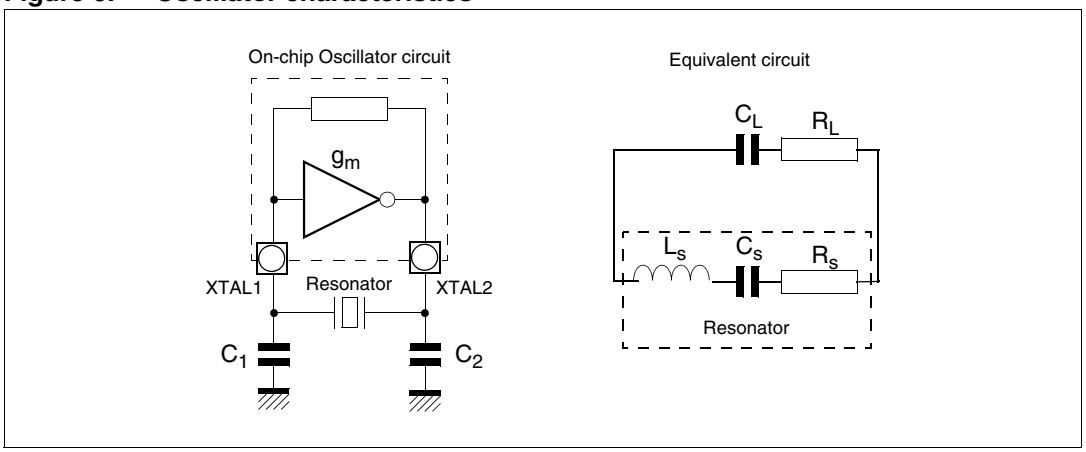
Oscillator hardware recommendations:

- Use the lowest frequency crystal possible and set the multiplication factor bits to obtain the proper system operating frequency which is generated from the PLL.
- The oscillator circuit has currents flowing at the crystal's fundamental frequency. Also, if the oscillator is clipped, then higher order harmonics will be present as well. In order to minimize the amount of emissions generated from these currents, the oscillator circuit should be kept as compact as possible.

- Also, $V_{SS_HV_OSC}$ should be connected directly to the ground plane so that return currents can flow easily between $V_{SS_HV_OSC}$ and the two capacitors (C1 and C2).
- EXTAL
  - Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode
  - Analog input for the clock generator when the oscillator is in bypass mode.
- XTAL—Analog output of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.

Note: As the oscillator is an auto-gain version, a serial resistance (R1) is normally not recommended. Please check with your crystal supplier.

Figure 6. Oscillator characteristics



3.2 Approved crystals and resonators

Following is a list of approved crystals and resonators. If you wish to use a crystal not on this list please work with the crystal manufacturer to ensure compatibility.

Table 5. Approved Crystals

Nominal frequency (MHz)	NKD crystal reference	Crystal equivalent series resistance ESR	Crystal motional capacitance (Cl) pF	Crystal motional inductance (Ll) mH	Load on xtalin/ xtalout C1=C2(pF)(1)	Shunt capacitance b/w xtalout and xtalin C0(2)(pF)
4.0	NX8045GB	300	2.68	591.0	21.0	2.93
8.0	NX5032GA	300	2.46	160.7	17.0	3.01
10.0	NX5032GA	150	2.93	86.6	15.0	2.91
12.0	NX5032GA	120	3.11	56.5	15.0	2.93
16.0	NX5032GA	120	3.90	25.3	10.0	3.00
40.0	NX5032GA	50	6.18	2.56	8.0	3.49

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

The CERALOCK resonators listed below have also been approved for use on all SPC560Pxx devices based on the e200z0 core.

Table 6. Approved Resonators

Part number	Vibration	Fr [kHz]	Fa [kHz]	Fa-Fr (dF) [kHz]	Ra [ohm]	R1 [ohm]	L1 [mH]	C1 [pF]	Co [pF]	Qm	CL1 (nominal) pF	CL2 (nominal) pF
CSTCR 4M00G 53-R0	Funda mental	3929. 50	4163. 25	233.75	372.41	12.78	0.8444 3	1.942 68	15.85 730	1630.9 3	15	15
CSTCR 4M00G 55-R0	Funda mental	3898. 00	4123. 00	225.00	465.03	11.38	0.8824 4	1.889 17	15.90 537	1899.7 7	39	39

3.3 Oscillator and electromagnetic compatibility (EMC)

The following rules and recommendations will help ensure an optimal layout and hence minimize EMC susceptibility:

- Avoid other high frequency signals near the oscillator circuitry as they can have an undesirable influence on the oscillator.
- Lay out/configure the ground supply on the basis of low impedance.
- Shield the crystal with an additional ground plane underneath the crystal.
- Do not lay out sensitive signals near the oscillator. Analyze cross-talk between different layers.
- The V_{SS} pin close to the XTAL pins must be connected to the ground plane and decoupled to the closest V_{DD} pin.
- Place capacitors at both ends of the crystal, connected directly to the ground plane while keeping the overall loop as small as possible.
- The crystal package, when metallic, should be connected directly to ground.

4 Supply pins and decoupling

SPC560Pxx family devices have different pins supply voltages. For example the SP560P50xx has six different pins supply voltage as follow:

- I/O voltage ($V_{DD_HV_IOx}$)
- Internal voltage regulator supply voltage ($V_{DD_HV_REG}$)
- Core supply ($V_{DD_LV_CORx}$)
- ADC0 and ADC1 supply ($V_{DD_HV_ADx}$)
- Crystal oscillator amplifier supply voltage ($V_{DD_HV_OSC}$)
- Code and data Flash supply voltage ($V_{DD_HV_FL}$)

for all the others family devices supply signals refer to the relative device datasheet.

4.1 Supply pins description and circuit

Table 7 lists the power supply and reference voltages for the SPC560P50xx devices.

Table 7. Supply pins on SPC560P50XX LQFP144

Supply	Symbol	Description
VREG control and power supply pins	BCTRL	Voltage regulator external NPN ballast base control pin
	VDD_HV_REG (3.3 V or 5.0 V)	Voltage regulator supply voltage
	VDD_LV_REGCOR	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between these pins and VSS_LV_REGCOR.
	VSS_LV_REGCOR	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between these pins and VDD_LV_REGCOR.
ADC0/ADC1 reference and supply voltage	VDD_HV_AD0(1)	ADC0 supply and high reference voltage
	VSS_HV_AD0	ADC0 ground and low reference voltage
	VDD_HV_AD1	ADC1 supply and high reference voltage
	VSS_HV_AD1	ADC1 ground and low reference voltage

Table 7. Supply pins on SPC560P50XX LQFP144 (continued)

Supply	Symbol	Description
Power supply pins (3.3 V or 5.0 V)	VDD_HV_IO0	Input/Output supply voltage
	VSS_HV_IO0	Input/Output ground
	VDD_HV_IO1	Input/Output supply voltage
	VSS_HV_IO1	Input/Output ground
	VDD_HV_IO2	Input/Output supply voltage
	VSS_HV_IO2	Input/Output ground
	VDD_HV_IO3	Input/Output supply voltage
	VSS_HV_IO3	Input/Output ground
	VDD_HV_FL	Code and data Flash supply voltage
	VSS_HV_FL	Code and data Flash supply ground
	VDD_HV_OSC	Crystal oscillator amplifier supply voltage
	VSS_HV_OSC	Crystal oscillator amplifier ground
Power supply pins (1.2 V)	VDD_LV_COR0	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VSS_LV_COR0 pin.
	VSS_LV_COR0	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VDD_LV_COR0 pin.
	VDD_LV_COR1	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VSS_LV_COR1 pin.
	VSS_LV_COR1	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VDD_LV_COR1 pin.
	VDD_LV_COR2	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VSS_LV_COR2 pin.
	VSS_LV_COR2	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VDD_LV_COR2 pin.
	VDD_LV_COR3	1.2 V decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest VDD_LV_COR3.
	VSS_LV_COR3	1.2 V decoupling pins for on-chip core logic. Decoupling capacitor must be connected between this pin VSS_LV_COR3.

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on VDD_HV_ADx/VSS_HV_ADx pins.

4.1.1 Internal supply decoupling capacitors

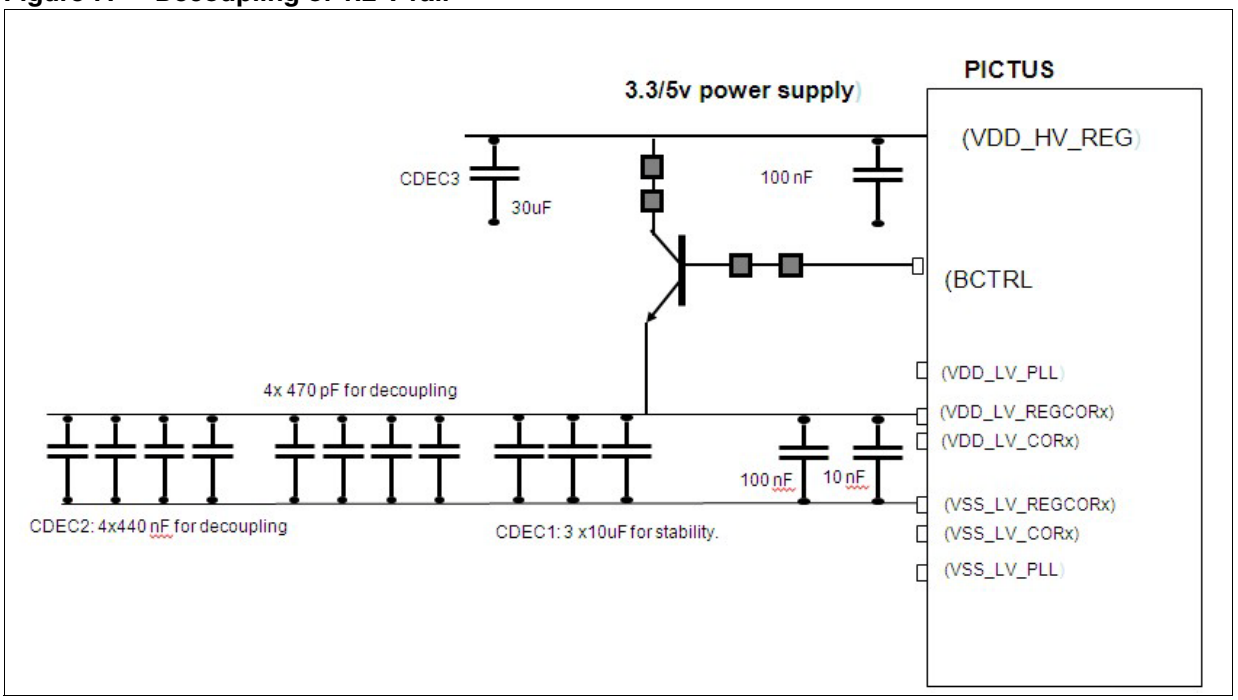
The external ballast needs output bypass capacitance for stability. Three 10 µF capacitors are recommended for transient capability. In addition, for decoupling (that is, supply variations) a pair of ceramic capacitors is required for each supply/GND pair. The general rule for decoupling capacitors is to share equally the CDEC2 value (refer to device's datasheet), and the 1880 pF capacitance value among all the supply pins VDD_LV_CORx/VSS_LV_CORx.

In order to remain in the range requested by DS, required capacitor values have to include the de-rating factor coming from tolerance, temperature, and aging effects. These factors must be taken into account to assure proper operation under worst case conditions.

X7R type materials are recommended for all capacitors, based also on ESR characteristics.

In *Figure 7* is shown as example the decoupling of 1.2 V rail for SPC50P50L5 whose number of supply pins VDD_LV_CORx/VSS_LV_CORx is 4. It can be avoided to use decoupling cap near pin pair VDD_LV_REGCOR/VSS_LV_REGCOR.

Figure 7. Decoupling of 1.2 V rail



Layout recommendations:

- The three stability capacitors C_{DEC1} (that is, 3 x 10 µF) must be placed next to the ballast output.
- Use preferably a small plane to distribute Vcore (that is, 1.2 V) with a low parasitic inductance to each pin or a star topology from the ballast output.
- The Resulting parasitic inductance, ESL of VDD_HV_REG, BCTRL and VDD_LV_CORx pins, must be kept below the maximum value of L_{REG} parameter as described in the device datasheet
- Low Equivalent Series Resistance (ESR) and low Equivalent Series Inductance (ESL) capacitors should be used for the 10 µF stability capacitors. Use preferably ceramic capacitors. Do not use electrolytic capacitors as stabilization capacitors.

Note: Check the device datasheet R_{REG} parameter for the recommended maximum ESR value.

Note: The use a multi-layer printed circuit board (PCB) with a separate layer dedicated to the ground and another one to the voltages supply is recommended.

4.1.2 Specific supply decoupling

Although SPC560Pxx/SPC56APxx/SPC56APxx devices have only one external supply, several types of pins are connected to this supply and consequently must have a specific decoupling.

Each pair of V_{CC}/GND pins must have two ceramic capacitors for local decoupling.

Flash, Oscillator

A pair of ceramic capacitors (100 nF + 470 pF) is recommended per V_{CC}/GND pair.

I/Os

I/O decoupling should be checked according to the I/O real activity.

Each V_{CC}/GND pair for I/O supply must have a pair of decoupling ceramic capacitors; one with a value of 33 nF to 100 nF and the other one with a value of 470 pF to 1 nF.

ADC

During SPC560Pxx/SPC56APxx design, several supply schemes of the two ADCs have been analyzed and simulated. The best one is the one with shared supply and reference per ADC.

For this reason, serial resistance on ADC supply and GND must be avoided.

PLL

The PLL is supplied by the 1.2 volt rail. Recommended decoupling capacitors are 100 nF and 10 nF.

Main supply decoupling

The recommendations described above assume that enough reservoir capacitors are placed at the output of the VREG generating the 5 V or 3.3 V supply for the SPC560Pxx/SPC56APxx device. Those capacitors are dependent on the type of voltage regulator used and hence are not specified here.

4.1.3 Power-on current control

On power-on, the embedded voltage regulator starts to work at about 2.8 V and stops to at about 2.5 V (0.3 V hysteresis with power-on threshold).

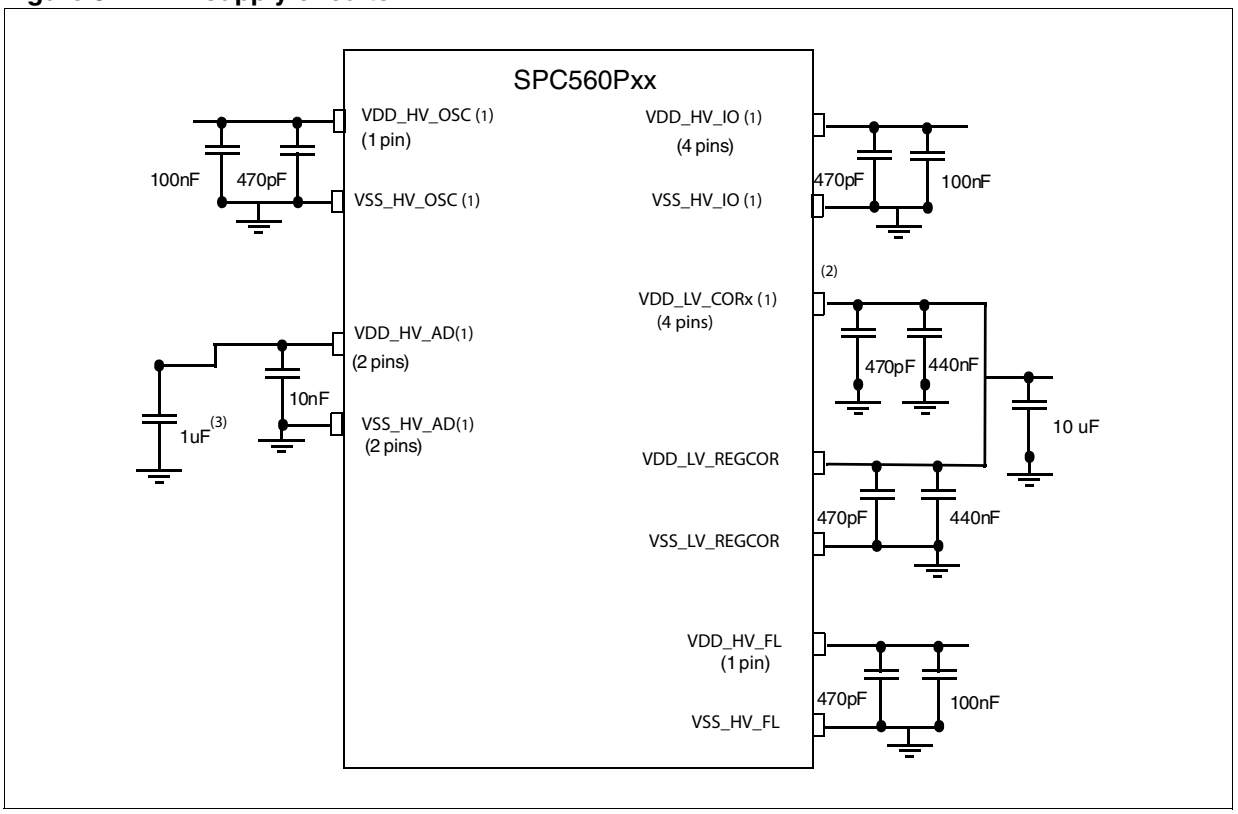
Once the minimum supply is met, the embedded voltage regulator then switches ON the external ballast.

Slope characteristics on all VDD during power up has to be inside TVDD parameter range as described in the device datasheet [(a)].

4.1.4 Summary

Figure 8 summarizes the SPC560Pxx device decoupling requirements (please refer to *Table 7* for descriptions of the supply/ground reference lines).

Figure 8. Pin supply circuits



1. The microcontroller can have more than one pin of this type. A couple of capacitors must be placed close to each pin as shown in this diagram.
2. The microcontroller can have more than one pin of this type. A 10 uF capacitors must be placed close to each pin
3. The capacitor is only one. These capacitors on VDD_HV_AD pin can be also not close to the associated pins.
4. The recommended decoupling/stability capacitors can vary based on specific chosen ballast or circuitry. See the device datasheet to choose the best recommended values For more information on SPC560Pxx reset, please refer to the device reference manual.

a. For the following list of devices:

-SPC560P34xx/P40xx cut1.1 and older

-SPC560P50xx/P44xx cut3.4 and older

-SPC560P60xx/P54xx

-SPC56AP60xx/AP54xx

It is not enough to be inside TVDD parameter range. it is needed on VDD_HV_REG pin a monotonic ramp up to 5V or 3.3V starting from zero. To make the power up of the device more robust put a resistive network between VDD_HV_REG, VDD_LV_REG and GND (see AN4057 for more details)

5 Unused pin management

In some applications, not all pins of the device may be needed.

For all unused pins (digital pin and analog pin), it is recommended that software configure them as floating input with internal or external weak pull-up/pull-down. Using both internal and external weak pull, pay attention to use the same pull type so to avoid direct link to VDD/VSS. For unused analog pin don’t enable the analog pad control PCR[APC].

More pins can be linked to the same pull-up/down resistance.

Additional recommendation:

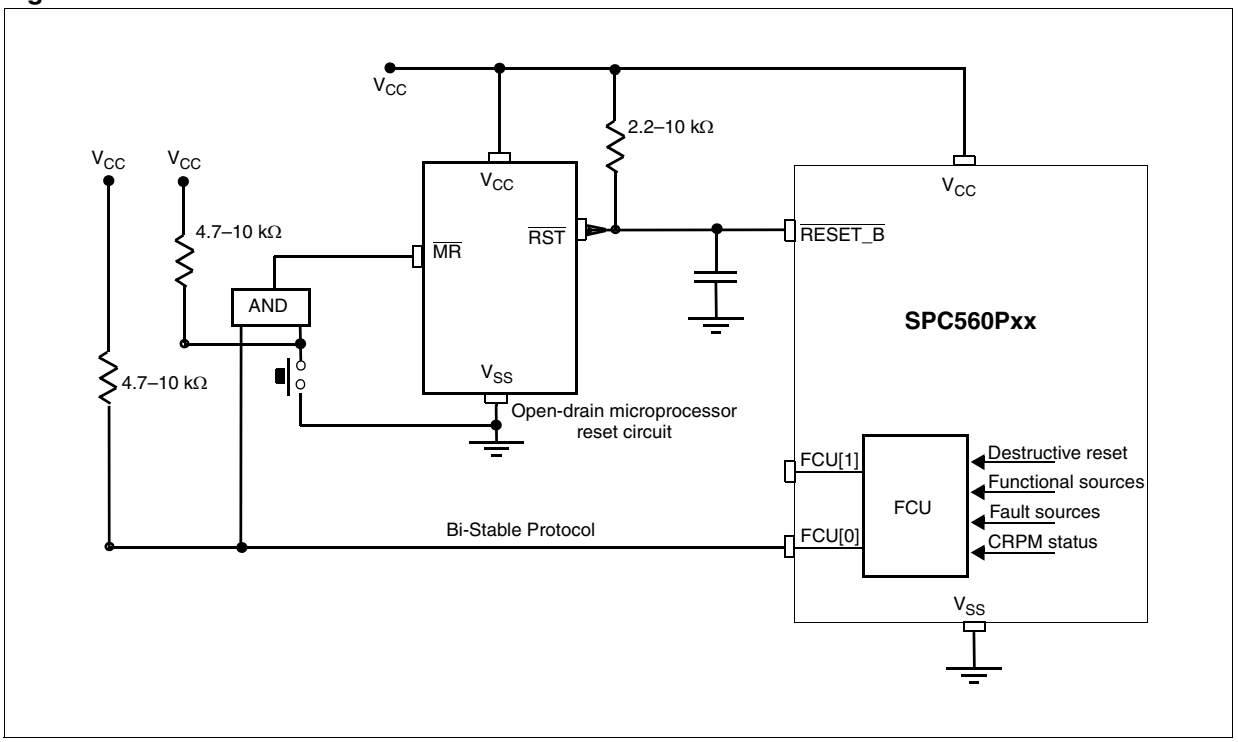
All unused pins should be tied off. Software doesn't enable the output buffers of the pads (PCR[OBE] bit) to avoid a path with current injection inside the device.

There is no specific recommendation for external resistances but it is good practice to use 10 kOhm as pull-up/down resistance.

6 Reference reset circuit

The minimum reset pulse duration is 500 ns as reported in the device datasheet.

Figure 9. Reference reset circuit



7 Revision history

Table 8. Document revision history

Date	Revision	Changes
2-Apr-2009	1	Initial release.
16-Jan-2013	2	Updated *Section 2.1.1: Voltage regulator*. Updated *Section 2.1.3: Recommended transistors*. Updated *Section 4.1.1: Internal supply decoupling capacitors*. Updated *Section 4.1.3: Power-on current control*. Added *Table 5*. Added *Table 6*. Added *Chapter 5: Unused pin management*.
18-Sep-2013	3	Updated Disclaimer.

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