TMP63 100-kΩ Linear Thermistor With 0402 Package Option

1 Features

- Silicon-based thermistor with a Positive Temperature Coefficient (PTC)
- Linear resistance change across temperature
- 100-kΩ nominal resistance at 25°C (R25)
  - ±1% maximum (0°C to 70°C)
- Wide operating temperature of –40°C to +125°C
- Consistent sensitivity across temperature
  - 6400 ppm/°C TCR (25°C)
  - 0.2% typical TCR tolerance across temperature range
- Fast thermal response time of 0.6 s (DEC)
- Long lifetime and robust performance
  - Built-in fail-safe in case of short-circuit failures
  - <1% maximum long term sensor drift
- Available package options:
  - X1SON (DEC/0402 footprint)

2 Applications

- Temperature Monitoring
  - HVAC & thermostats
  - Industrial control and appliances
- Thermal compensation
  - Display backlights
  - Building automation
- Thermal threshold detection
  - Motor control
  - Chargers

3 Description

The TMP63 series of linear thermistors exhibit a large change in resistance with temperature.

Its linearity and consistent sensitivity across temperature enable simple and accurate methods for temperature conversion. Low power consumption and a small thermal mass minimize the impact of self-heating. The built-in failsafe behavior at high temperatures and powerful immunity to environmental variation of these devices is designed for a long lifetime of high performance. The small size of the TMP63 series allows for close placement to heat sources and quick response times.

Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory in the processor.

The TMP63 series is currently available in a 0402 footprint-compatible X1SON package.

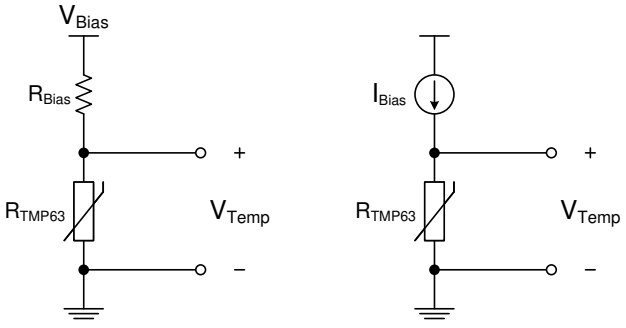
For complete resistance vs temperature table (R-T table) computation and helpful methods to derive temperature, see the Thermistor Design Tool.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP63	X1SON (2)	0.60 mm × 1.00 mm

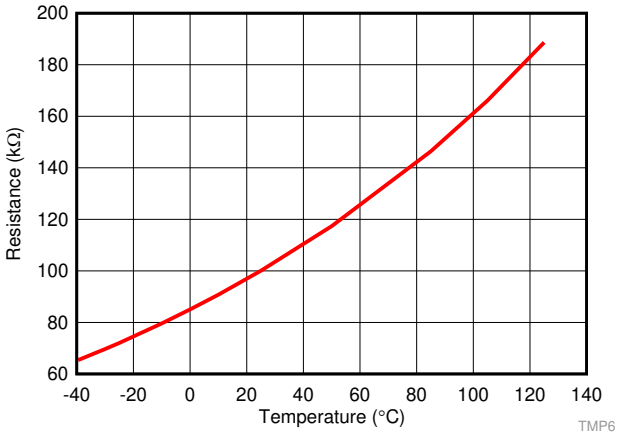
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Implementation Circuits



$$V_{Temp} = \frac{V_{Bias} * R_{TMP63}}{R_{Bias} + R_{TMP63}} \qquad V_{Temp} = I_{Bias} * R_{TMP63}$$

Typical Resistances vs Ambient Temperature



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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 TMP63 R-T table ... 9
7.4 Feature Description ... 9
7.5 Device Functional Modes ... 9
8 Application and Implementation ... 10
8.1 Application Information ... 10
8.2 Typical Application ... 10
9 Power Supply Recommendations ... 15
10 Layout ... 15
10.1 Layout Guidelines ... 15
10.2 Layout Example ... 15
11 Device and Documentation Support ... 16
11.1 Receiving Notification of Documentation Updates 16
11.2 Support Resources ... 16
11.3 Trademarks ... 16
11.4 Electrostatic Discharge Caution ... 16
11.5 Glossary ... 16
12 Mechanical, Packaging, and Orderable Information ... 16

4 Revision History

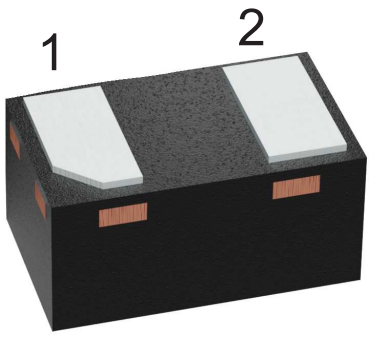
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2019) to Revision A	Page
• Changed device status from Advanced Information to Production Data	1

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5 Pin Configuration and Functions

DEC Package
2-Pin X1SON
Top View (Angled)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	X1SON (DEC)		
–	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across pins 2 (+) and 1(–)		+6	V
Current through the device		+450	µA
Junction temperature (T_J)	–40	+150	°C
Storage temperature (T_{stg})	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) per JESD22-A114 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage across pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current through the device	0		400	µA
T_A	Operating free-air temperature (specified performance) (X1SON/DEC Package)	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP63 DEC (X1SON) 2 PINS	Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2) (3)	443.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	254.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

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6.5 Electrical Characteristics

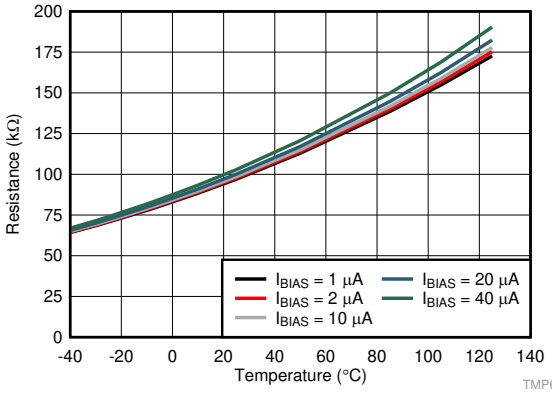
T_A = -40°C - 125°C, I_{Sns} = 20 µA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25°C	T_A = 25°C		100		kΩ
R_{TOL}	Resistance Tolerance	T_A = 25°C	–1		1	%
		T_A = 0°C - 70°C	–1		1	
		T_A = -40°C - 125°C	–1.5		1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = -40°C, T2 = -30°C		+6220		ppm/°C
TCR_{25}		T1 = 20°C, T2 = 30°C		+6400		
TCR_{85}		T1 = 80°C, T2 = 90°C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = -40°C, T2 = -30°C		±0.4		%
TCR_{25} %		T1 = 20°C, T2 = 30°C		±0.2		
TCR_{85} %		T1 = 80°C, T2 = 90°C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation RH = 85%, T_A = 130°C, V_{Bias} = 5.5 V	0.1		0.8	%
		600 hours continuous operation T_A = 150°C, V_{Bias} = 5.5 V	0.1		1	
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63%	T1 = 25°C in Still Air to T2 = 125°C in Stirred Liquid		0.6		s
$t_{RES\ (still\ air)}$	Thermal response to 63%	T1 = 25°C to T2 = 70°C in Still Air		3.2		s

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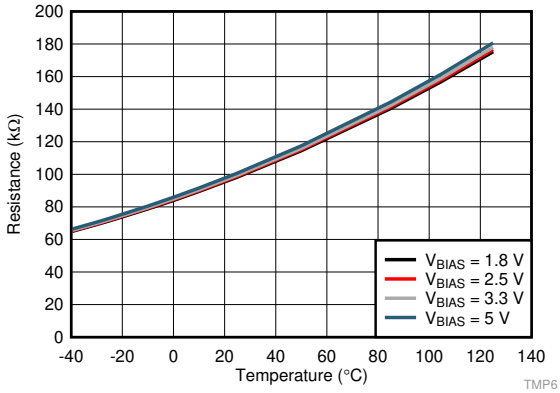
6.6 Typical Characteristics

at T_A = 25°C, (unless otherwise noted)



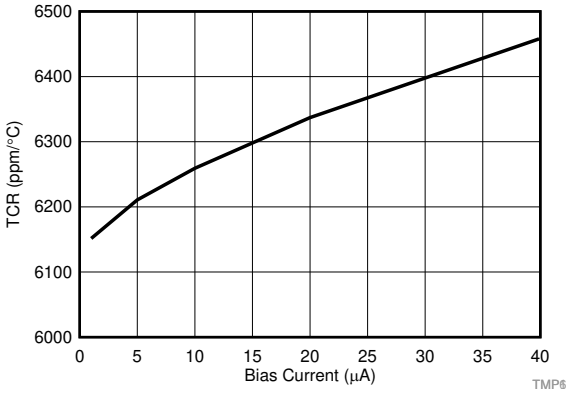
TMP63: I_{Bias} = 1 µA, 10 µA, 20 µA, and 40 µA

Figure 1. Resistance vs. Ambient Temperature Using Multiple Bias Currents



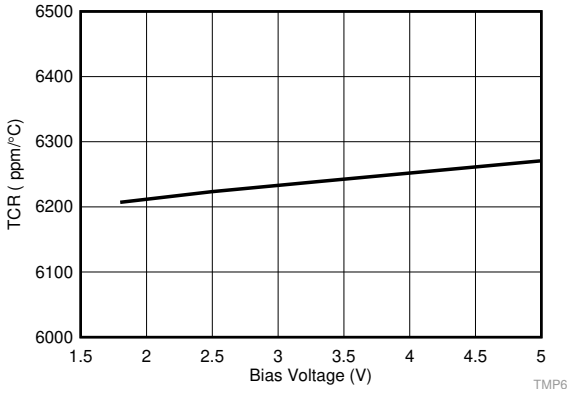
TMP63: V_{Bias} = 1.8 V, 2.5 V, 3.3 V, and 5.0 V, R_{Bias} = 100 kΩ with ±0.01% Tolerance

Figure 2. Resistance vs. Ambient Temperature Using Multiple Bias Voltages



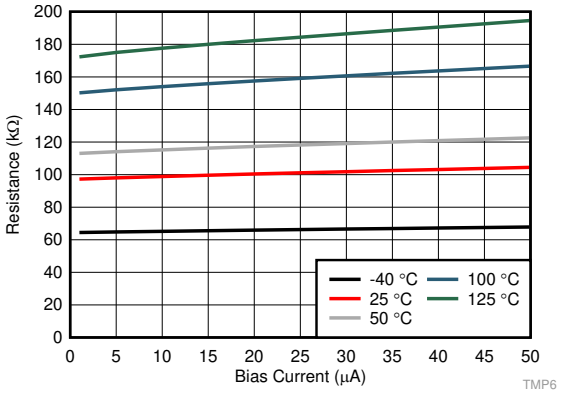
TMP63: I_{Sns} = 1 µA, 10 µA, 20 µA, and 40 µA

Figure 3. TCR as a Function of Sense Currents I_{Sns}



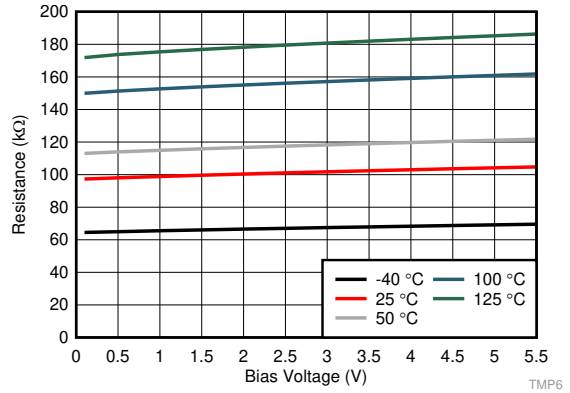
TMP63: V_{Sns} = 1.8 V, 2.5 V, 3.3 V, and 5.0 V, R_{Bias} = 100 kΩ with ±0.01% Tolerance

Figure 4. TCR as a Function of Sense Voltages, V_{Sns}



TMP63: T_A = –40°C, 25°C, 50°C, 100°C, and 125°C

Figure 5. Supply Dependence R vs. I_{Bias}



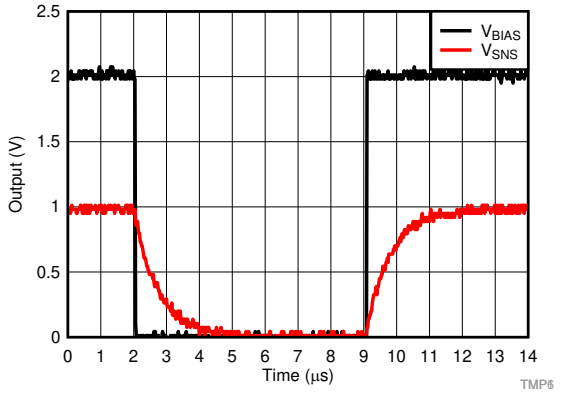
TMP63: T_A = –40°C, 25°C, 50°C, 100°C, and 125°C, R_{Bias} = 100 kΩ with ±0.01% Tolerance

Figure 6. Supply Dependence R vs. V_{Bias}

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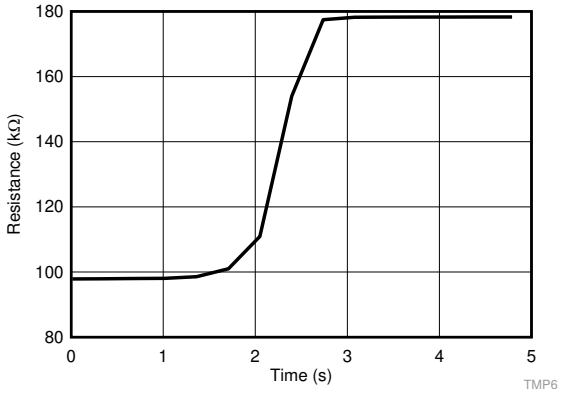
Typical Characteristics (continued)

at T_A = 25°C, (unless otherwise noted)



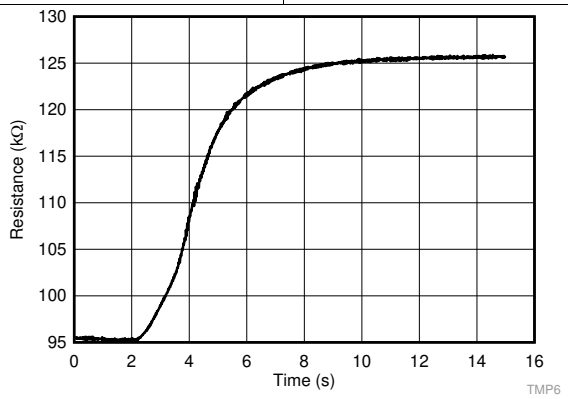
TMP63: V_{Sns} = 1 V

Figure 7. Step Response



TMP63: Stirred Liquid

Figure 8. Thermal Response Time



TMP63: Still Air

Figure 9. Thermal Response Time

7 Detailed Description

7.1 Overview

The TMP63 series of silicon linear thermistors has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range. To fabricate the TMP63, a special silicon process is used where the devices key characteristics—the temperature coefficient resistance (TCR) and nominal resistance (R25)—are controlled by the doping level and active region area. Note that the TMP63 has an active area and a substrate due to the polarized terminals of the device. The positive terminal should be connected to the highest potential, while the negative terminal should be connected to the lowest potential.

The TMP63 is different from a NTC, where a NTC is a purely resistive device, the TMP63's resistance is affected by the current across the part and will change with temperature. In a voltage divider circuit, it is recommended that the top resistor is kept at 100 kΩ. Changing the top resistor or the VBIAS will change the resistance vs temperature table (R-T table) of the TMP63, and subsequently the polynomials as described in *Design Requirements*. Consult the TMP63 R-T table section for more information.

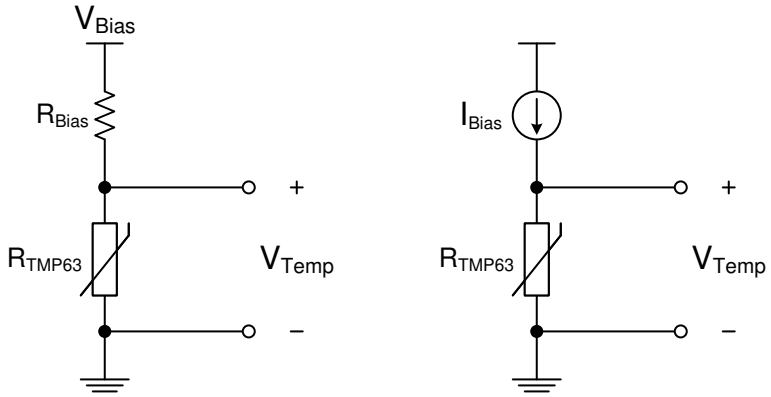
Equation 1 can help the user approximate the TCR.

$$TCR\ (ppm/°C) = (R_{T2} - R_{T1}) / ((T_2 - T_1) \times R_{(T2+T1)/2}) \quad (1)$$

Below are the definitions of the key terms used throughout this document:

- I_{Sns}: Current flowing through the TMP63.
- V_{Sns}: Voltage across the two TMP63 terminals.
- I_{BIAS}: Current supplied by the biasing circuit.
- V_{BIAS}: Voltage supplied by the biasing circuit.
- V_{TEMP}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{Sns}. In the use case of a voltage divider circuit with the TMP63 in the high side, V_{TEMP} is taken across R_{BIAS}.

7.2 Functional Block Diagram



$$V_{Temp} = \frac{V_{Bias} * R_{TMP63}}{R_{Bias} + R_{TMP63}} \qquad V_{Temp} = I_{Bias} * R_{TMP63}$$

Figure 10. Typical Implementation Circuits

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7.3 TMP63 R-T table

The TMP63 R-T table must be re-calculated for any change in the bias voltage, bias resistor, or bias current. TI provides a Thermistor Design Tool to calculate the R-T table. The system designer should always validate the calculations provided.

7.4 Feature Description

7.4.1 Linear resistance curve

The TMP63 has good linear behavior across the whole temperature range as shown in Figure 3. This allows a simpler resistance to temperature conversion method that reduces look up table memory requirements. Additionally the linearization circuitry or midpoint calibration associated with traditional NTCs is not necessary with TMP63.

Because the TMP63 is linear across the entire temperature range, this has an added benefit that the TMP63 will also not lose sensitivity at higher operating temperatures.

7.4.2 Positive Temperature Coefficient (PTC)

The TMP63 has a positive temperature coefficient. As temperature increases the TMP63 resistance will increase leading to a reduction in power consumption of the bias circuit. A negative coefficient system will have power consumption increase with temperature as the resistance decreases.

The TMP63 will also benefit from the reduced power consumption of the bias circuit with less self-heating than a typical NTC system.

7.5 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP63 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves like a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP63 has a nominal resistance at 25°C (R25) of 100 kΩ, a maximum operating voltage of 5.5 V (V_{Sns}), and maximum supply current of 400 µA (I_{Sns}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

8.2 Typical Application

8.2.1 Thermistor Biasing Circuits

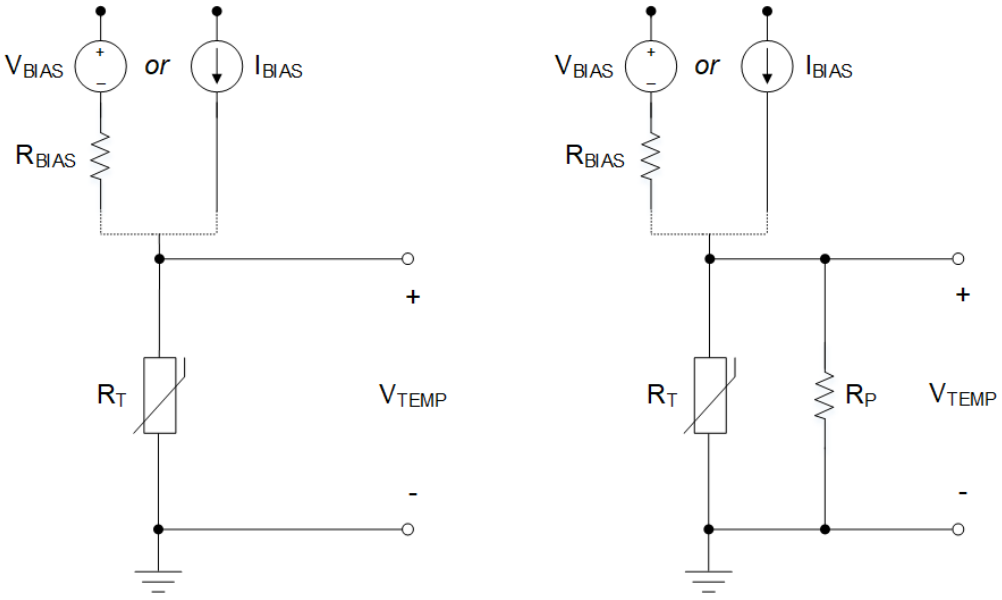


Figure 11. Biasing Circuit Implementations With Linear Thermistor (Left) vs. Non-Linear Thermistor (Right)

8.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature vs. resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. Thermistor Biasing Circuits highlights the two implementations where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Alternatively, the thermistor can be biased directly using a precision current source (yielding the highest accuracy

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Typical Application (continued)

and voltage gain). It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP63, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such that the voltage measured across it increases linearly with temperature. As such, the need for a linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the TMP63, as described in Equation 2, can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T). The Thermistor Design Tool must be used to translate Vtemp to Temperature. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, the bias voltage (V_{BIAS}) should be tied to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The engineer can also implement a low-pass filter to reject system level noise, and the user should place the filter as close to the ADC input as possible.

8.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply will be canceled and will not affect the temperature accuracy. This type of configuration is shown in Figure 12. Equation 2 describes the output voltage (V_{TEMP}) based on the variable resistance of the TMP63 (R_{TMP63}) and bias resistor (R_{BIAS}). The ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution is given in Equation 3.

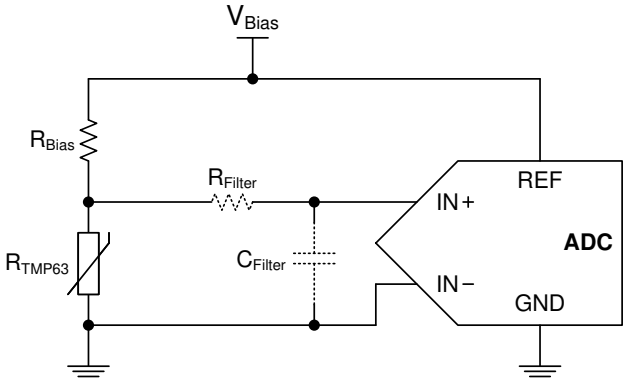


Figure 12. TMP63 Voltage Divider With an ADC

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP63}}{R_{BIAS} + R_{TMP63}} \right) \quad (2)$$

$$\text{ADC Code} = \left(\frac{V_{TEMP}}{FSR} \right) \times 2^n \quad (3)$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows whenever $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$\text{ADC Code} = \left(\frac{V_{BIAS} \times \left(\frac{R_{TMP63}}{R_{BIAS} + R_{TMP63}} \right)}{V_{BIAS}} \right) \times 2^n = \left(\frac{R_{TMP63}}{R_{BIAS} + R_{TMP63}} \right) \times 2^n \quad (4)$$

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Typical Application (continued)

The engineer can use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller. The Thermistor Design Tool should be used to translate the TMP63 resistance to temperature.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, not all of the ADC codes will be used due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

The engineer can use a current source-based circuit, like the one shown in Figure 13, to have better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 40 µA is used with the TMP63, the output voltage will span approximately 5.5 V and will have a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full utilization of the ADC codes and full-scale range. Based on the bias current, the temperature voltage is shown in Figure 18. Similar to the ratiometric approach above, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

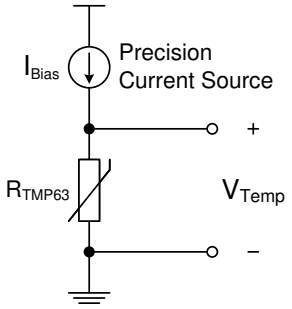


Figure 13. TMP63 Biasing Circuit With Current Source

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP63 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, are shown in Figure 14. Consider an example where V_{BIAS} = 5 V, R_{BIAS} = 100 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 100-kΩ resistor. The TMP63 produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear but greatly affects the output voltage range.

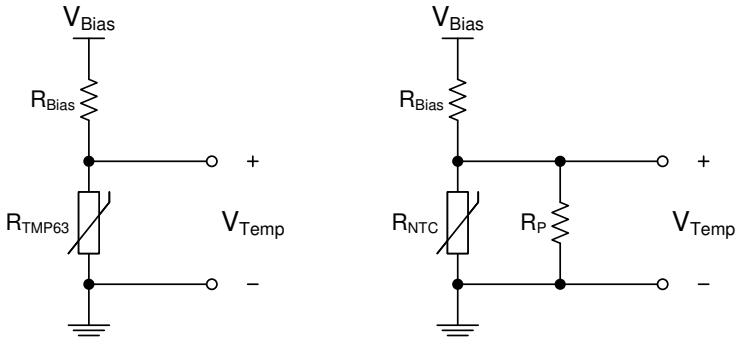


Figure 14. TMP63 vs. NTC With Linearization Resistor (R_P) Voltage Divider Circuits

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Typical Application (continued)

8.2.1.2.1 Thermal Protection With Comparator

The engineer can use the TMP63, a voltage reference, and a comparator to program the thermal protection. As shown in Figure 15, the output of the comparator will remain low until the voltage of the thermistor divider, with R_{BIAS} and R_{TMP63}, rises above the threshold voltage set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

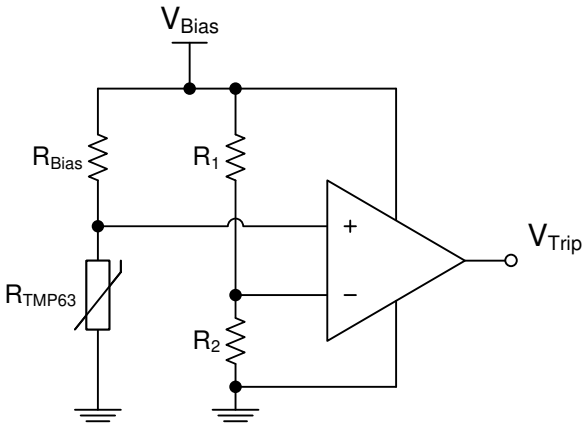


Figure 15. Temperature Switch Using TMP63 Voltage Divider and a Comparator

8.2.1.2.2 Thermal Foldback

One application that uses the output voltage of the TMP63 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The TMP63 voltage output increases with temperature when the output is in the lower position of the voltage divider and can provide a response used to fold back the current. Typically, the current is held at a specified level until a high temperature is reached, known as the knee point, where the current must be rapidly reduced. To better control the temperature/voltage sensitivity of the TMP63, a rail-to-rail operational amplifier is used. In the example shown in Figure 16, the temperature “knee” where the foldback begins is set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 5 (like 110°C, for example). A buffer is used in-between the voltage divider with R_{TMP63} and the input to the op amp to prevent loading and variations in V_{TEMP}.

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Typical Application (continued)

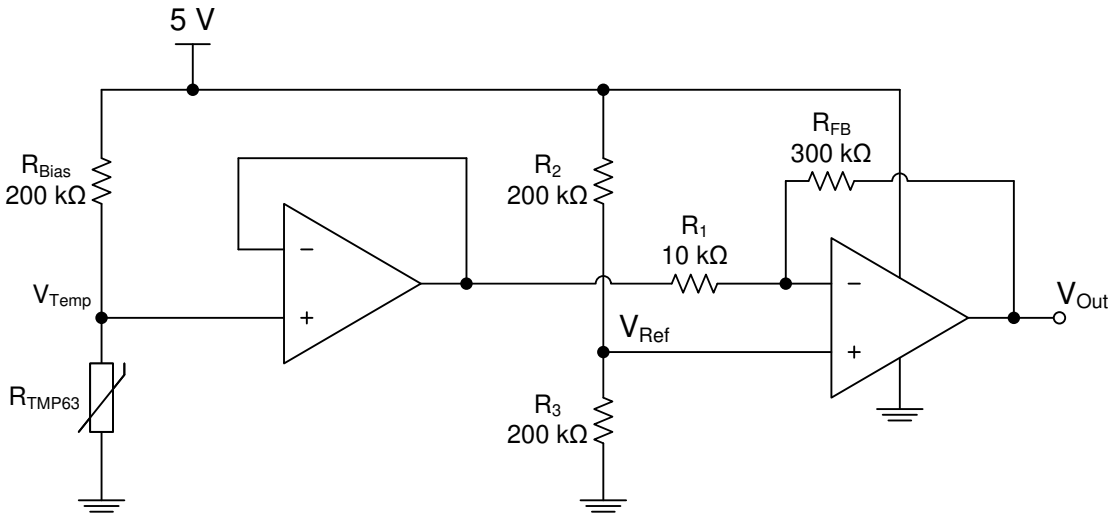


Figure 16. Thermal Foldback Using TMP63 Voltage Divider and a Rail-to-Rail Op Amp

The op amp will remain high as long as the voltage output is below V_{Ref}. When the temperature goes above 110°C, then the output will swing low to the 0-V rail of the op amp. The rate at which the foldback occurs is dependent on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, given by Equation 6. This in return controls the voltage/temperature sensitivity of the circuit. This voltage output is fed into a LED driver IC that will adjust output current accordingly. The final output voltage used for thermal foldback is V_{OUT}, and is given in Equation 7. In this example where the knee point is set at 110°C, the output voltage curve is as shown in Figure 17.

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP63}}{R_{BIAS} + R_{TMP63}} \right) \tag{5}$$

$$G = \frac{R_{FB}}{R_1} \tag{6}$$

$$V_{OUT} = -G \times V_{TEMP} + (1 + G) \times V_{REF} \tag{7}$$

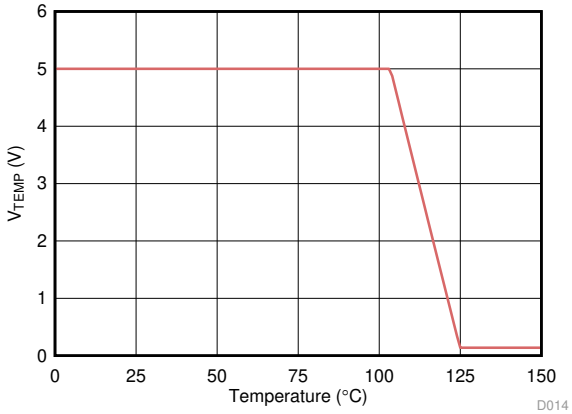


Figure 17. Thermal Foldback Voltage Output Curve

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Typical Application (continued)

8.2.2 Application Curve

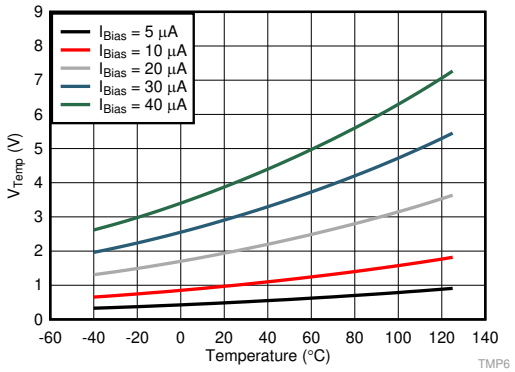


Figure 18. TMP63 Temperature Voltage With Varying Current Sources

9 Power Supply Recommendations

The maximum recommended operating voltage of the TMP63 is 5.5 V (V_{Sns}), and the maximum current through the device is 400 µA (I_{Sns}).

10 Layout

10.1 Layout Guidelines

The layout of the TMP63 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground, and V+ is connected to the output (V_{TEMP}). If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage (V_{TEMP}). Figure 19 shows the device layout.

10.2 Layout Example

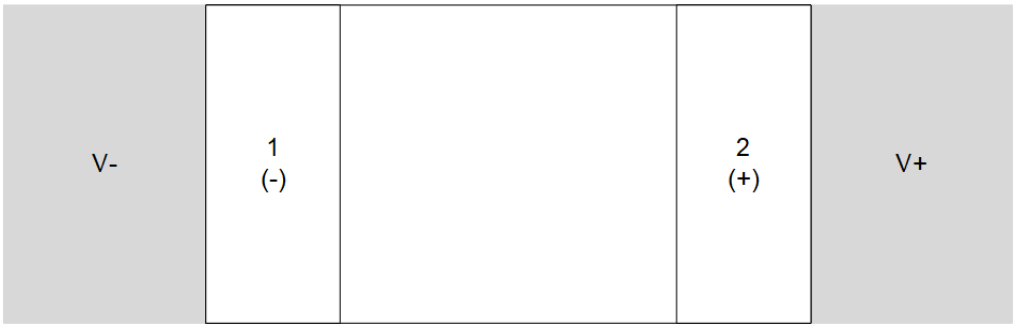


Figure 19. Recommended Layout: DEC Package

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP6331DECT	ACTIVE	X1SON	DEC	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC	Samples
TMP6331DECR	ACTIVE	X1SON	DEC	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC	Samples
TMP6331DECT	ACTIVE	X1SON	DEC	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

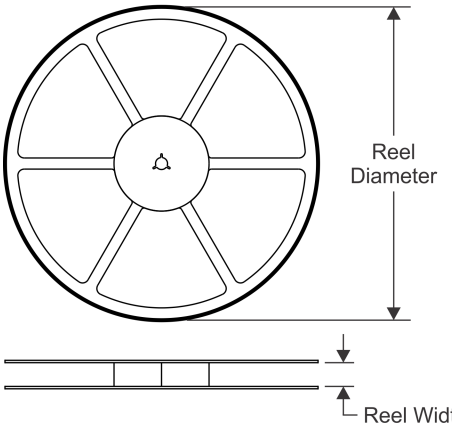
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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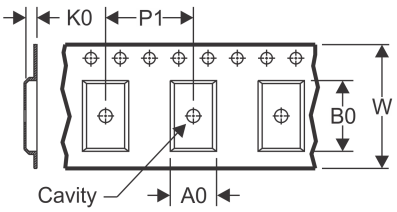
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

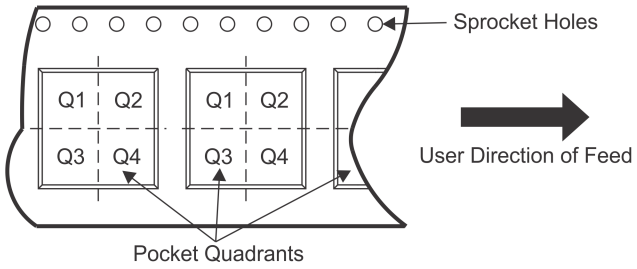


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

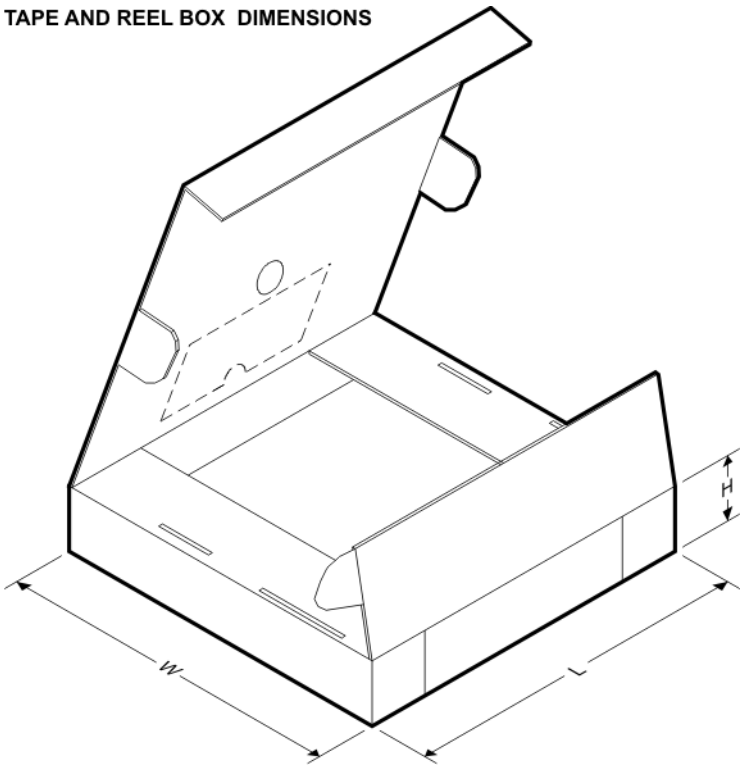
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6331DECR	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6331DECT	X1SON	DEC	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

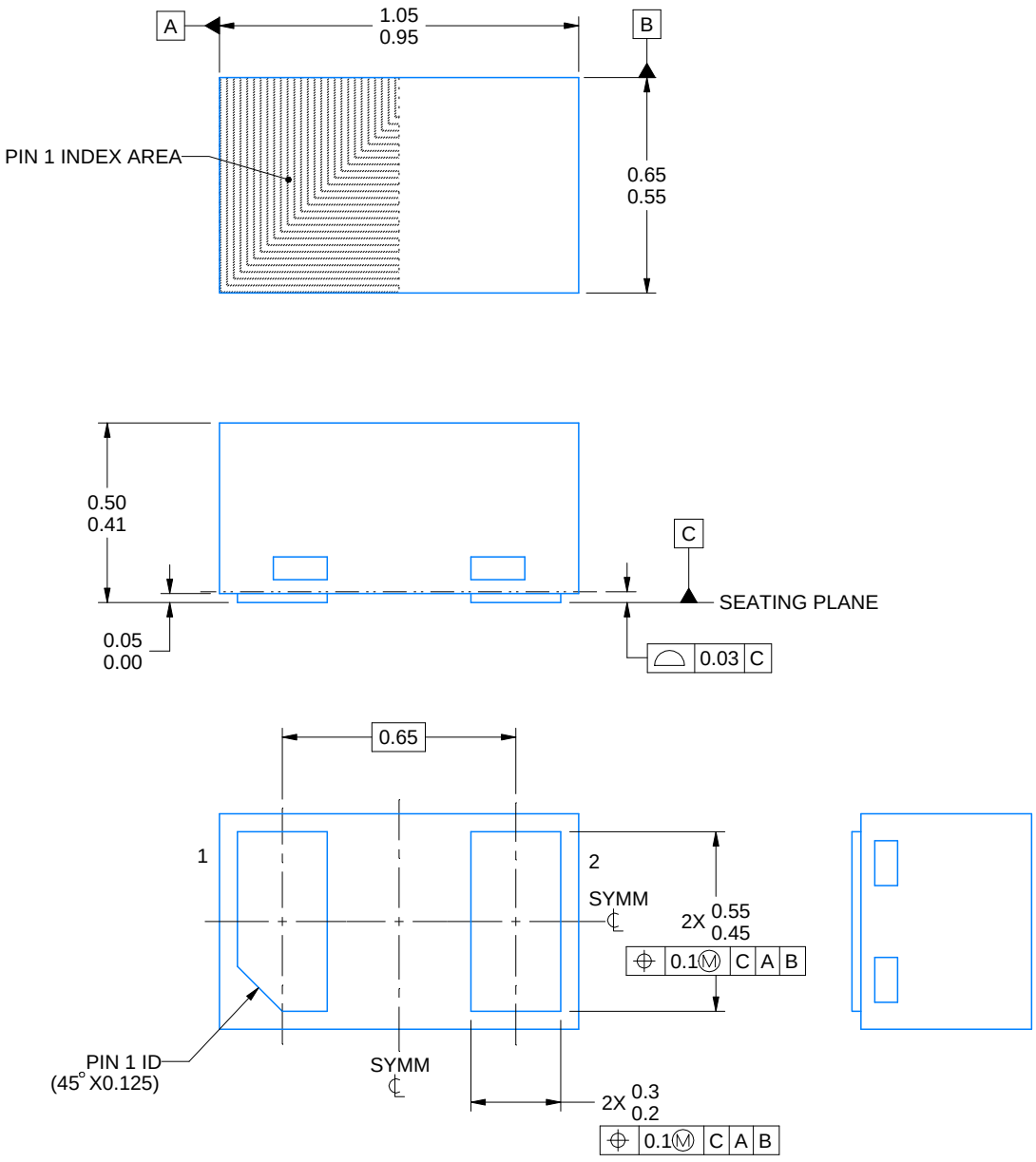
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6331DECR	X1SON	DEC	2	10000	205.0	200.0	33.0
TMP6331DECT	X1SON	DEC	2	250	205.0	200.0	33.0

PACKAGE OUTLINE

DEC0002A

X1SON - 0.5 mm max height

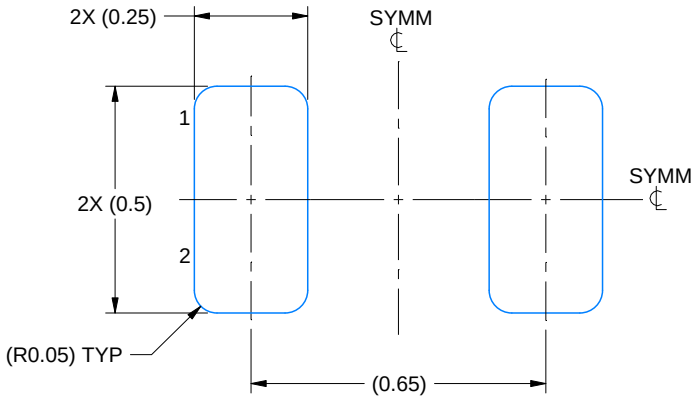
PLASTIC SMALL OUTLINE - NO LEAD



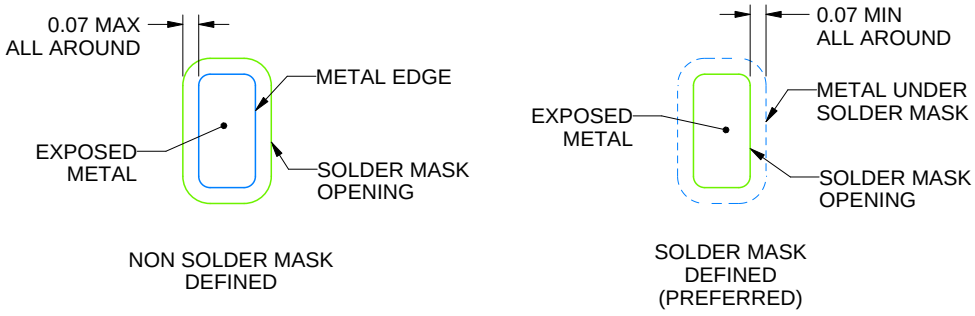
4224506/A 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

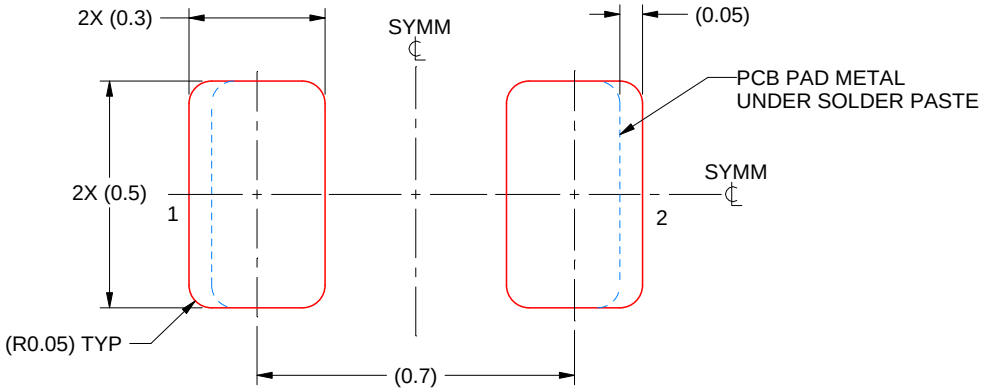


SOLDER MASK DETAILS

4224506/A 08/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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