# AN-7515

## Combined Single-Pulse and Repetitive UIS Rating System

## Summary

A rating system for Unclamped Inductive Switching (UIS) in PowerMOS transistors already widely accepted and implemented on Fairchild PowerMOS transistor datasheets can be applied to a wide range of applications and expanded to cover repetitive UIS pulses by superposition. This allows PowerMOS transistor users to determine if their application lies within the rated capability of a power transistor. Two examples are given of the analysis of UIS stress level in representative applications. The ability of PowerMOS transistors to withstand UIS has been recognized since 1985. Although Blackburn has clearly shown[1] UIS stress level is not directly related to energy, many manufacturers of PowerMOS transistors persist in rating their devices in terms of energy capability. Since the energy capability varies with the operating conditions, this rating is valid only at the condition specified and the PowerMOS transistor user has no way to calculate whether the particular application exceeds the device rating. Ronan has defined a rating system[3], herein after called the UIS Rating System, that allows manufacturers to specify the capability of PowerMOS transistors for single-pulse UIS in such a way that users can determine if the application exposes the device to more UIS stress than is guaranteed in the datasheet.

### Single-Pulse UIS Rating System

This UIS Rating System requires the user to determine only the peak current through the PowerMOS transistor ($I_{AS}$), the junction temperature at the start of the UIS pulse ($T_J$), and the time the transistor remains in avalanche ($t_{AV}$). It allows the determination of the conformance of any application to a specified UIS capability where the worst-case conditions can be simulated. It is also quite feasible to calculate the UIS stresses for circuits not yet constructed or conditions not easily simulated.

The UIS rating for a PowerMOS transistor (*see Figure 1*) is presented as a chart with a vertical axis of ($I_{AS}$) maximum avalanche current vs. ($t_{AV}$) time in avalanche as the horizontal axis. Two lines are shown, one for 25°C and one for a higher junction temperature. It is fairly easy, in most applications, to determine the avalanche current and time in avalanche in an existing application by using a current probe. If the time in avalanche and avalanche current plotted on the UIS rating curve fall above and to the right of the 25°C line, the application is beyond the UIS rating of the device and the user stands a risk of device failure. If the time and current plotted on the rating curve fall below and to the left of the maximum junction temperature line, the application is within the UIS rating of the device. In either case, no further analysis is needed. If the time and current plotted on the rating chart falls between the 25°C and the maximum junction temperature lines, further analysis is required.

To analyze those cases where the starting temperature and time in avalanche fall between the 25°C and maximum temperature line, determine the junction temperature of the PowerMOS transistor at the start of the UIS pulse. If the UIS stress occurs after a long period in conduction, it may be sufficient to measure the case temperature of the device and calculate the temperature rise between the case and junction from the dissipation and thermal resistance of the device. Any other approach may be used. Once the junction temperature at the start of the pulse has been determined, extrapolate between the two published rating curves to determine the UIS capability at that starting junction temperature.

Ronan[3], Stoltenburg[2] and Blackburn[1] have all indicated that the UIS capability $I^2_{AS}t_{AV}$ is a linear function of temperature. Using this allows a straight line extrapolation of the UIS capability of the device at the calculated junction temperature. Then compare the calculated capability to the stress to determine if the device is within ratings. This simple approach allows users to decide if the application is safe for any single UIS pulse.

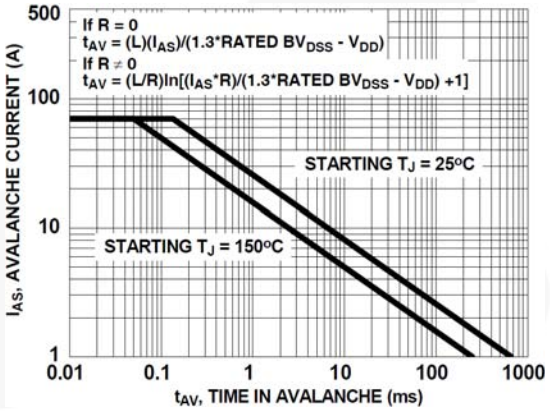


**Figure 1. FDB8444 Unclamped Inductive Switching (Single-Pulse UIS)**

## Multiple or Repetitive UIS

The handling of repetitive UIS pulses has been mostly ignored by PowerMOS transistor manufacturers except for an attempt by one manufacturer to rate repetitive UIS at 0.01% of the 25°C power rating with no further qualifications. The UIS rating system outlined by Ronan's[3] is applicable to repetitive pulses by using the technique of superposition as is commonly used in evaluating repetitive SOA pulses. Each UIS pulse is considered a separate event and evaluated as if no other pulse existed. It is necessary only to determine $I_{AV}$ (avalanche current), $t_{AV}$ (time in avalanche), and $T_J$ (junction temperature at the start of the pulse); just as in the single pulse case[6]. Usually the last pulse in a series occurs at the highest junction temperature and is therefore the most severe stress. If the PowerMOS transistor is within the specified UIS rating for that pulse, it is certainly within the UIS ratings for previous pulses that occurred at a lower junction temperature.

The junction temperature variation of a PowerMOS transistor over a full repetitive period is usually very small. The device has a thermal capacitance and does not change temperature instantaneously, so using average junction temperature for starting temperature to evaluate avalanche stress does not usually result in appreciable error. Where the period is long, other means must be used to determine junction temperature at the start of the UIS pulse.

## Examples

The following two examples shown next are intended only to illustrate the techniques used to calculate whether or not a PowerMOS transistor is within its UIS rating. Since UIS capability is an interactive function of other environmental stresses, it is necessary to include some calculation of other operating conditions as part of this analysis. The operating conditions in both examples are calculated rather than measured since the determination of UIS capability using measured values for $I_{AV}$ and $t_{AV}$ seemed trivial and self explanatory. The first example is a "single" pulse stress with sufficient time between stresses so that there is no interaction between subsequent pulses. The second has a period short enough that the temperature variation over a period is small.

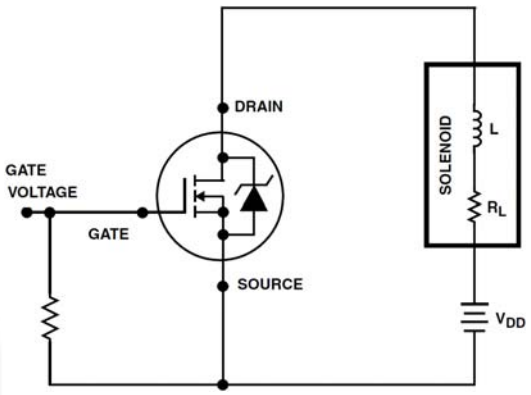


**Figure 2. Schematic**

Solenoid Driver: Single Pulse
Given: $V_{DD}$=13.4V
$R_L$=1.25Ω
Pulse width=Steady state ON
Transistor=FDB8444, $R_{DS(ON)}$=5.5mΩ
Gate "on" drive=10V
Maximum $T_J$=150°C
$T_A$=110°C

**Calculate**: L (Maximum allowable inductance)
$\theta_{CA}$ (Required case-to-ambient thermal resistance)

$R_{TOTAL}=R_L + R_{DS(ON)}$=1.25 + (0.0055 x 1.67) *(see Figure 3 for the 150C $r_n$ multiplication factor)*
$R_{TOTAL}$=1.259Ω
$I_{AVALANCHE}$=213.4/1.259=10.64A (peak avalanche current)

Using the guideline that the avalanche voltage is equal to the rated breakdown rating multiplied by 1.3:

$V_{AVALANCHE}$=40 x 1.3=52V
$t_{AVALANCHE}=(L/ R_{TOTAL}) \times \ln[(I_{AV} \times R_{TOTAL})/(V_{AV} - V_{DD}) +1]$
$t_{AVALANCHE}=(L/1.259) \times \ln[(10.64 \times 1.259)/(52 – 13.4) +1]$
$L=t_{AVALANCHE} /0.237$

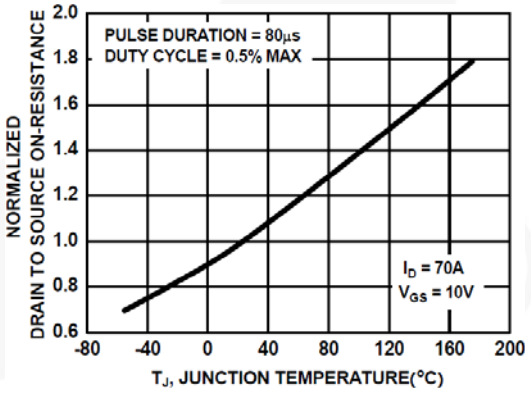


**Figure 3. FDB8444 Normalized $I_{DS(ON)}$ vs. Junction Temperature**

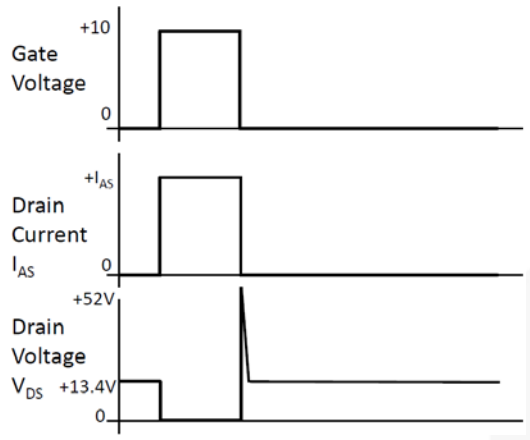


**Figure 4. Single UIS Event Waveform**

Referring to the FDB8444 UIS chart (*see Figure 1*) at 150°C and for $I_{AS}$=10.64A, read an allowable $t_{AVALANCHE}$ of 2ms. This gives a maximum allowable L of:

$$L = (0.002)/0.237 = 8.45mH \quad (1)$$

where L= maximum allowable inductance

Now to calculate the required heat sink thermal resistance:

$$P_D = (I^2 \times R_{DS(ON)}) = (10.06^2) \times (0.0055 * 1.67) = 1.04W \quad (2)$$

$$\Theta_{CA} = [T_{JMAX} - P_D \times \Theta_{JC} - T_A]/P_D \quad (3)$$

$$\Theta_{CA} = [150 - (1.04 \times 0.9) - 110]/1.04 \quad (4)$$

where required case to ambient thermal resistance.

$$\Theta_{CA} = 37.6°C/W \quad (5)$$

**Example 2**

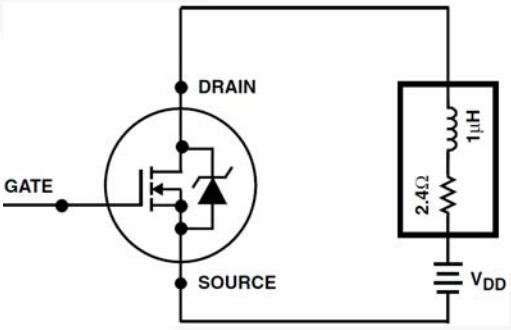


**Figure 5. Schematic**

Switching Regulator =100kHz
Given:
Frequency=100kHz
Duty Cycle=50%
$R_L$=2.4Ω
$V_{DD}$=13.4V
$T_A$=110°C
$T_{JUNCTION}$=150°C maximum junction temperature objective
L=1µH (leakage inductance)
PowerMOS transistor=FDB8444 (rated $T_J$ is 175°C).

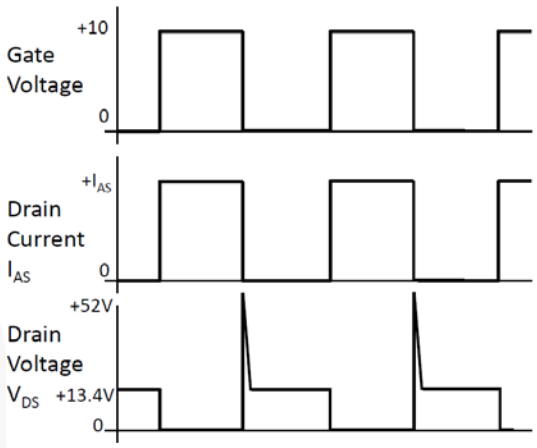


**Figure 6. Repetitive UIS Waveform**

**Determine:**
Is the PowerMOS transistor within UIS rating?
What $\theta_{CA}$ is required?
$I_{AVALANCHE}=V_{DD}/(R_L + R_{DS(ON)})$
$I_{AVALANCHE}$=13.4/(2.4 +(0.0055 x 1.67)) (*see Figure 3 for the 150C $r_n$ multiplication factor*)
$I_{AVALANCHE}$=5.56A
$t_{AVALANCHE}=(L/(R_L + r_{DS(ON)}) \times \ln[(I_{AV} \times (R_L + R_{DS(ON)}))/V_{AV} - V_{DD}) +1]$
$t_{AVALANCHE}$=(1E-6/2.409) x ln[5.34 x 2.409/(52 – 13.4) +1]
$t_{AVALANCHE}$=0.124µs
Referring to the FDB8444 UIS chart (*see Figure 1*) at 5.56A, device has a $t_{AVALANCHE}$ capability at 150°C of 7.5ms. This application does not challenge the UIS capability of the FDB8444.

Calculate the required heat sink thermal resistance:

$E_{AVALANCHE}=(V_{AVALANCHE} \times I_{AVALANCHE} \times t_{AVALANCHE}) /2$
$E_{AV}$=((40 x 1.3) x 5.34 x (0.119µ))/2
$E_{AV}$=17.9µJ per avalanche
$P_{AVALANCHE}=E_{AVALANCHE}$ x frequency
$P_{AVALANCHE}$=17.9µ x 100K
$P_{AVALANCHE}$=1.78W
$P_{CONDUCTION}=(I_{AV}^2 \times R_{DS(ON)}))/2$
$P_C=((5.56)^2 \times 0.00919)/2$
$P_C$=0.14W
$P_{TOTAL}=P_{AV} + P_C$
$P_{TOTAL}$=1.78 + 0.14
$P_{TOTAL}$=1.93W
$\theta_{CA}=[T_{JMAX} - (P_{TOTAL} \times \theta_{JC}) - T_A]/P_{TOTAL}$
$\theta_{CA}$=[150 - (1.93 x 0.9) - 110]/1.93
$\theta_{CA}$=19.8°C/W as a heatsink requirement.

## Application to Other Circuits

Usually the designer has carefully determined the temperature of the devices over the entire range of operating conditions. Using only the junction temperature of the device at the start of a UIS pulse, the duration of the pulse, and the current level of the pulse; the designer can determine whether or not the application exceeds the UIS rating of the device. These quantities are easily measured or calculated. By superposition, this rating can be applied to multiple or repetitive pulses as illustrated in the two examples shown. Any circuit can be analyzed for UIS stress using this approach. There is no need for a separate repetitive UIS rating.

## Thermal Modeling

Avalanche waveforms in operating waveforms often have avalanche currents of variable amplitudes and repetition rates. Thermal analysis of such waveforms often requires more sophisticated analysis methods to adequately estimate operating junction temperature. A reasonable estimate of the PowerMOS transistor junction temperature may be obtained with the use of circuit simulation software, the device thermal impedance model, the heatsink thermal impedance model (or a reasonable estimate of the PowerMOS transistor case temperature), and operating waveforms.

Measurement of semiconductor thermal response involves a calibrated power pulse. Power dissipated within a device causes a junction temperature rise because of the thermal impedance from the die and package. Expression $Z_{\theta JC}(t)$ describes thermal impedance as the result of a change in junction temperature divided by power dissipation.

$$Z_{\theta JC}(t) = \frac{\Delta T_J(t)}{P_D} = \frac{T_J(t) - T_J(0)}{P_D} \quad (6)$$

A basic semiconductor thermal model and its electrical analogue are shown in Figure 7. Heat is generated at the device junction, flows through the silicon to the case, and finally to the heat sink.

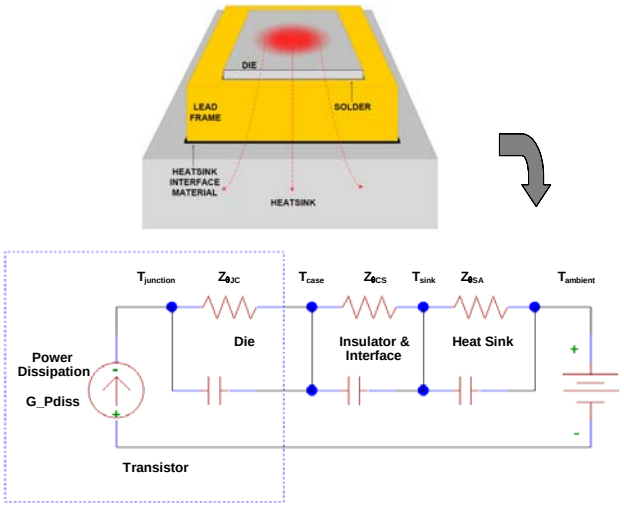


**Figure 7. Semiconductor Thermal Impedance Model**

Junction temperature information is determined by the inclusion of the device's thermal network $Z_{\theta JC}$ and current source *G_PDISS*. *G_PDISS* is the semiconductor's instantaneous operating loss and expresses the result in the form of a current. This is a circuit form representation of the junction temperature as expressed as:

$$T_J = T_{ambient} + G\_Pdiss \bullet (Z_{\theta JC} + Z_{\theta CS} + Z_{\theta SA}) \quad (7)$$

where:

$T_J$ = junction temperature

$G\_P_{diss}$ = instantaneous power loss

$Z_{\theta JC}$ = thermal impedance junction-to-case

$Z_{\theta CS}$ = thermal impedance case-to-heat sink

$Z_{\theta SA}$ = thermal impedance heat sink-to-ambient.

The unit conversion for the electrical analogy of the thermal system is listed in Table 1. $Z_{\theta JC}$ is provided in manufacturer datasheets using the single-pulse normalized thermal impedance curve as in Figure 8. $Z_{\theta JC}$ may be represented using an equivalent electrical analogy model as in Figure 9.

**Table 1. Electrical / Thermal Analogy**

| Electrical | Thermal |
|---|---|
| Ω Resistance | °C/Watt (Thermal Resistance) |
| Farad (Capacitance) | Joules/°C (Thermal Capacitance |
| Amp. (Current) | Watt (Power) |
| Volt (Voltage) | °C (Temperature) |

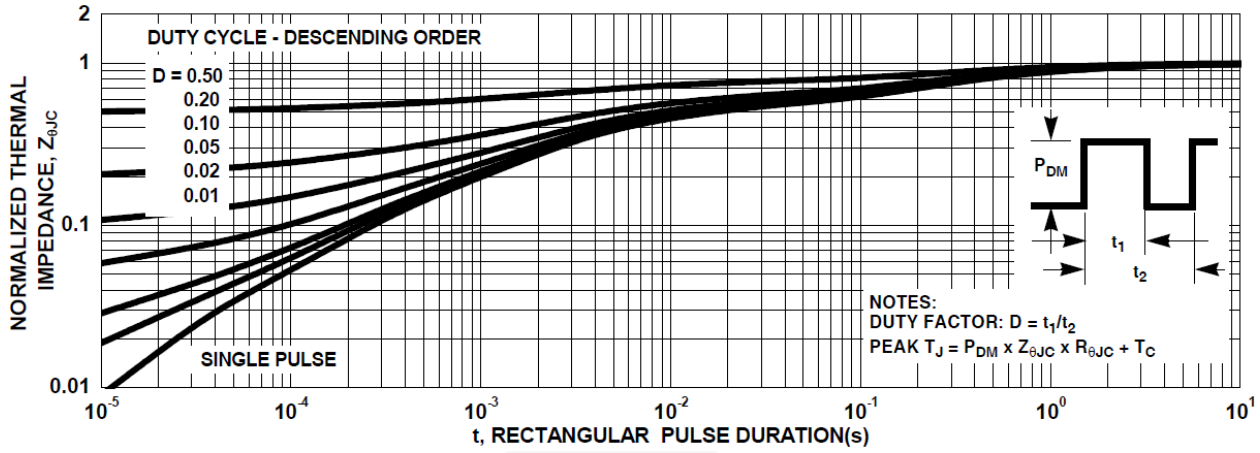


**Figure 8. FSB8444 Normalized Transient Thermal Impedance Curve**

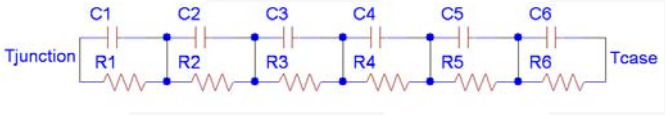


**Figure 9. ZΘJC Thermal Impedance Model Structure**

When thermal model parameters are unavailable, they may be derived from the datasheet $\theta_{JC}$ and by extracting data points from the single-pulse normalized thermal transient impedance curve. The electrical analog model may be expressed as:

$$Z(t) = R_1 \cdot (1 - e^{\frac{-t}{R_1 \cdot C_1}}) + \ldots + R_6 \cdot (1 - e^{\frac{-t}{R_6 \cdot C_6}}) \quad (8)$$

R-C parameters may be found by using curve fitting software such as TableCurve 2D®[5].

Knowing operating waveforms and system-level thermal impedance information, thermal response to complex waveforms may be analyzed. An example circuit and simulation result for an FDB8444 MOSFET at a case temperature of 125°C driving a 1mH/0.6Ω solenoid operated under repetitive avalanche during PowerMOS turn-off is shown in Figure 10. Although average power dissipation is within the 175°C device operating temperature rating (Figure 11), peak temperature excursions during avalanche exceed the maximum rating and could result in degrade a operating life of the transistor.

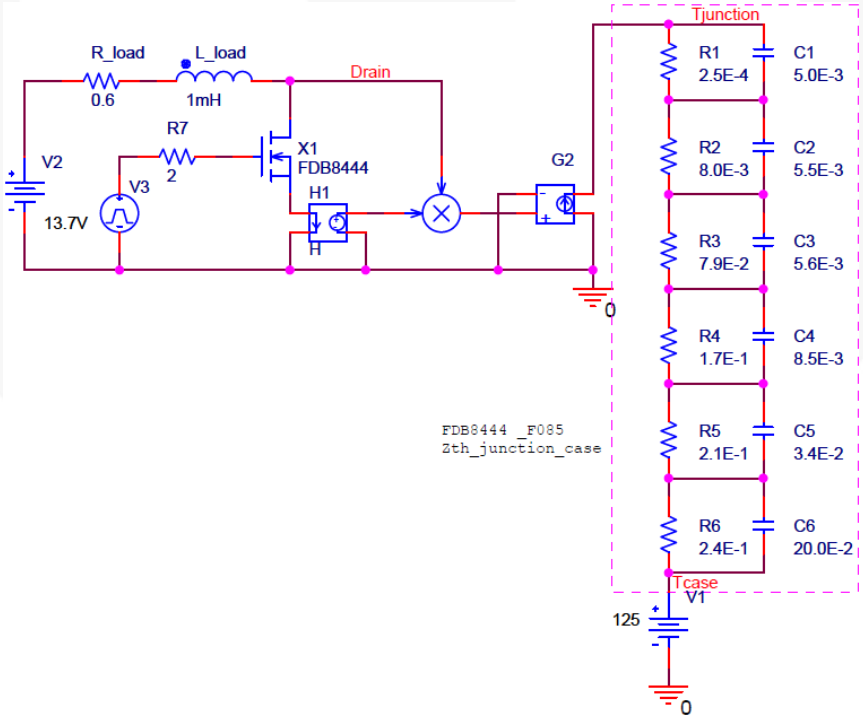


**Figure 10. Electrical Analogy of System Losses**

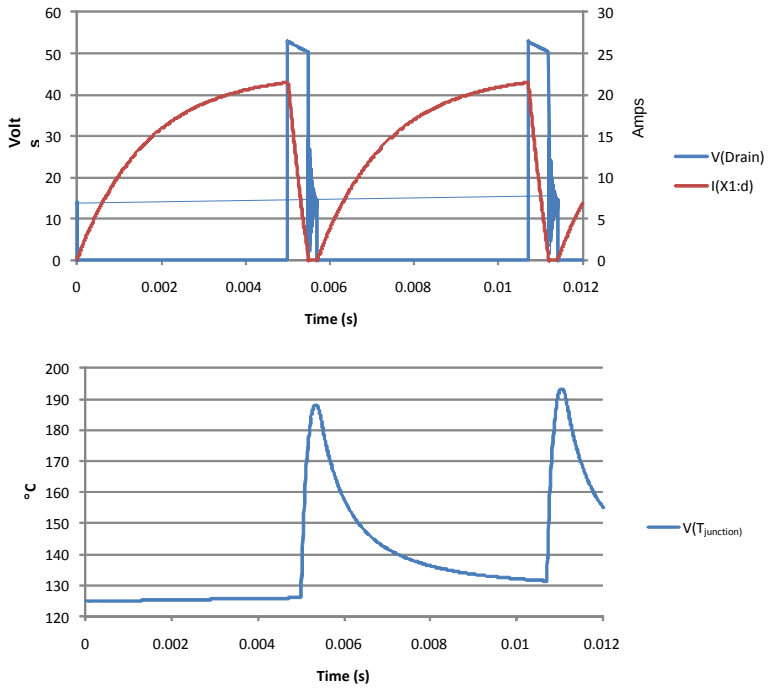


**Figure 11. Simulation Results**

The FDB8444 MOSFET thermal impedance model is provided by an RC ladder network (R1-R6, C1-C6). Instantaneous power dissipation information is evaluated by multiplying the MOSFET current I(H1) by the drain voltage. The resulting power pulse is represented as a voltage waveform that is then converted as an electrical analogy of the power thermal pulse by current source G2. Case temperature is set with voltage source V1. A more detailed system-level thermal impedance network could be implemented in place of V1. Instantaneous junction temperature information is represented at node $T_J$.

## Summary

Thermal analysis methods for simple and complex repetitive UIS events were described. Reasonable junction temperature estimates can be made given single-pulse UIS datasheet rating curves, PowerMOS thermal impedance models, and an analytical understanding of the transistor ambient operating condition.

## References

*For Fairchild documents available on the internet, see web site http://www.fairchildsemi.com*

[1] D.L. Blackburn, *"Turn-off Failure of Power MOSFETS,"* Proc. 1985 IEEE Power Electronics Specialists Conference, pp 429-435, June, 1985.

[2] Rodney R. Stoltenburg, *"Boundary of Power-MOSFET Unclamped Inductive Switching (UIS) Avalanche Current Capability,"* Proc. 1989 Applied Power Electronics Conference, pp 359-364, March 1989.

[3] Harold R. Ronan, *"Rating System Compares Single Pulse Unclamped Inductive Switching for MOSFETS,"* Power Conversion and Intelligent Motion, pp 32-40, September 1991.

[4] Fairchild Semiconductor Corporation, Datasheet FDB8444, http://www.fairchildsemi.com.

[5] http://www.systat.com/products/TableCurve2D/

[6] Fairchild Semiconductor Corporation, *"Single Pulse Unclamped Inductive Switching: A Rating System", Application Note AN7514*", http://www.fairchildsemi.com.