General Description

The MAX17047/MAX17050 incorporate the Maxim ModelGauge™ m3 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. ModelGauge m3 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m3 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time.

The device automatically compensates for aging, temperature, and discharge rate and provides accurate state of charge (SOC) in mAh or %, as well as time-to-empty over a wide range of operating conditions. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer.

The device provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire (I^2C) interface provides access to data and control registers. The MAX17047 is available in a lead(Pb)-free, 3mm x 3mm, 10-pin TDFN package. The MAX17050 is available in a 0.4mm pitch 9-bump WLP package.

Applications

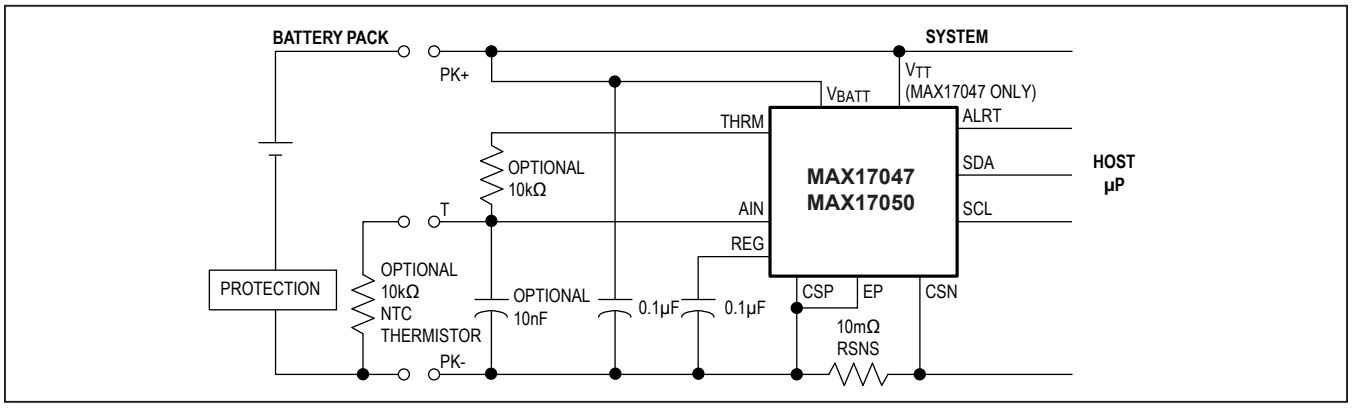
- Smartphones, Tablets
- Health and Fitness Monitors
- Digital Still, Video and Action Cameras
- Medical Devices
- Handheld Computers and Terminals
- Wireless Speakers

Features

- Accurate Battery-Capacity and Time-To-Empty Estimation
  - Temperature, Age, and Rate Compensated
  - Does Not Require Empty, Full, or Idle States to Maintain Accuracy
- Precision Measurement System
  - No Calibration Required
- ModelGauge m3 Algorithm
  - Long-Term Influence by Voltage Fuel Gauge Cancels Coulomb-Counter Drift
  - Short-Term Influence by Coulomb Counter Provides Excellent Linearity
  - Adapts to Cell Characteristics
- External Temperature-Measurement Network
  - Actively Switched Thermistor Resistive Divider Reduces Current Consumption
- Low Quiescent Current
  - 25µA Active, < 0.5µA Shutdown
- Alert Indicator for SOC, Voltage, Temperature, and Battery Removal/Insertion Events
- AtRate Estimation of Remaining Capacity
- 2-Wire (I^2C) Interface
- Tiny, Lead(Pb)-Free, 3mm x 3mm, 10-Pin TDFN Package or Tiny 0.4mm Pitch 9-Bump WLP Package

***Ordering Information* appears at end of data sheet.**

Simple Fuel-Gauge Circuit Diagram



ModelGauge is a trademark of Maxim Integrated Products, Inc.

Absolute Maximum Ratings

V_{BATT}, SDA, SCL, ALRT to CSP .....-0.3V to +6V
REG to CSP .....-0.3V to +2.2V
V_{TT} to CSP.....-0.3V to +6V
THRM, AIN to CSP.....-0.3V to (V_{TT} + 0.3V)
CSN to CSP .....-2V to +2V
Continuous Sink Current (V_{TT}) 20mA
Continuous Sink Current (SCL, SDA, ALRT).....20mA

Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C above +70°C).....1951.2mW
WLP (derate 11.9mW/°C above +70°C).....952.0mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....84°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BATT} = 2.5V to 4.5V, **T_A = -20°C to +70°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{BATT}	(Note 3)	2.5		4.5	V
Supply Current	I_{DD0}	Shutdown mode, $T_A \le$ +50°C		0.5	2	µA
	I_{DD1}	Active mode, average current		25	42	
REG Regulation Voltage	V_{REG}		1.5		1.9	V
Measurement Error, V_{BATT}	V_{GERR}	T_A = +25°C	-7.5		+7.5	mV
			-20		+20	
Measurement Resolution, V_{BATT}	V_{LSb}			0.625		mV
V_{BATT} Measurement Range	V_{FS}		2.5		4.98	V
Input Resistance CSN, AIN			15			MΩ
Ratiometric Measurement Accuracy, AIN	T_{GERR}		-0.5		+0.5	%
Ratiometric Measurement Resolution, AIN	T_{LSb}			0.0244		% Full Scale
Current Register Resolution	I_{LSb}			1.5625		µV
Current Full-Scale Magnitude	I_{FS}			±51.2		mV
Current Offset Error	I_{OERR}			±1.5		µV
Current Gain Error	I_{GERR}		-1		+1	% of Reading
Time-Base Accuracy	t_{ERR}	V_{DD} = 3.6V at T_A = +25°C	-1		+1	%
		T_A = 0°C to +50°C	-2.5		+2.5	
		T_A = -20°C to +70°C	-3.5		+3.5	

Electrical Characteristics (continued)

(V_{BATT} = 2.5V to 4.5V, **T_A = -20°C to +70°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THRM Output Drive		I_{OUT} = 0.5mA	V_{TT} - 0.1			V
THRM Precharge Time	t_{PRE}		8.48			ms
SDA, SCL, ALRT Input Logic High	V_{IH}		1.5			V
SDA, SCL, ALRT Input Logic Low	V_{IL}				0.5	V
SDA, ALRT Output Logic Low	V_{OL}	I_{OL} = 4mA			0.4	V
SDA, ALRT Pulldown Current	I_{PD}	Active mode, V_{SDA} = 0.4V, V_{ALRT} = 0.4V	0.05	0.2	0.4	µA
ALRT Leakage					1	µA
THRM Operating Range			2.5		V_{TT}	V
Battery-Removal Detection Threshold—V_{AIN} Rising	V_{DETR}	V_{THRM} - V_{AIN}	40	125	200	mV
Battery-Removal Detection Threshold—V_{AIN} Falling	V_{DETF}	V_{THRM} - V_{AIN}	70	150	230	mV
Battery-Removal Detection Comparator Delay	t_{TOFF}	V_{AIN} step from 70% to 100% of V_{THRM} to ALRT falling; Alrtp = logic 0; EnAIN = logic 1; FTHRM = logic 1			100	µs
External AIN Capacitance		R_{THM} = 10kΩ NTC			100	nF

Electrical Characteristics (2-Wire Interface)

(2.5V ≤ V_{BATT} ≤ 4.5V, **T_A = -20°C to +70°C**.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 4)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 6, 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 6)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns

Electrical Characteristics (2-Wire Interface) (continued)

(2.5V ≤ V_{BATT} ≤ 4.5V, **T_A = -20°C to +70°C**.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 2: Specifications are 100% tested at T_A = +25°C. Limits over the operating range are guaranteed by design and characterization.
Note 3: All voltages are referenced to CSP.
Note 4: Timing must be fast enough to prevent the device from entering shutdown mode due to bus low for a period > 45s minimum.
Note 5: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 6: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 7: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the minimum VIH of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 9: C_B—total capacitance of one bus line in pF.

I²C Bus Timing Diagram

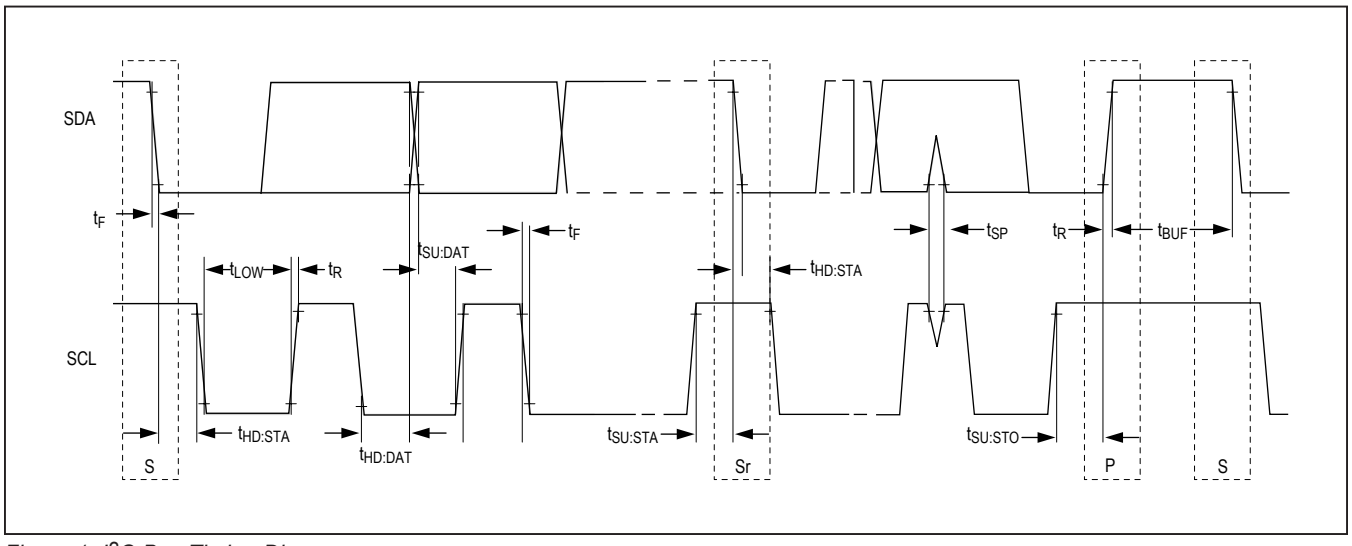
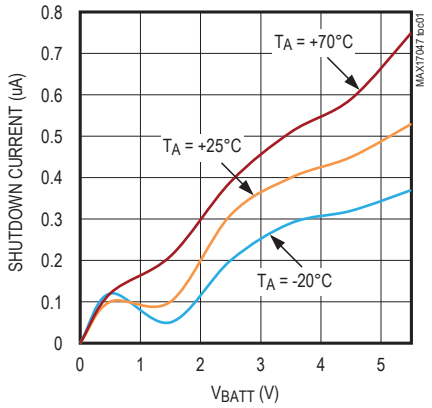


Figure 1. I²C Bus Timing Diagram

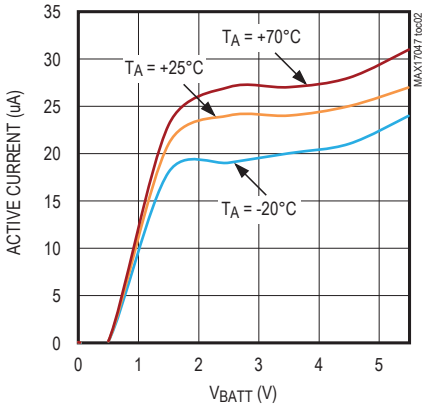
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

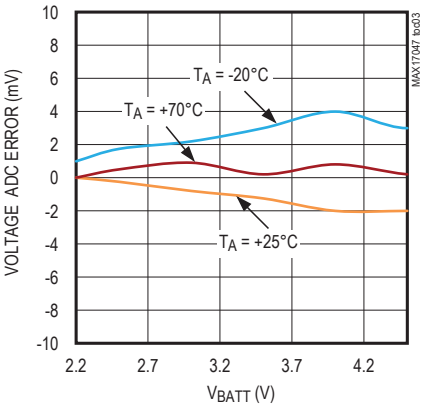
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



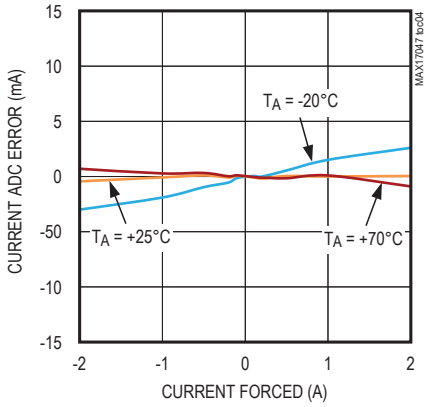
ACTIVE CURRENT vs. SUPPLY VOLTAGE



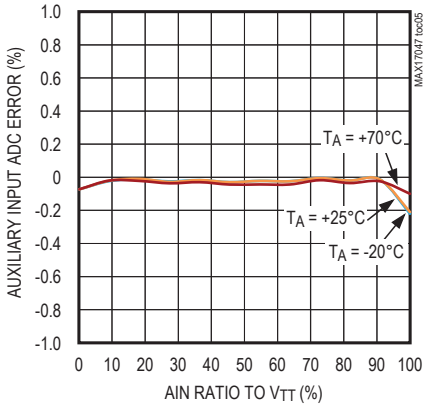
VOLTAGE ADC ERROR vs. TEMPERATURE AND SUPPLY VOLTAGE



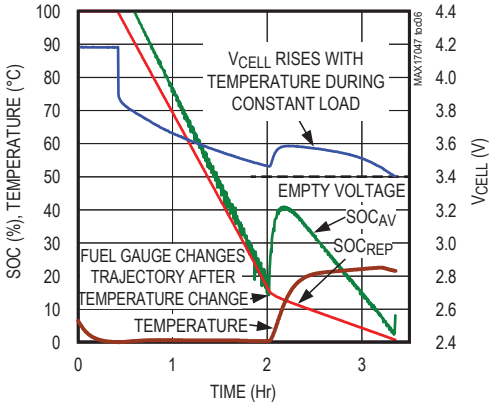
CURRENT ADC ERROR vs. TEMPERATURE



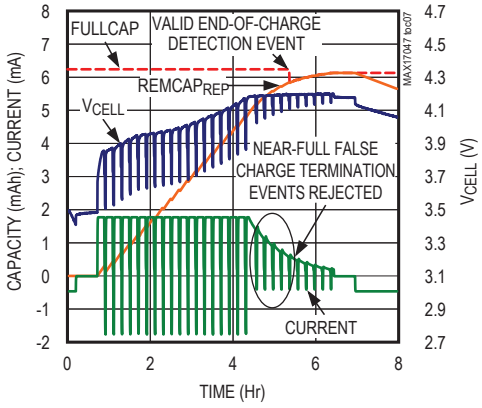
AUXILIARY INPUT ADC ERROR vs. TEMPERATURE



RESPONSE TO TEMPERATURE TRANSIENT AT CONSTANT-CURRENT LOAD



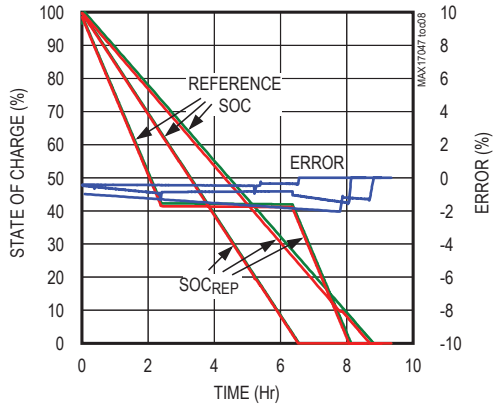
END OF CHARGE DETECTION



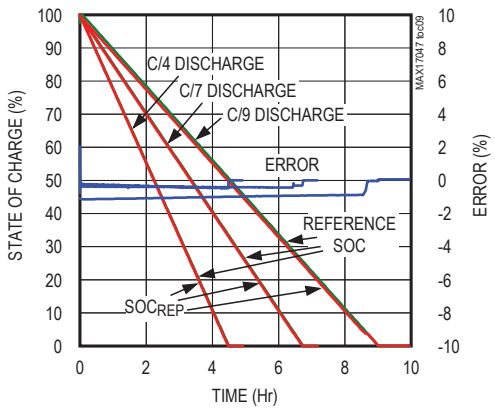
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

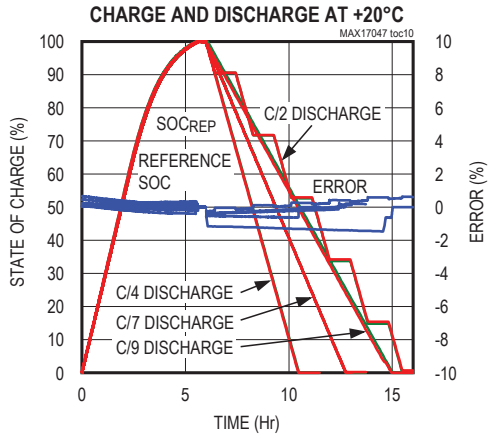
COLD DISCHARGE (0°C)



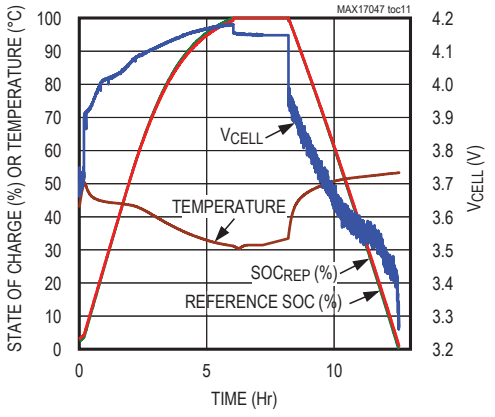
DISCHARGE AT +40°C



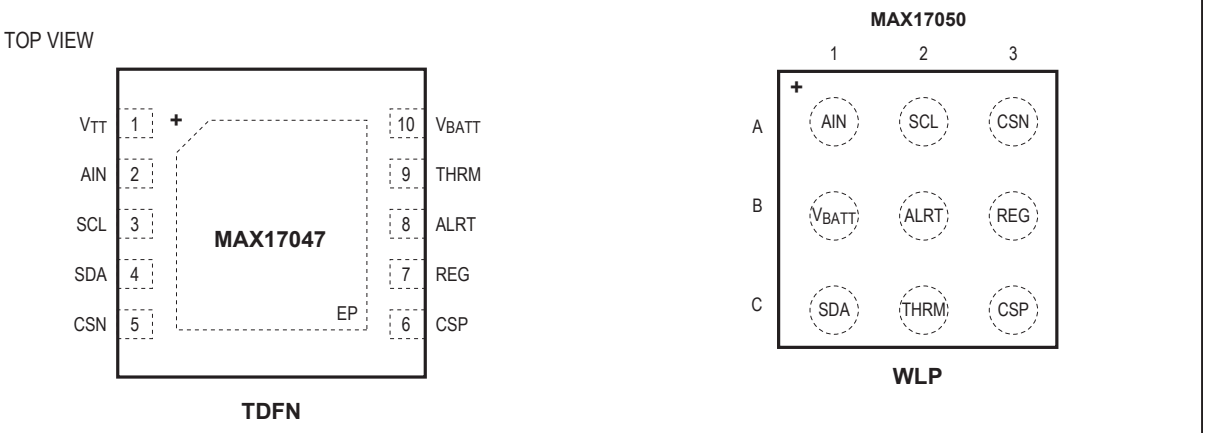
CHARGE AND DISCHARGE AT +20°C



CHARGE AND DISCHARGE IN ACTUAL SYSTEM



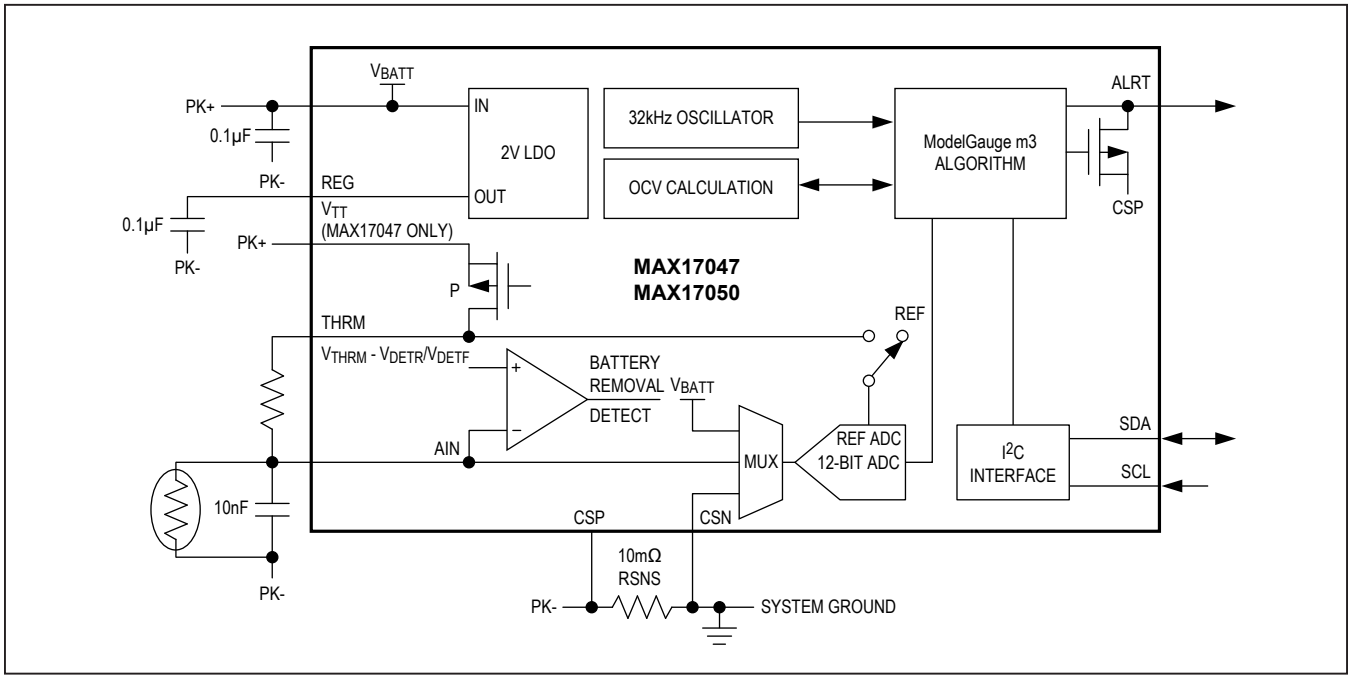
Pin/Bump Configurations



Pin/Bump Descriptions

PIN TDFN	BUMP WLP	NAME	FUNCTION
1	—	V_{TT}	Supply Input for Thermistor Bias Switch (MAX17047 Only.) V_{TT} is connected internally to V_{BATT} on the MAX17050. Connect to supply for ratiometric AIN pin-voltage measurements. In most applications, connect V_{TT} to V_{BATT}.
2	A1	AIN	Auxiliary Voltage Input. Auxiliary voltage input from external thermal-measurement network. AIN also provides battery insertion/removal detection. Connect to V_{BATT}, if not used.
3	A2	SCL	Serial Clock Input. 2-wire clock line. Input only.
4	C1	SDA	Serial Data Input/Out. 2-wire data line. Open-drain output driver.
5	A3	CSN	Sense Resistor Connection. System ground connection and sense resistor input.
6	C3	CSP	Chip Ground and Sense Resistor Input
7	B3	REG	Voltage Regulator Bypass. Connect a 0.1µF capacitor from REG to CSP.
8	B2	ALRT	Alert Indication. An open-drain n-channel output used to indicate specified condition thresholds have been met. A 200kΩ pullup resistor to power rail is required for use as an output. Alternatively, ALRT can operate as a shutdown input with the output function disabled.
9	C2	THRM	Thermistor Bias Connection. Supply for thermistor resistor-divider. Connect to the high side of the thermistor/resistor-divider. THRM connects internally to V_{TT} during temperature measurement.
10	B1	V_{BATT}	Power-Supply and Battery Voltage-Sense Input. Kelvin connect to positive terminal of battery pack. Bypass with a 0.1µF capacitor to CSP.
—	—	EP	Exposed Pad (TDFN Only). Connect to CSP.

Block Diagram



Detailed Description

The MAX17047/MAX17050 incorporate the Maxim ModelGauge m3 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. ModelGauge m3 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m3 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time.

The device automatically compensates for aging, temperature, and discharge rate and provides accurate state-of-charge (SOC) in mAh or % over a wide range of operating conditions. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer.

The device provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire (I^2C) interface provides access to data and control registers. The MAX17047 is available in a 3mm x 3mm, 10-pin TDFN package. The MAX17050 is available in a 0.4mm pitch 9-bump WLP package.

ModelGauge m3 Algorithm

The ModelGauge m3 algorithm combines a high-accuracy coulomb counter with a voltage fuel gauge (VFG) as represented in Figure 2.

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causes the reported capacity error to increase over time, and requires periodic corrections. Corrections are usually performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the SOC based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over

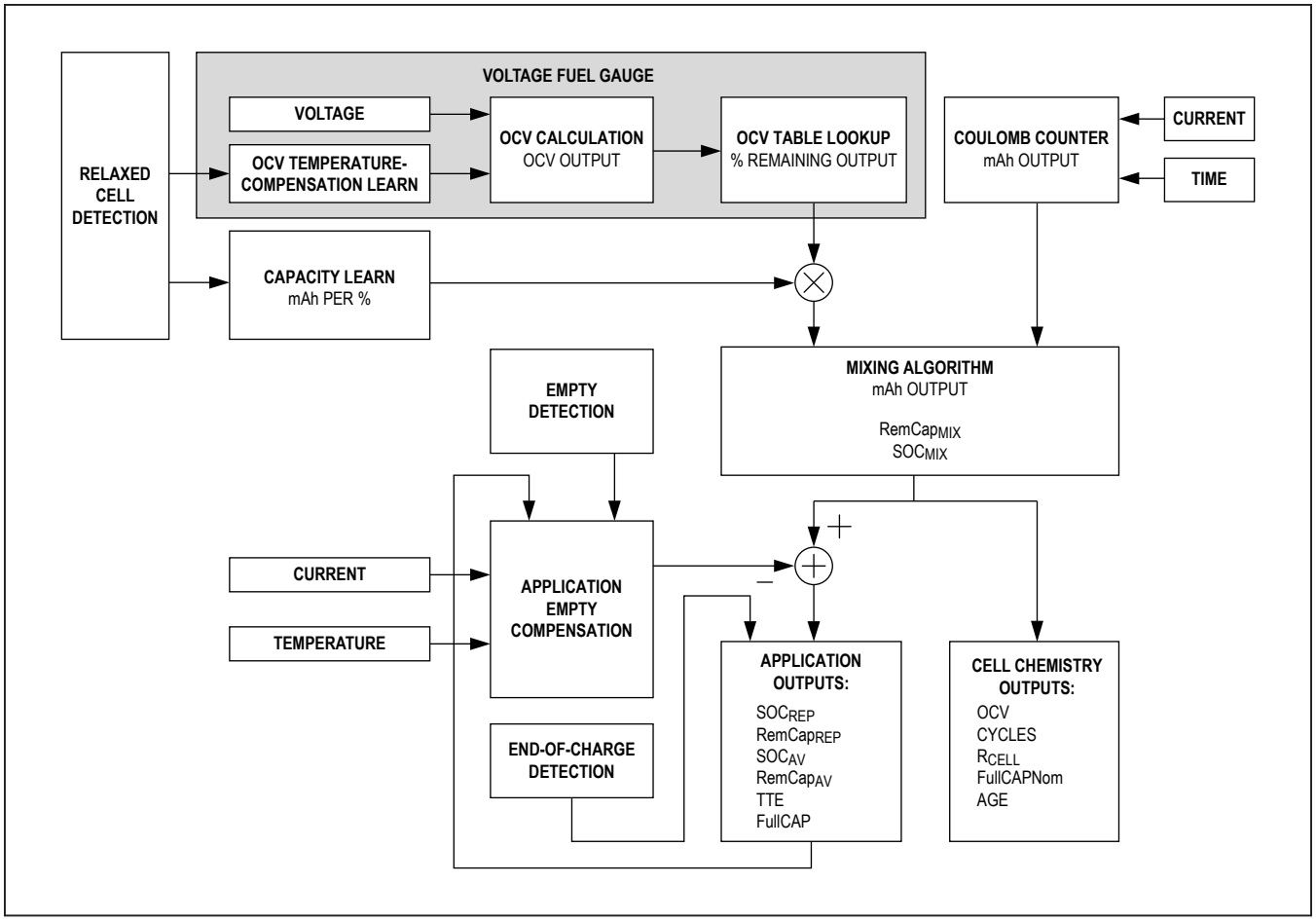


Figure 2. ModelGauge m3 Overview

time in the actual application, the error in the system is **boundless**. The performance of classic coulomb counters is dominated by the accuracy of such corrections.

Classical voltage-measurement-based SOC estimation has poor accuracy due to inadequate cell modeling, but does not accumulate offset error over time.

The device includes an advanced VFG, which estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a lithium-ion (Li+) battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC based on table lookup. This SOC estimation does not accumulate offset error over time.

The ModelGauge m3 algorithm combines a high-accuracy coulomb counter with a VFG. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG, while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift.

The ModelGauge m3 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system.

The ModelGauge m3 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the VFG dynamics adapt based on cell-voltage behavior in the application.

OCV Estimation and Coulomb-Count Mixing

The core of the ModelGauge m3 algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the coulomb-count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing. Servo mixing provides a fixed magnitude continuous error correction to the coulomb count, up or down, based on the direction of error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly. See Figure 3.

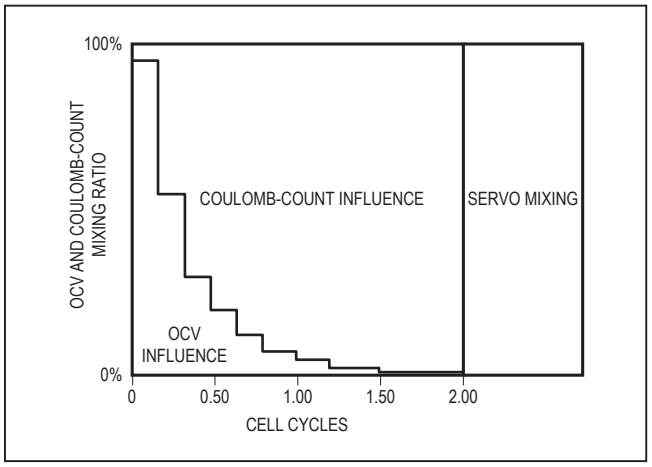


Figure 3. ModelGauge m3 OCV and Coulomb-Count Mixing

The resulting output from the mixing algorithm does not suffer drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm; see Figure 4. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

Fuel-Gauge Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m3 algorithm distinguishes between remaining capacity of the cell ($RemCap_{MIX}$) and remaining capacity of the application ($RemCap_{AV}$) and reports both results to the user.

Fuel-Gauge Learning and Age Support

The device periodically makes internal adjustments to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small undercorrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. To maintain learned accuracy through power loss, the host must periodically save learned information and then restore after power is returned. See the *Power-Up and Power-On Reset* section for details:

- **Full Capacity Available to Application (FullCAP).** This is the total capacity available to the application at full. FullCAP is updated near the end of charging when termination is detected. See the *End-of-Charge Detection* section.

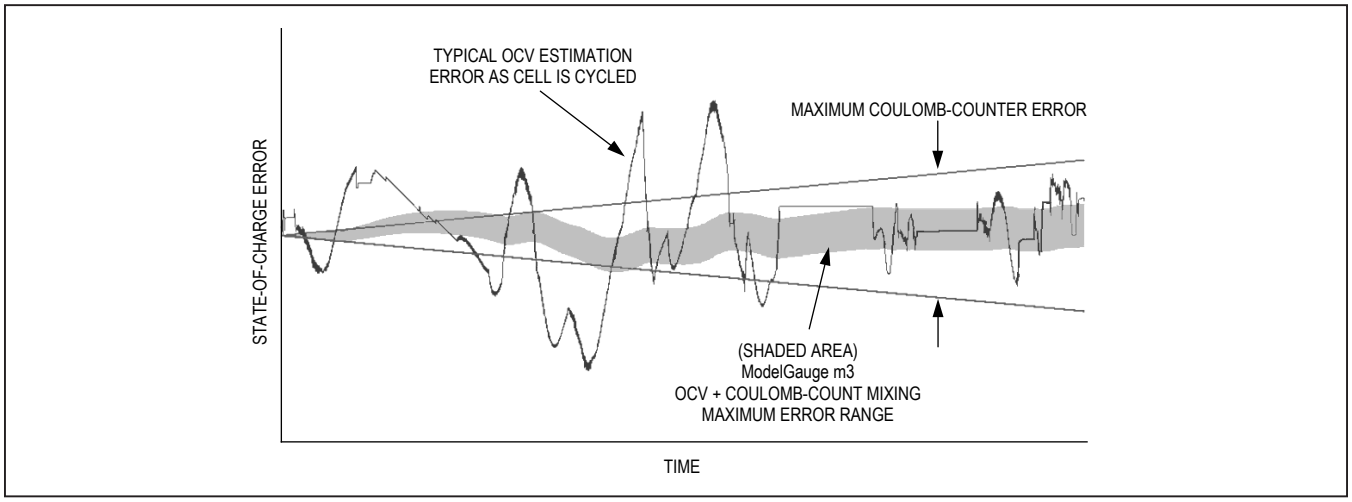


Figure 4. ModelGauge m3 Algorithm Mixing Conceptual Illustration

- **Cell Capacity (FullCapNom).** This is the total cell capacity at full, according to the VFG. This includes some capacity that is not available to the application at high loads and/or low temperature. The device periodically compares percent change based on OCV measurement vs. coulomb-count change as the cell charges and discharges. This information allows the device to maintain an accurate estimation of the cell's capacity in mAh as the cell ages.
- **Voltage Fuel-Gauge Adaptation.** The device observes the battery's relaxation response and adjusts the dynamics of the VFG. This adaptation adjusts the RCOMP0 register during qualified cell relaxation events.
- **Empty Learning.** The device updates internal data whenever cell empty is detected (V_{CELL} < **V_empty**) to account for cell age or other cell deviations from the characterization information. This maintains SOC accuracy as the battery ages.

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge, as experienced by end users, the battery should be exercised in a dynamic manner. The end-user accuracy cannot be understood with only simple cycles.

To challenge a correction-based fuel gauge, such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user may operate the device for 10min and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration. Refer to Application Note 4799: *Cell Characterization Procedure for a ModelGauge m3 Fuel Gauge.*

Initial Accuracy

The device uses the first voltage reading after power-up or after cell insertion to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading; however, this is not always the case. If the cell was recently charged or discharged, the voltage measured by the device may not represent the true state of charge of the cell, resulting in initial error in the fuel gauge outputs. In most cases, this error is minor and is quickly removed by the fuel gauge algorithm during normal operation.

Typical Operating Circuit

The device is designed to mount outside the cell pack that it monitors. Voltage of the battery pack is measured directly at the pack terminals by the V_{BATT} and CSP connections. Current is measured by an external sense resistor placed between the CSP and CSN pins. An external resistor-divider network allows the device to measure temperature of the cell pack by monitoring the AIN pin. The THRM pin provides a strong pullup for the resistor-divider that is internally disabled when temperature is not being measured.

Communication to the host occurs over a standard I²C interface. SCL is an input from the host, and SDA is an open-drain I/O pin that requires an external pullup. The ALRT pin is an output that can be used as an external interrupt to the host processor if certain application conditions are detected. ALRT can also function as an input, allowing the host to shut down the device. This pin is also open drain and requires an external pullup resistor. Figure 5 is the typical operating circuit.

Multicell Circuit

The MAX17047 can be used in multicell pack applications. A resistor-divider network divides the pack voltage down so that the IC monitors the equivalent voltage of a single cell. The MAX9910 buffers the divider output so that loading by the MAX17047 does not affect accuracy. V_{TT} must be connected to a regulated supply in the system to prevent overloading the MAX9910. Contact the factory for a MAX17050 multicell application circuit. See Figure 6.

Thermistor Sharing Circuit

The MAX17047 can share the cell thermistor circuit with the system charger. In this circuit, there is a single thermistor inside the cell pack and a single bias resistor external to the cell pack. The device shares the same external bias as the charger circuit and measurement point on the thermistor. In this configuration, each device can measure temperature individually or simultaneously without interference. Alternatively, if the bias voltage in the charger circuit is not available to the device, a separate bias voltage on the V_{TT} pin can be used. For proper operation, the separate bias voltage must be larger than the minimum operating voltage of the device, but no larger than one diode drop above the charger circuit bias voltage. The MAX17050 cannot be operated in his configuration. See Figure 7.

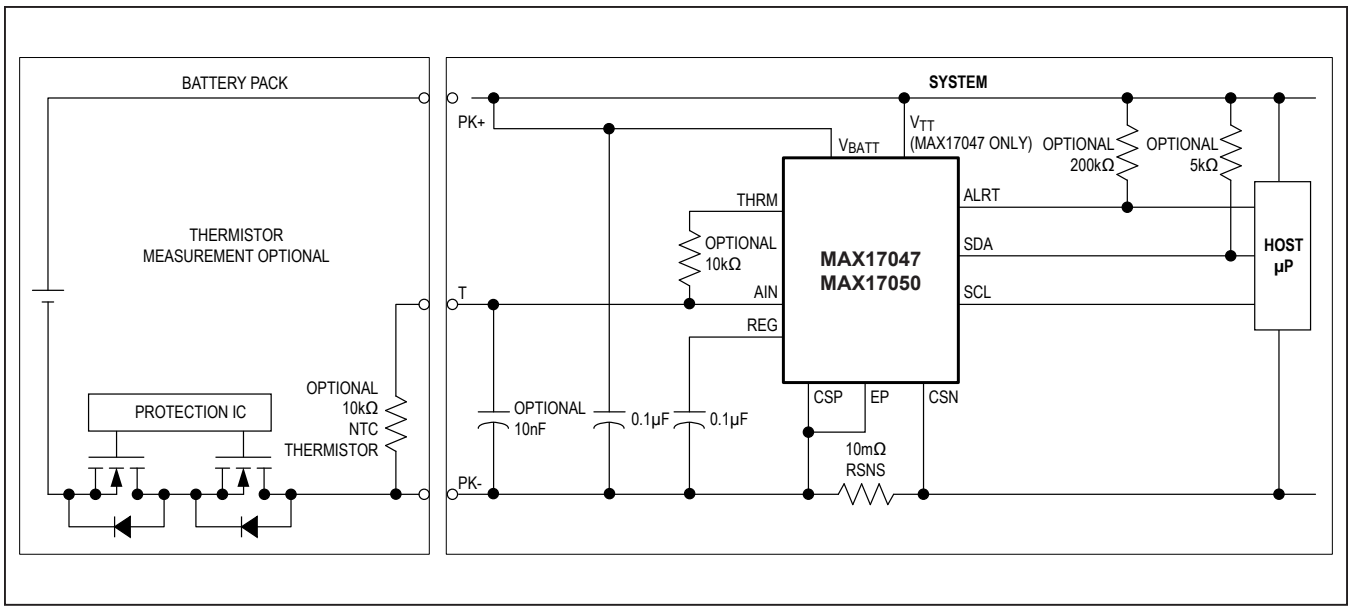


Figure 5. Typical Operating Circuit

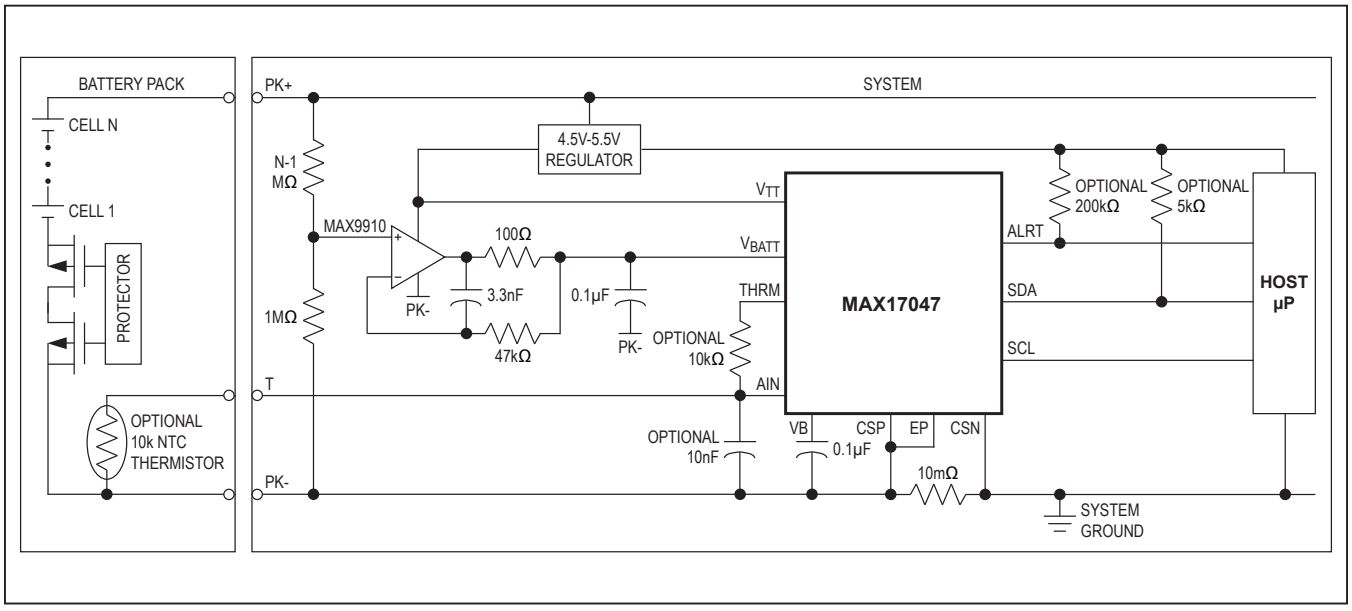


Figure 6. Multicell Application Circuit

Recommended Layout

Proper circuit layout (see Figure 8) is essential for measurement accuracy when using the MAX17047/MAX17050 ModelGauge m3 ICs. The recommended layout guidelines are as follows:

1) Mount R_{SNS} as close as possible to PACK-. The device shares both voltage and current measurements on the CSP pin. Therefore, it is important to limit the amount of trace resistance between the current-sensing resistor and PACK-.
2) V_{BATT} trace should make a Kelvin connection to PACK+. The device shares the V_{BATT} pin for both voltage measurement and IC power. Limiting the voltage loss through this trace is important to voltage-measurement accuracy. PCB resistance that cannot be removed can be compensated for during characterization of the application cell.
3) CSN and CSP traces should make Kelvin connections to R_{SNS}. The device measures current differentially through the CSN and CSP pins. Any shared high-current paths on these traces will affect current-measurement gain accuracy. PCB resistance that cannot be removed can be compensated for during characterization of the application cell.
4) V_{BATT} capacitor trace loop area should be minimized. The device shares the V_{BATT} pin for both voltage measurement and IC power. Limiting noise at the V_{BATT} pin is important to current-measurement accuracy.
5) REG capacitor trace loop area should be minimized. The helps filter any noise from the internal regulated supply.
6) There are no limitations on any other IC connection. Connections to THRM, ALRT, SDA, SCL, V_{TT}, and AIN, as well as any external components mounted to these pins, have no special layout requirements.

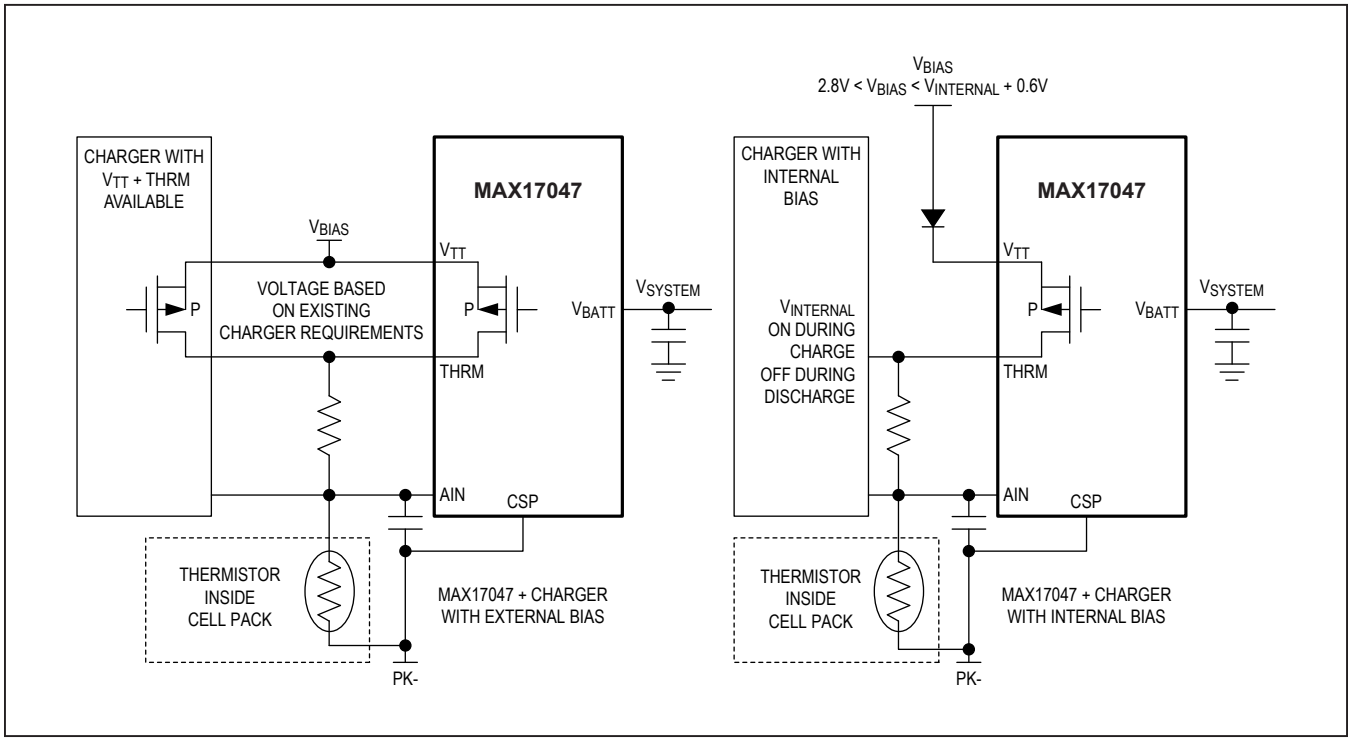


Figure 7. Operating Circuits that Share Pack Thermistor with System Charger

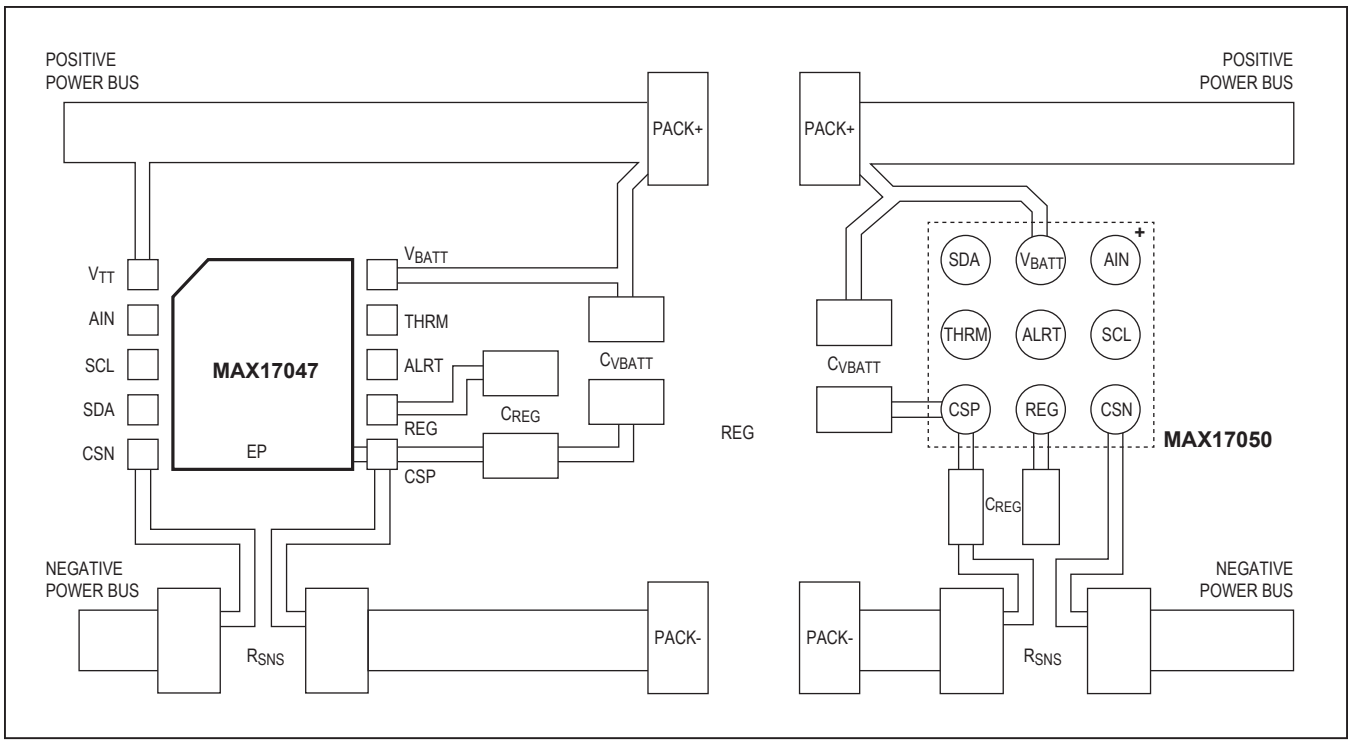


Figure 8. Proper Board Layout

ModelGauge m3 Registers

To calculate accurate results, ModelGauge m3 requires information about the cell, the application, and real-time information measured by the device. Figure 9 shows all inputs and outputs to the algorithm grouped by category. Analog input registers are the real-time measurements of voltage, temperature, and current performed by the device. Application-specific registers are programmed by the customer to reflect the operation of the application. The Cell Characterization Information registers hold characterization data that models the behavior of the cell over the operating range of the application. The Algorithm Configuration registers allow the host to adjust performance of the device for its application. The Save and Restore registers allow an application to maintain accuracy of the algorithm after the device has been power cycled. The following sections describe each register in detail.

ModelGauge Algorithm Output Registers

The following registers hold the output results from the ModelGauge m3 algorithm.

SOC_{MIX} Register (0Dh)

The SOC_{MIX} register holds the calculated present state of charge of the cell before any empty compensation adjustments are performed. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit state-of-charge value is desired, the host can discard the lower byte and use only the upper byte of the register with a resolution of 1.0%. Figure 10 shows the SOC_{MIX} register format.

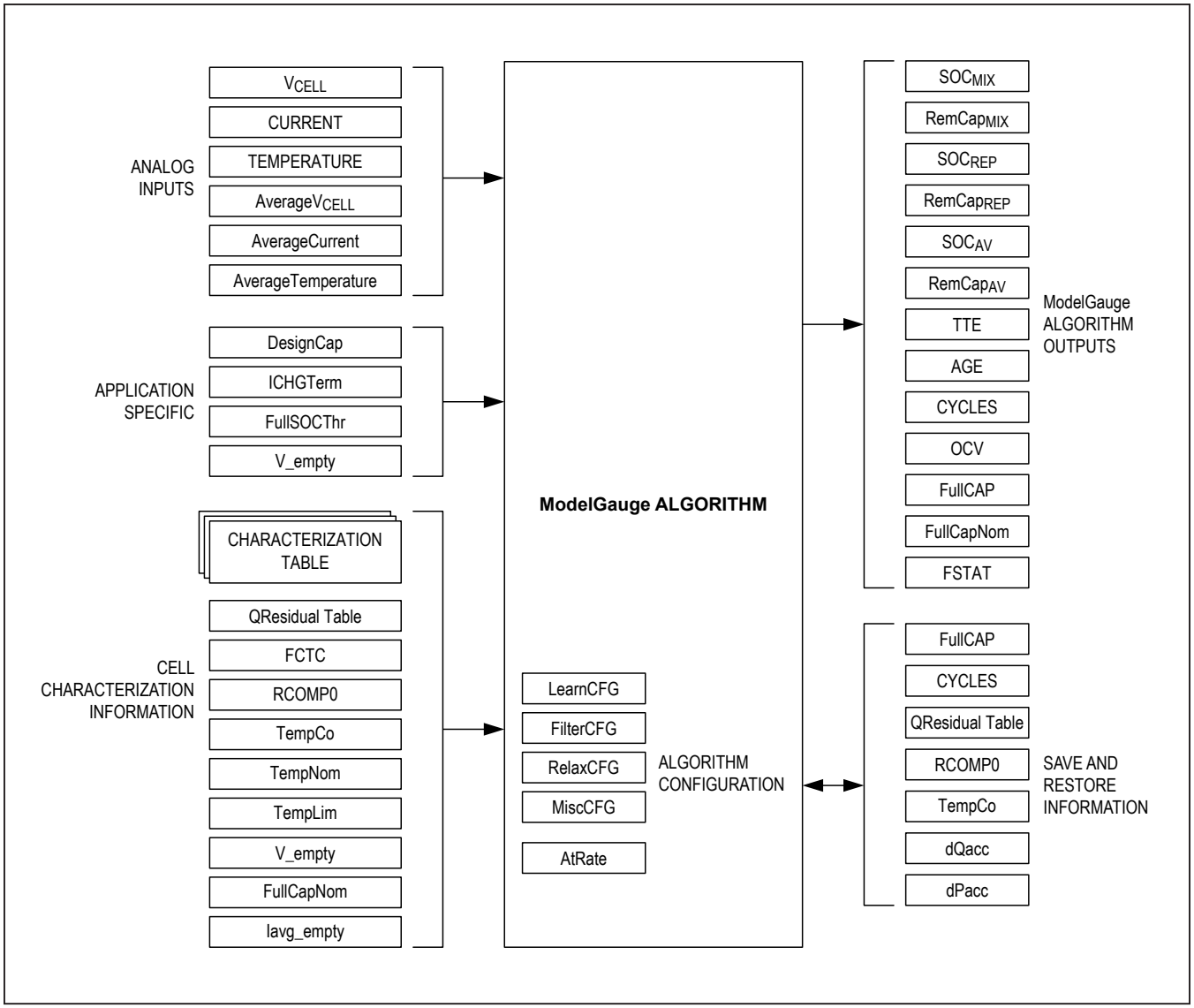


Figure 9. ModelGauge m3 Register Map

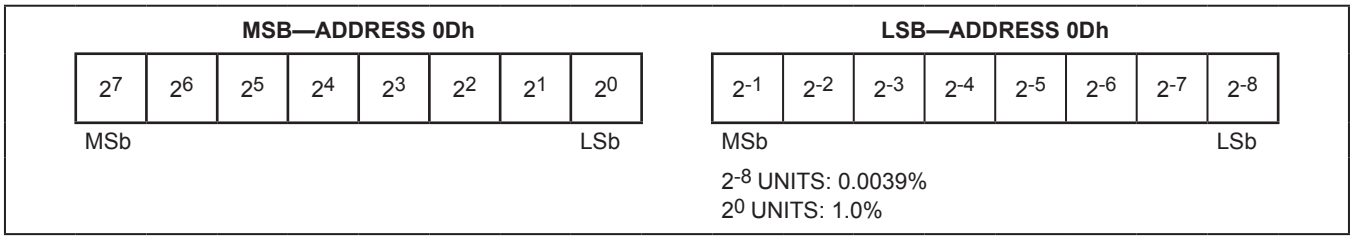


Figure 10. SOC_{MIX} Register Format (Output)

$RemCap_{MIX}$ Register (0Fh)

The $RemCap_{MIX}$ register holds the calculated remaining capacity of the cell before any empty compensation adjustments are performed. The value is stored in terms of µVh and must be divided by the application sense-resistor value to determine remaining capacity in mAh. Figure 11 shows the $RemCap_{MIX}$ register format.

SOC_{REP} Register (06h)

SOC_{REP} is a filtered version of the SOC_{AV} register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit SOC value is desired, the host can discard the lower byte and use only the upper byte of the register with a resolution of 1.0%. Figure 12 shows the SOC_{REP} register format.

$RemCap_{REP}$ Register (05h)

$RemCap_{REP}$ is a filtered version of the $RemCap_{AV}$ register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. The value is stored in terms of µVh and must be divided by the application sense-resistor value to determine remaining capacity in mAh. During application idle periods where the AverageCurrent Register value is less than ±6 LSbs, $RemCap_{REP}$ does not change. The measured current during this period is still accumulated into $RemCap_{MIX}$ and is slowly reflected in $RemCap_{REP}$ once cell loading or charging occurs. Figure 13 shows the $RemCap_{REP}$ register format.

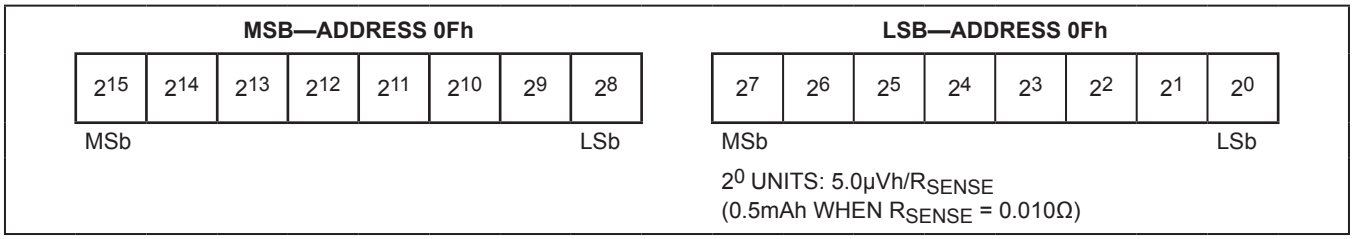


Figure 11. $RemCap_{MIX}$ Register Format (Output)

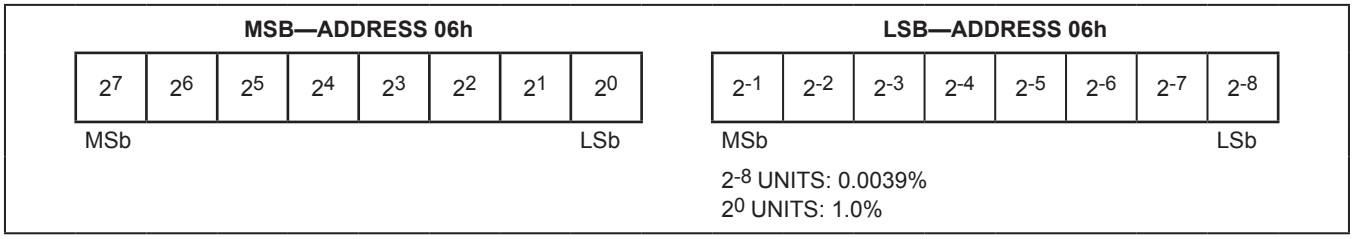


Figure 12. SOC_{REP} Register Format (Output)

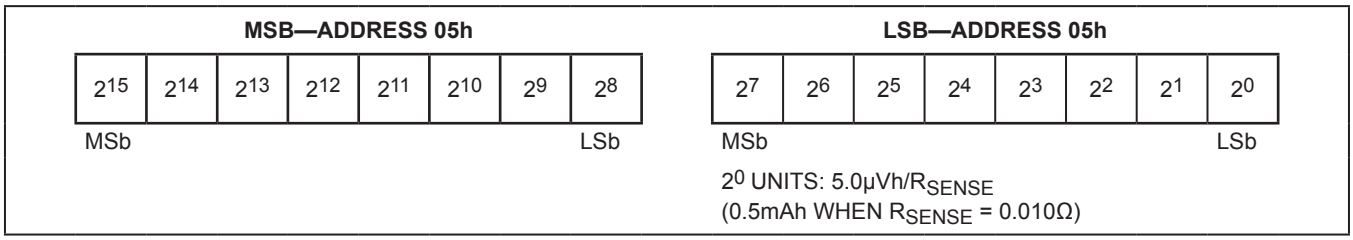


Figure 13. $RemCap_{REP}$ Register Format (Output)

SOC_{AV} Register (0Eh)

The SOC_{AV} register holds the calculated present state of charge of the cell based on all inputs from the ModelGauge m3 algorithm including empty compensation. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit state-of-charge value is desired, the host can discard the lower byte and use only the upper byte of the register with a resolution of 1.0%. The SOC_{AV} register value is an unfiltered calculation. Jumps in the value can be caused by changes in the application such as abrupt changes in load current. Figure 14 shows the SOC_{AV} register format.

$RemCap_{AV}$ Register (1Fh)

The $RemCap_{AV}$ register holds the calculated remaining capacity of the cell based on all inputs from the ModelGauge m3 algorithm including empty compensation. The value is stored in terms of µVh and must be divided by the application sense-resistor value to determine the remaining capacity in mAh. The register value is an unfiltered calculation. Jumps in the value can be caused by changes in the application such as abrupt changes in load current. Figure 15 shows the $RemCap_{AV}$ register format.

SOC_{VF} Register (FFh)

The SOC_{VF} register holds the calculated present SOC of the battery according to the voltage fuel gauge. The register value is stored as a percentage with a resolution of 0.0039% per LSb. If an 8-bit SOC value is desired, the host can discard the lower byte and use only the upper byte of the register with a resolution of 1.0%. Figure 16 shows the SOC_{VF} register format.

TTE Register (11h)

The TTE register holds the estimated time to empty for the application under present conditions. The TTE value is determined by dividing the $RemCap_{AV}$ register by the AverageCurrent register. The result is stored in the TTE register with a resolution of 5.625s per LSb.

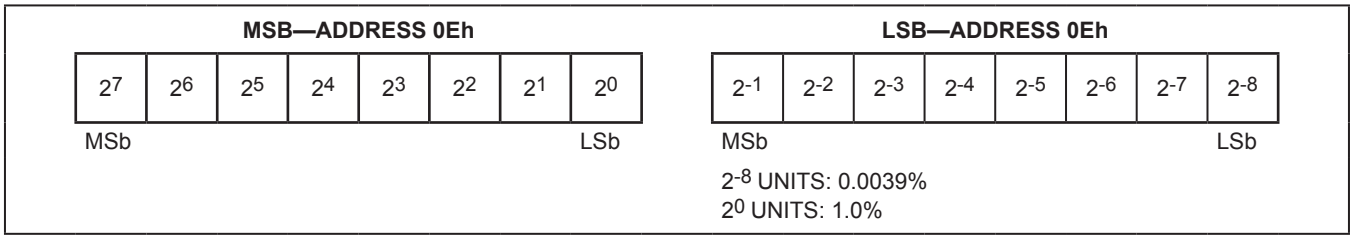


Figure 14. SOC_{AV} Register Format (Output)

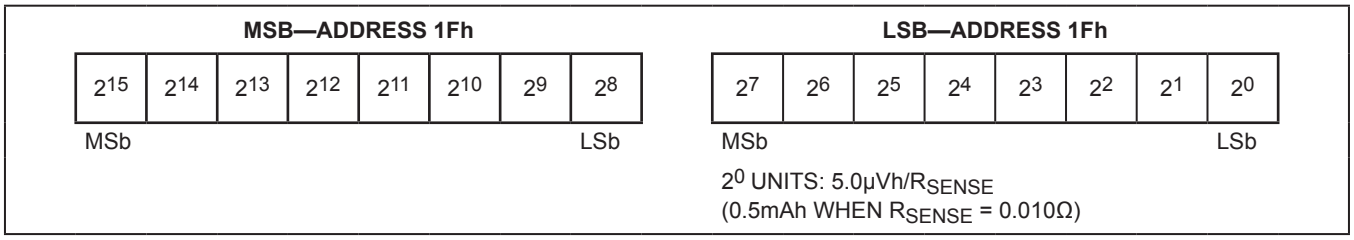


Figure 15. $RemCap_{AV}$ Register Format (Output)

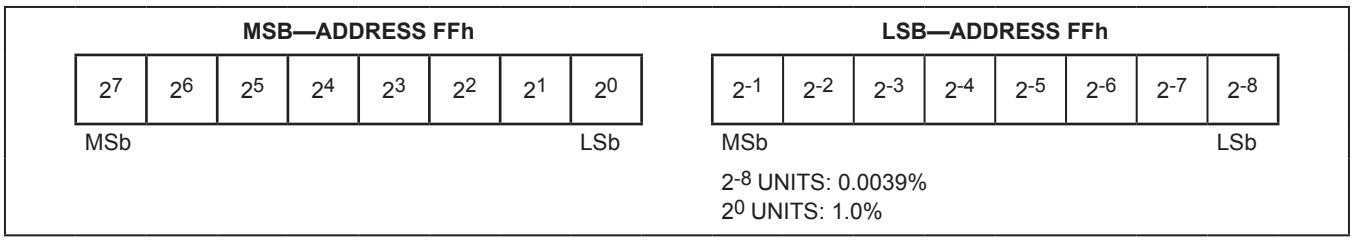


Figure 16. SOC_{VF} Register Format (Output)

Alternatively, the TTE register can be used to estimate time to empty for any given current load. Whenever the AtRate register is programmed to a negative number, representing a discharge current, the TTE register displays the estimated time to empty for the application based on the AtRate register value. Figure 17 shows the TTE register format.

Age Register (07h)

The Age register contains a calculated percentage value of the application's present cell capacity compared to its expected capacity. The result can be used by the host to gauge the cell's health as compared to a new cell of the same type. The result is displayed as a percentage value from 0 to 256% with a 0.0039% LSb. Figure 18 shows the Age register format. The equation for the register output is:

Age Register = 100% x (FullCAP Register/ DesignCap Register)

Cycles Register (17h)

The Cycles register accumulates total percent change in the cell during both charging and discharging. The result is stored as a total count of full charge/discharge cycles. For example, a full charge/discharge cycle results in the Cycles register incrementing by 100%. The Cycles register has a full range of 0 to 65535% with a 1% LSb. This register is reset to 0% at power-up. To maintain the lifetime cycle count of the cell, this register must be periodically saved by the host and rewritten to the device at power-up. See the *Save and Restore Registers* section for details. See Figure 19 for the Cycles register format.

VFOCV Register (FBh)

The VFOCV register contains the raw open-circuit voltage output of the voltage fuel gauge. This value is used in other internal calculations and can be read for debug purposes. The result is a 12-bit value ranging from 2.5V to 5.119V where 1 LSb is 1.25mV. The bottom 4 bits of this register are don't care bits. See Figure 20 for the VFOCV register format.

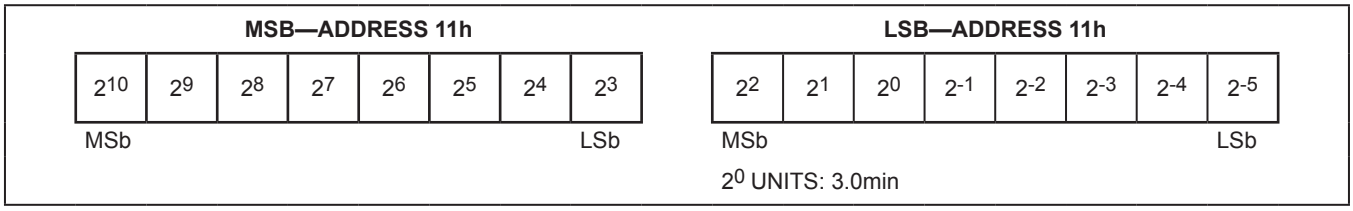


Figure 17. TTE Register Format (Output)

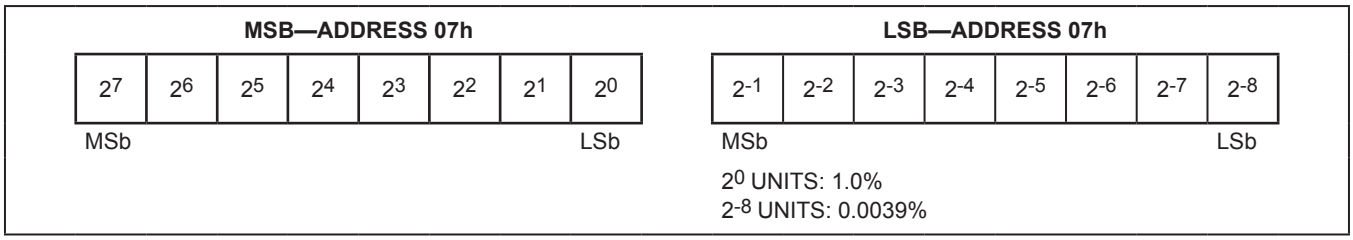


Figure 18. Age Register Format (Output)

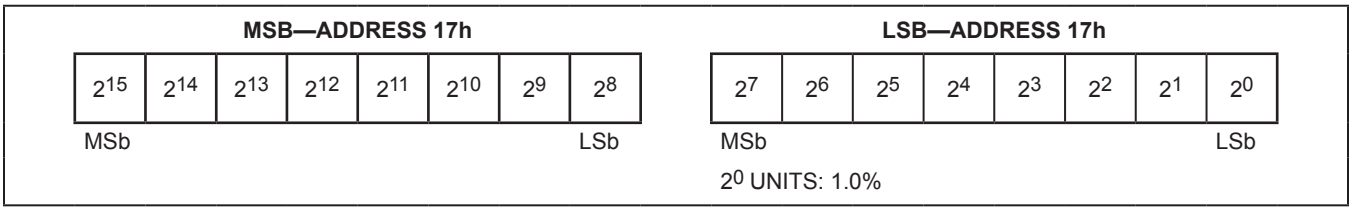


Figure 19. Cycles Register Format (Output)

FullCAP Register (10h)

This register holds the ModelGauge m3 algorithm calculated full capacity of the cell under best-case conditions (light load, hot). A new full-capacity value is calculated after the end of every charge cycle in the application. The value is stored in terms of µVh and must be divided by the application sense-resistor value to determine capacity in mAh. Figure 21 is the FullCAP register format. See the *End-of-Charge Detection* section.

FullCapNom Register (23h)

This register holds the calculated full capacity of the cell, not including temperature and charger tolerance. New full capacity values are calculated periodically by the IC during operation. The value is stored in terms of µVh and must be divided by the application sense resistor value to determine capacity in mAh. This register is used to calculate the outputs of the ModelGauge m3 algorithm and is available to the user only for debug. Figure 22 is the FullCapNom register format.

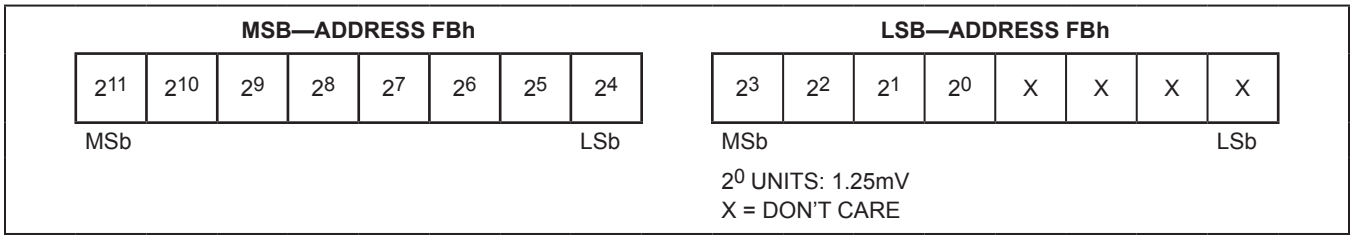


Figure 20. VFOCV Register Format (Output)

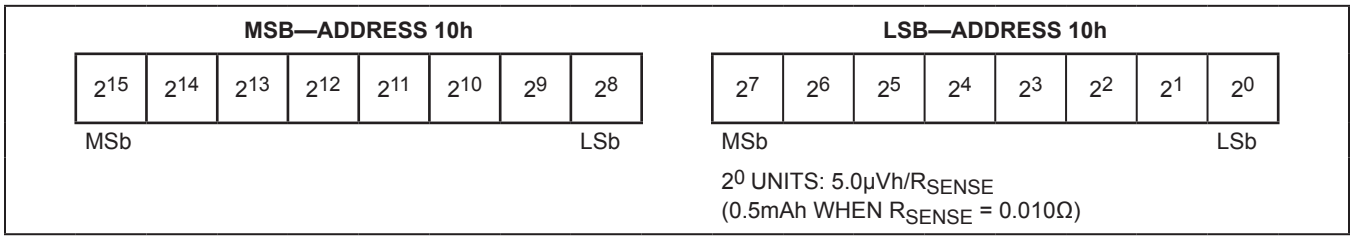


Figure 21. FullCAP Register Format (Output)

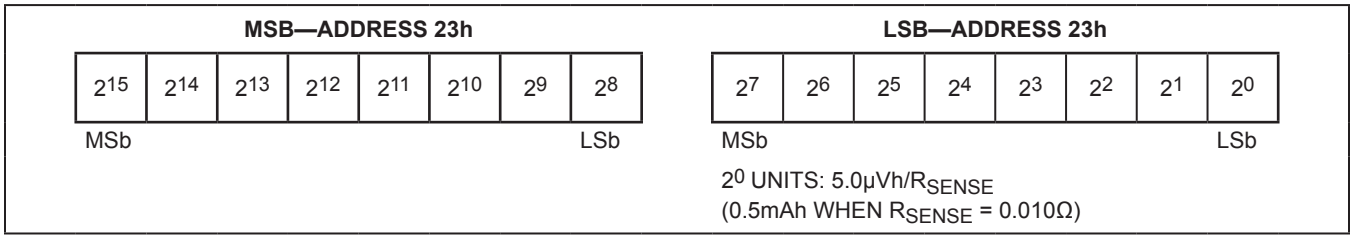


Figure 22. FullCapNom Register Format (Output)

QH Register (4Dh)

The QH register displays the raw coulomb count generated by the device. This register is used internally as an input to the mixing algorithm. Monitoring changes in QH over time can be useful for debugging device operation. The QH register is set to 0000h at power-up. The QH register format is shown in Figure 23.

Application-Specific Registers

The following registers define the behavior of the application. They must be programmed by the user before the ModelGauge m3 algorithm is accurate. Any changes to these register values require recharacterization of the cell.

DesignCap Register (18h)

The DesignCap register holds the expected capacity of the cell. This value is used to determine age and health of the cell by comparing against the calculated present capacity stored in the FullCAP register. DesignCap has an LSb equal to 5.0µVh and a full range of 0 to 327.68mVh. The user should multiply the mAh capacity of the cell by the sense resistor value to determine the µVh value to store in the DesignCap register. The DesignCap register format is shown in Figure 24.

FullSOCThr Register (13h)

The FullSOCThr register gates detection of end-of-charge. SOC_{VF} must be larger than the FullSOCThr value before ICHGTerm is compared to the AverageCurrent register value. The recommended FullSOCThr register setting for most applications is 95%. See the ICHGTerm register description for details. The FullSOCThr register is 70% at power-up. Figure 25 is the FullSOCThr register format.

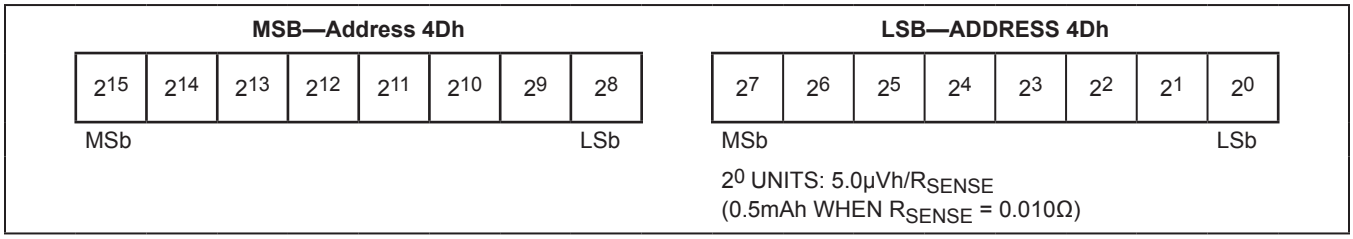


Figure 23. QH Register Format (Output)

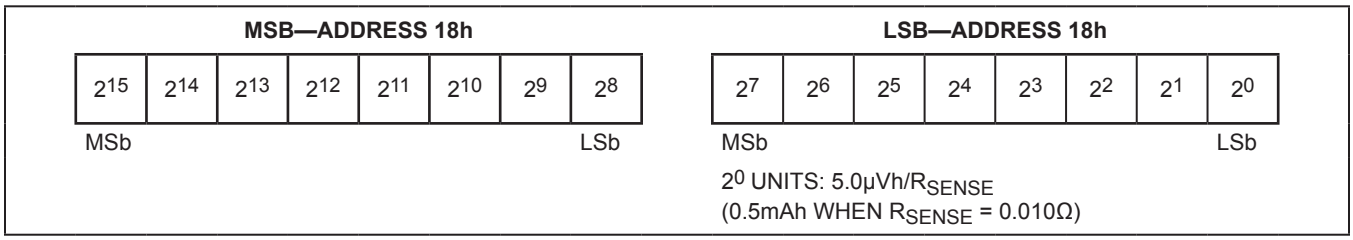


Figure 24. DesignCap Register Format (Input)

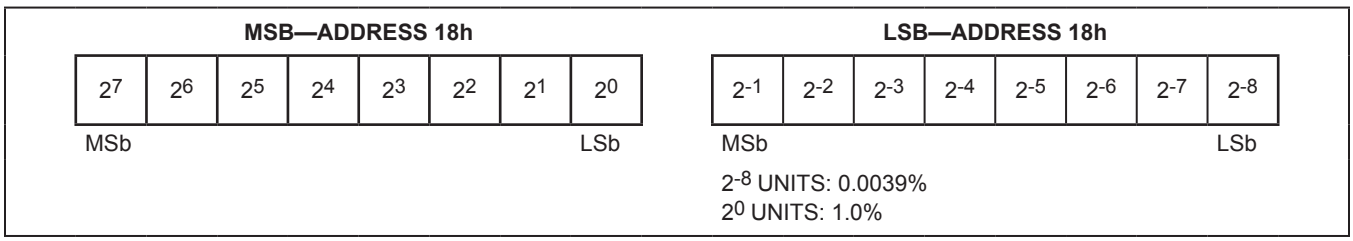


Figure 25. FullSOCThr Register Format (Input)

End-of-Charge Detection

The device detects the end of a charge cycle when the application current falls into the band set by the ICHGTerm register value. By monitoring both the Current and AverageCurrent registers, the device can reject false end-of-charge events such as application load spikes or early charge-source removal. See the End-of-Charge Detection graph in the *Typical Operating Characteristics* and Figure 26.

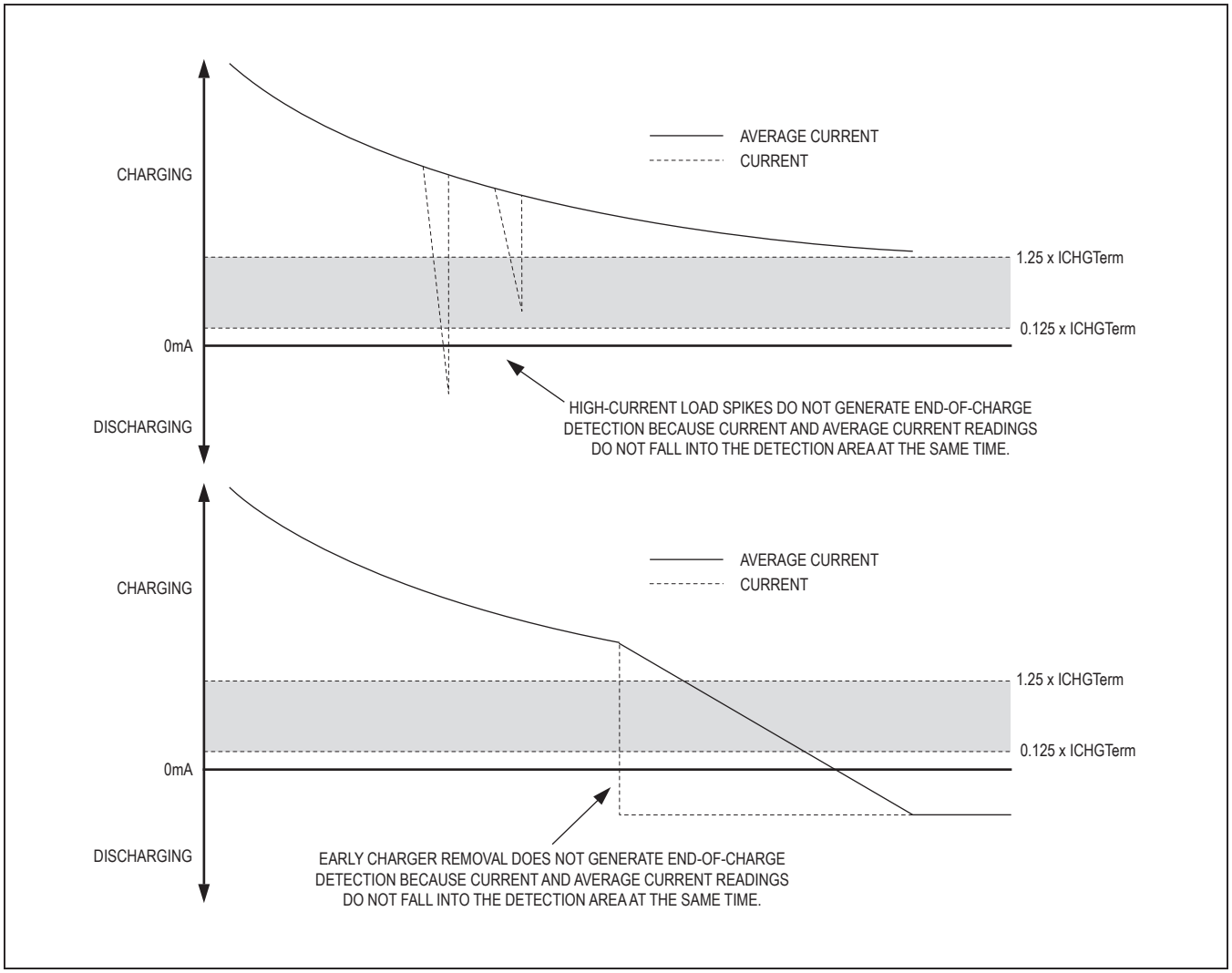


Figure 26. False End-of-Charge Events

When a proper end-of-charge event is detected, the device learns a new FullCAP register value based on the $RemCap_{REP}$ output. If the old FullCAP value was too high, it is adjusted downward after the last valid end-of-charge detection. If the old FullCAP was too low, it is adjusted upward to match $RemCap_{REP}$. This prevents the calculated state of charge from ever reporting a value greater than 100%. See Figure 27.

ICHGTerm Register (1Eh)

The ICHGTerm register allows the device to detect when a charge cycle of the cell has completed. The host should set the ICHGTerm register value equal to the exact charge termination current used in the application. The device detects end of charge if all the following conditions are met:

- SOC_{VF} > FullSOCThr
- AND ICHGTerm x 0.125 < Current < ICHGTerm x 1.25
- AND ICHGTerm x 0.125 < AverageCurrent < ICHGTerm x 1.25

Values are stored in µV. Multiply the termination current by the sense resistor to determine the desired register value. This register has the same range and resolution as the Current register. Figure 28 shows the ICHGTerm register format. ICHGTerm defaults to 150mA (03C0h) at power-up.

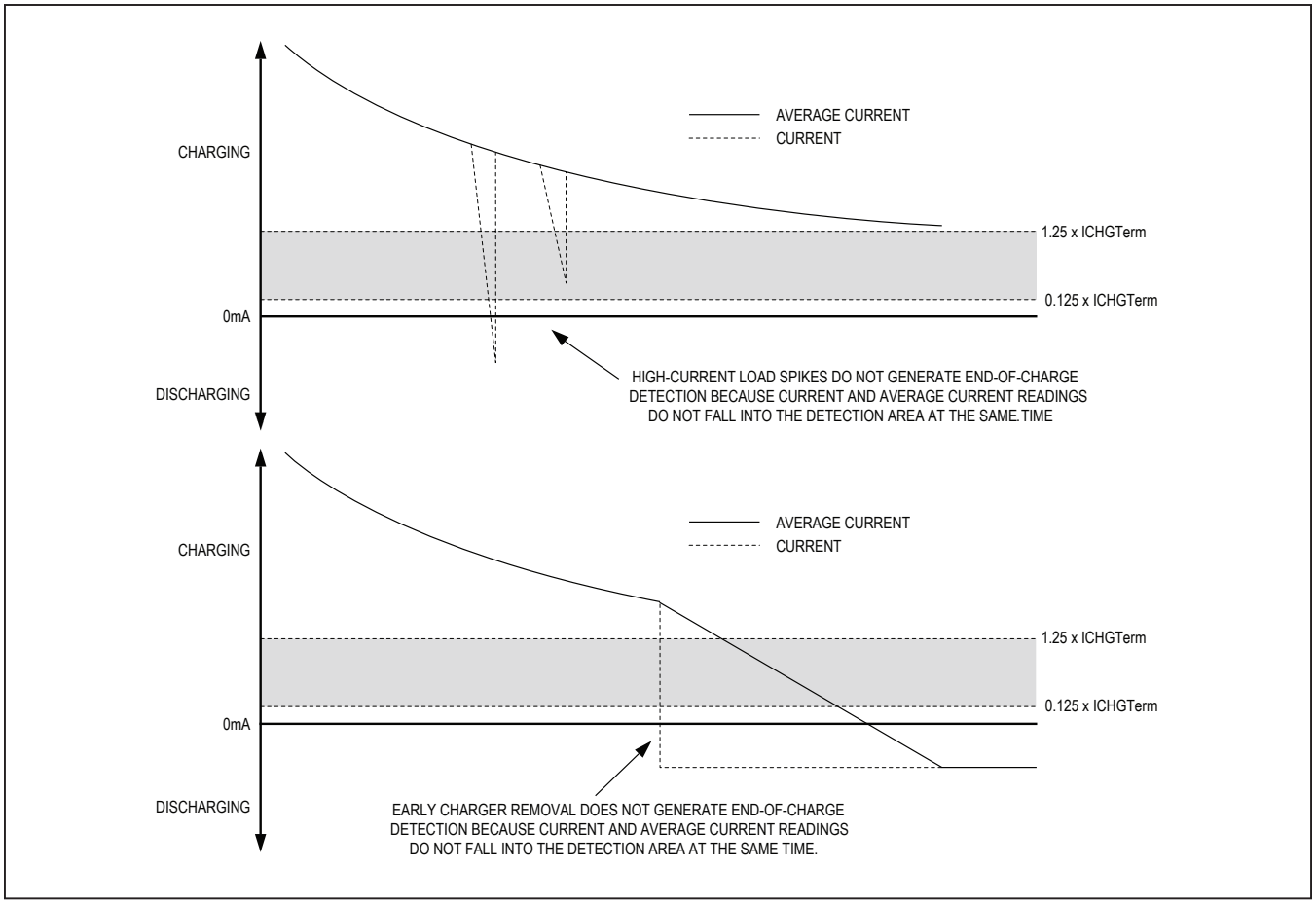


Figure 27. FullCAP Learning at End of Charge

V_empty Register (3Ah)

The V_empty register sets thresholds related to empty detection during operation. Figure 29 is the V_empty register format.

VE^8:VE^0—Empty Voltage. Sets the voltage level for detecting empty. A 10mV resolution gives a 0 to 5.11V range. This value is written to 3.12V at power-up.

VR^6:VR^0—Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled. A 40mV resolution gives a 0 to 5.08V range. This value is written to 3.68V at power-up.

Cell Characterization Information Registers

Proper cell characterization is required to achieve accuracy. The following registers (Table 1) hold information that must be generated through a cell-characterization procedure. Maxim provides a cell-characterization service. Contact the factory for details.

Table 1. Cell Characterization Information Registers

REGISTER	ADDRESS
Characterization Table (48 words)	80h to AFh
FullCap	10h
DesignCap	18h
ICHGTerm	1Eh
FullCapNom	23h
RCOMP0	38h
Iavg_empty	36h
TempCo	39h
QResidual 00	12h
QResidual 10	22h
QResidual 20	32h
QResidual 30	42h

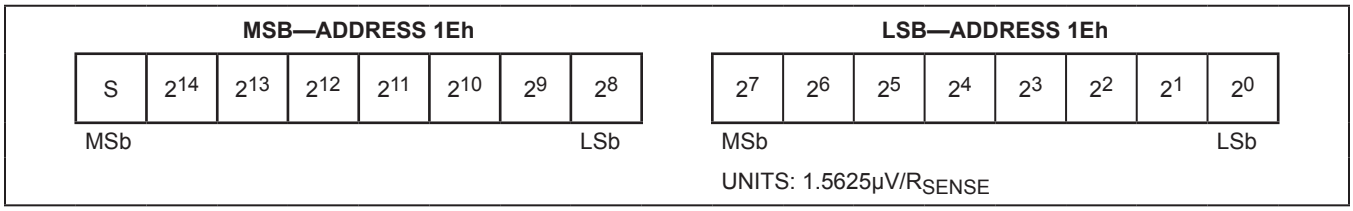


Figure 28. ICHGTerm Register Format (Input)

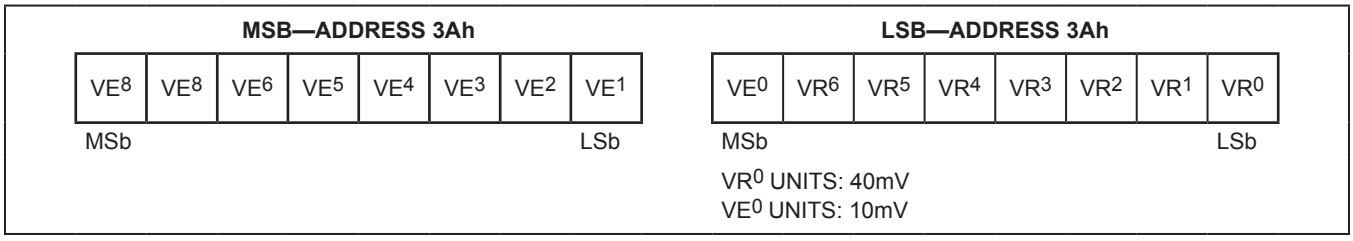


Figure 29. V_empty Register Format (Input)

Algorithm Configuration Registers

The following registers allow operation of the ModelGauge m3 algorithm to be adjusted for the application. It is recommended that the default values for these registers be used.

FilterCFG Register (29h)

The FilterCFG register sets the averaging time period for all A/D readings, for mixing OCV results and coulomb-count results. It is recommended that these values are not changed unless absolutely required by the application. Figure 30 shows the FilterCFG register format:

CURR3:CURR0—Sets the time constant for the AverageCurrent register. The default POR value of 4h gives a time constant of 11.25 seconds. The equation setting the period is:

$$\text{AverageCurrent time constant} = 175.8\text{ms} \times 2^{(2+\text{CURR})}$$

VOLT2:VOLT0—Sets the time constant for the AverageV_{CELL} register. The default POR value of 2h gives a time constant of 45.0s. The equation setting the period is:

$$\text{Average}V_{CELL}\text{ time constant} = 175.8\text{ms} \times 2^{(6+\text{VOLT})}$$

MIX3:MIX0—Sets the time constant for the mixing algorithm. The default POR value of Dh gives a time constant of 12.8 hours. The equation setting the period is:

$$\text{Mixing Period} = 175.8\text{ms} \times 2^{(5+\text{MIX})}$$

TEMP2:TEMP0—Sets the time constant for the AverageTemperature register. The default POR value of 1h gives a time constant of 12min. The equation setting the period is:

$$\text{AvergeTemperature time constant} = 175.8\text{ms} \times 2^{(8\ +\ \text{TEMP})}$$

X—Reserved. Do not modify.

RelaxCFG Register (2Ah)

The RelaxCFG register defines how the device detects if the cell is in a relaxed state. See Figure 32. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time, dV/dt, shows little or no change. If AverageCurrent remains below the Load threshold while V_{CELL} changes less than the dV threshold over two consecutive periods of dt, the cell is considered relaxed. Figure 31 shows the RelaxCFG register format:

Load6:Load0—Sets the threshold, which the AverageCurrent register is compared against. The AverageCurrent register must remain below this threshold value for the cell to be considered unloaded. Load is an unsigned 7-bit value where 1 LSb = 50µV. The default value is 800µV.

MSB—ADDRESS 29h

X	X	TEMP 2	TEMP 1	TEMP 0	MIX3	MIX2	MIX1
MSb							LSb

LSB—ADDRESS 29h

MIX0	VOLT2	VOLT1	VOLT0	CURR 3	CURR 2	CURR 1	CURR 0
MSb							LSb

Figure 30. FilterCFG Register Format (Input)

MSB—ADDRESS 2Ah

$Load^6$	$Load^5$	$Load^4$	$Load^3$	$Load^2$	$Load^1$	$Load^0$	dV4
MSb							LSb

LSB—ADDRESS 2Ah

dV3	dV2	dV1	dV0	dt3	dt2	dt1	dt0
MSb							LSb

$LOAD^0$ UNITS: $50\mu V/R_{SENSE}$
(5.0mAh WHEN R_{SENSE} = 0.010Ω)

Figure 31. RelaxCFG Register Format (Input)

dV4:dV0—Sets the threshold, which V_{CELL} is compared against. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed; dV has a range of 0 to 40mV where 1 LSb = 1.25mV. The default value is 1.75mV.

dt3:dt0—Sets the time period over which change in V_{CELL} is compared against dV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed. The default value is 6 minutes. The comparison period is calculated as:

$$\text{Relaxation Period} = 2^{dt} \times 0.1758s$$

LearnCFG Register (28h)

The LearnCFG register controls all functions relating to adaptation during operation. The LearnCFG register default values should not be changed unless specifically required by the application. Figure 33 is the LearnCFG register format:

0—Bit must be written 0. Do not write 1.

1—Bit must be written 1. Do not write 0.

Filt Empty—Empty Detect Filter. This bit selects whether empty is detected by a filtered or unfiltered voltage reading. Setting this bit to 1 causes the empty detection algorithm to use the AverageV_{CELL} register. Setting this bit to 0 forces the empty detection algorithm to use the V_{CELL} register. This bit is written to 0 at power-up.

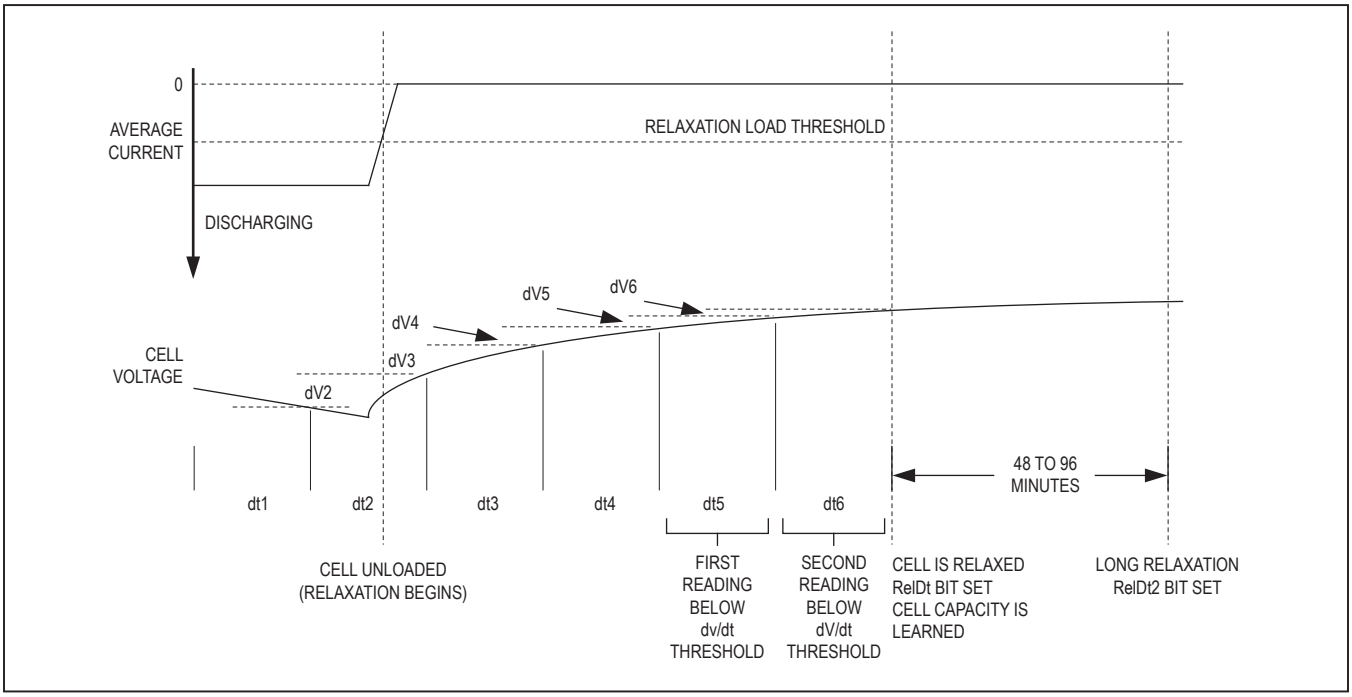


Figure 32. Cell Relaxation Detection

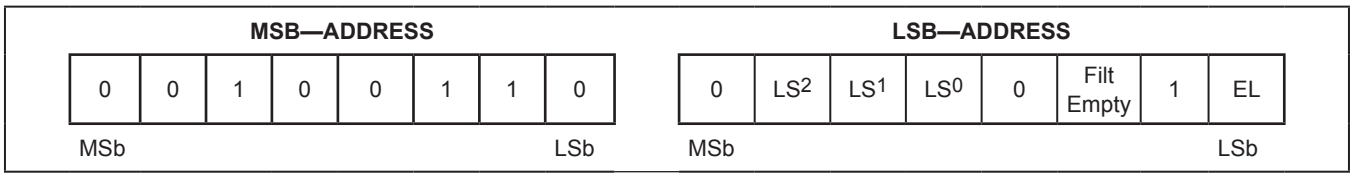


Figure 33. LearnCFG Register Format (Input/Output)

LS2:LS0—Learn Stage. See Figure 3 The Learn Stage value controls the influence of the VFG on the mixing algorithm. At power-up, Learn Stage defaults to 0h, making the voltage fuel gauge dominate. Learn Stage then advances to 7h over the course of two full cell cycles to make the coulomb counter dominate. Host software can write the Learn Stage value to 7h to advance to the final stage at any time. Writing any value between 1h and 6h is ignored. Learn Stage reflects the D5, D6, and D7 bits of the Cycles register. Update the Cycles register to advance to an intermediate state. For example, set Cycles = 160% to advance to Learn Stage 5.

EL—Empty Learning. Set this bit to 1 to turn on the Empty Learning feature. When enabled, the QResidual table is automatically adjusted at each empty event to compensate for the age of battery.

MiscCFG Register (2Bh)

The MiscCFG control register enables various other functions of the device. The MiscCFG register default values should not be changed unless specifically required by the application. Figure 34 is the MiscCFG register format:

0—Bit must be written 0. Do not write 1.

1—Bit must be written 1. Do not write 0.

X—Don't Care. Bit may read 0 or 1.

SACFG1:SACFG0—SOC Alert Config. SOC Alerts can be generated by monitoring any of the SOC registers as follows. SACFG defaults to 00 at power-up:

0 0 SOC Alerts are generated based on the SOC_{REP} register.

0 1 SOC Alerts are generated based on the SOC_{AV} register.

1 0 SOC Alerts are generated based on the SOC_{MIX} register.

1 1 SOC Alerts are generated based on the SOC_{VF} register.

MR4:MR0—Mixing Rate. This value sets the strength of the servo mixing rate after the final mixing state has been reached (> 2.08 complete cycles). The units are MR0 = 6.25µV, giving a range up to 19.375mA with a standard 0.010Ω sense resistor. Setting this value to 00000b disables servo mixing and the IC continues with time-constant mixing indefinitely. The default setting is 18.75µV or 1.875mA with a standard sense resistor.

enBi1—Enable reset on battery-insertion detection. Set this bit to 1 to force a reset of the fuel gauge whenever a battery insertion is detected based on AIN pin monitoring. This bit is written to 1 at power-up.

FSTAT Register (3Dh)

The FSTAT register is a read-only register that monitors the status of the ModelGauge algorithm. Do not write to this register location. Figure 35 is the FSTAT register format:

RelDt—Relaxed cell detection. This bit is set to a 1 whenever the ModelGauge m3 algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever a current greater than the Load threshold is detected. See Figure 32.

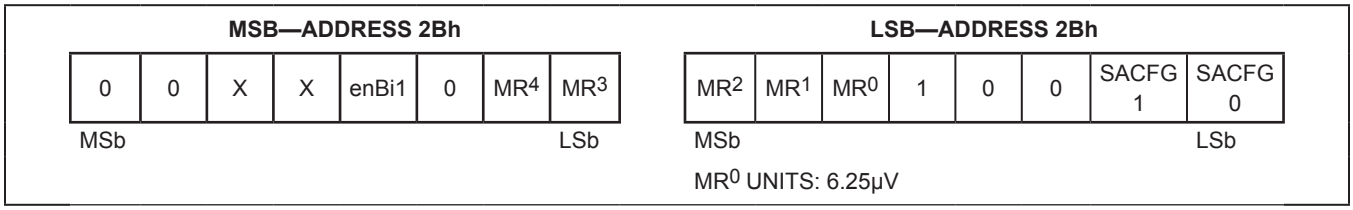


Figure 34. MiscCFG Register Format (Input)

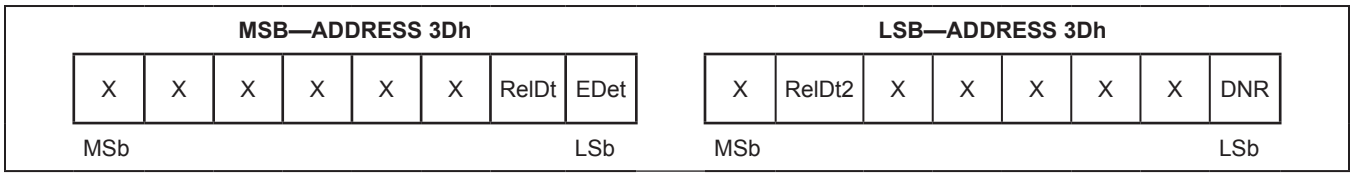


Figure 35. FSTAT Register Format (Output)

RelDt2—Long Relaxation. This bit is set to a 1 whenever the ModelGauge m3 algorithm detects that the cell has been relaxed for a period of 48 to 96 minutes or longer. This bit is cleared to 0 whenever the cell is no longer in a relaxed state. See Figure 32.

DNR—Data Not Ready. This bit is set to 1 at cell insertion and remains set until the output registers have been updated. Afterwards, the IC clears this bit indicating the fuel gauge calculations are now up to date. This takes between 445ms and 1.845s depending on whether the IC was in a powered state prior to the cell-insertion event.

EDet—Empty Detection. This bit is set to 1 when the IC detects that the cell empty point has been reached. This bit is reset to 0 when the cell voltage rises above the recovery threshold. See the V_empty register for details.

X—Don't Care. This bit is undefined and can be logic 0 or 1.

AtRate Register (04h)

The AtRate register allows host software to estimate remaining capacity, SOC, and time to empty for a theoretical load current. Whenever the AtRate register is programmed to 0 or a positive value, the device uses A/D measurements for determining the SOC_{AV}, $RemCap_{AV}$, and TTE register values. Whenever the AtRate register is programmed to a negative value indicating a hypothetical discharge current, the SOC_{AV}, $RemCap_{AV}$, and TTE registers calculate their values for the AtRate register theoretical current instead. The AtRate register holds a two's-complement 16-bit value. Do not write 8000h to this register. Figure 36 shows the AtRate register format.

Power-Up and Power-On Reset

Any power-on reset (POR) of the device resets all memory locations to their default POR value. This removes any custom cell characterization and application data, affects ALRT interrupt and shutdown mode settings, and resets all learned adjustments made by the fuel gauge. To maintain accuracy of the fuel gauge and reset operation settings of the device, the host must reload all application memory data and restore all learned fuel-gauge information. Note that the device may take up to 445ms to completely reset operation after a POR event occurs. See Figure 37. Saved data should not be restored until after this period is over. The following procedure is recommended:

1) Read Status register. If POR = 0, exit.
2) Wait 600ms for POR operation to fully complete.
3) Restore all application register values.
4) Restore fuel gauge learned-value information (see the *Save and Restore Registers* section).
5) Clear POR bit.

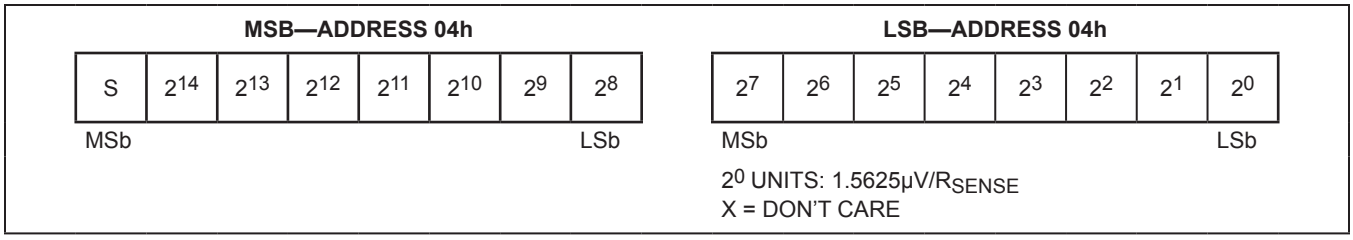


Figure 36. AtRate Register Format (Input)

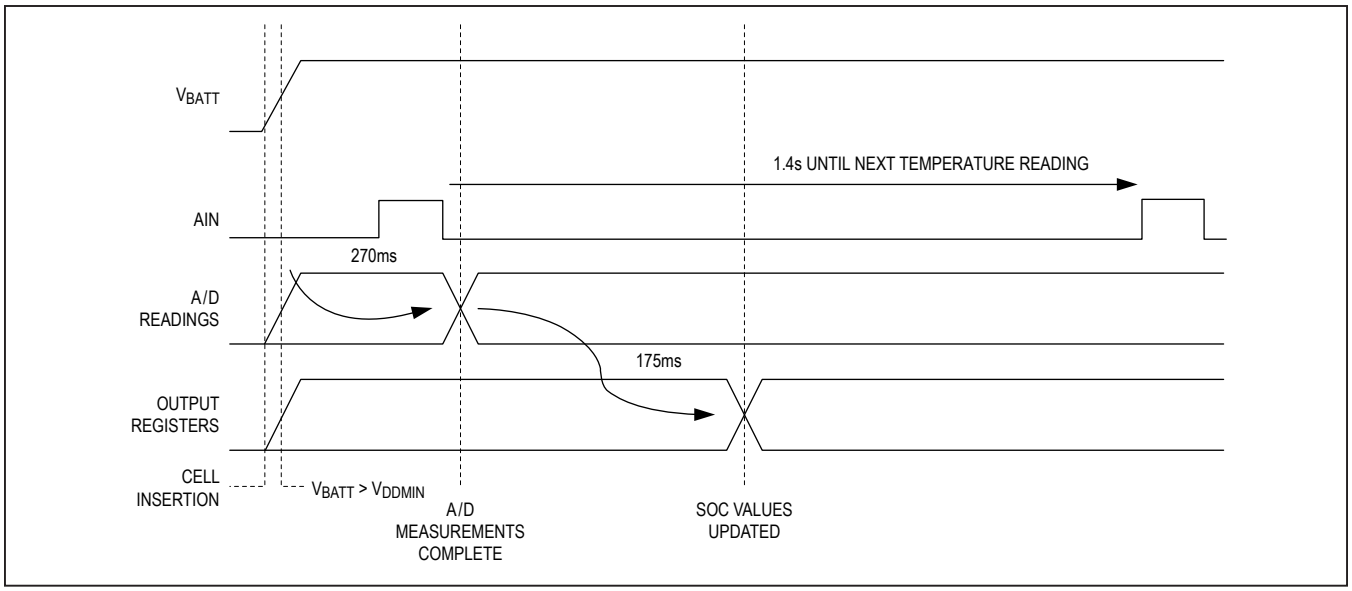


Figure 37. Power-Up Operation

Save and Restore Registers

The device is designed to operate outside the battery pack and can therefore be exposed to power loss when in the application. To prevent the loss of learned information during power cycles, a save-and-restore procedure can be used to maintain register values in nonvolatile memory external to the device. The registers (Table 2) must be stored externally and then rewritten to the device after power-up to maintain a learned state of operation.

Note that some registers are application outputs, some registers are for internal calculations, and some are characterization setup registers. Registers that are not internal are described in their own sections. These values should be stored by the application at periodic intervals. Some recommended back-up events are:

- End-of-charge
- End-of-discharge
- Prior to application entering shutdown state

The host is responsible for loading the default characterization data at first power-up of the device, and restoring the default characterization data plus learned information on subsequent power-up events.

Table 2. Save and Restore Registers

REGISTER	ADDRESS
FullCap	10h
Cycles	17h
RCOMP0	38h
TempCo	39h
QResidual 00	12h
QResidual 10	22h
QResidual 20	32h
QResidual 30	42h
dQacc	45h
dPacc	46h

Battery Removal and Insertion

The device detects when a cell has been removed or inserted into the application. This allows the device to adjust to the new cell to maintain accuracy. The removal-detection feature also allows the device to quickly warn the host processor through interrupt of impending power loss if enabled.

Detection occurs by monitoring the AIN pin voltage compared to the THRM pin. Whenever a cell is present, the external resistor-divider network sets the voltage of AIN. When the cell is removed, the remaining external resistor pulls AIN to the THRM pin voltage level. Whenever $V_{AIN} < V_{THRM} - V_{DETF}$, the device determines that a cell is present in the application. If $V_{AIN} > V_{THRM} - V_{DETR}$, the device determines that no cell is present at that time.

Cell Insertion (IC Already Powered)

The device is ready to detect a cell insertion if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. See Figure 38. When a cell insertion is detected, the fuel gauge is reset and all fuel-gauge outputs are updated to reflect the SOC of the newly inserted cell. This process can take up to 1.845s (FTHRM = 0) or 620ms (FTHRM = 1) from time of insertion. Note that the device uses the cell voltage as a starting point for the fuel gauge. If the cell voltage is not fully relaxed at time of insertion, the fuel gauge begins with some initial error. See the *Fuel-Gauge Learning and Age Support* section for details. The host can disable this feature by clearing the enBi1 bit in the MiscCFG register.

The device can also be configured to alert the host when cell insertion occurs. When Bei = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after insertion. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the IC must be reconfigured at each insertion.

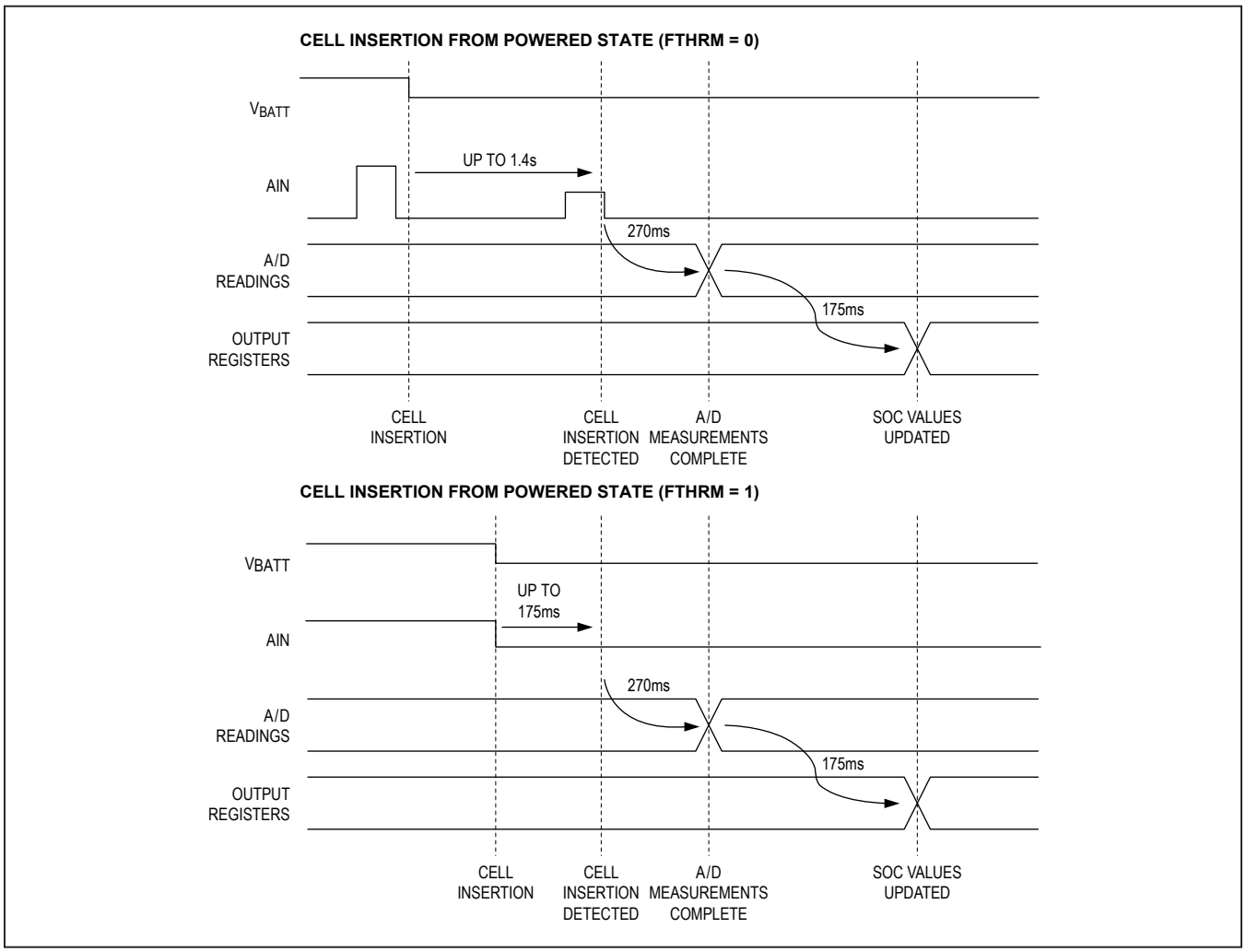


Figure 38. Operation After Cell Insertion

Cell Removal

The device detects a cell removal if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. Cell removal does not affect IC operation. The device continues to update fuel-gauge outputs. The host should monitor the Br and Bst bits of the Status register to determine if the fuel-gauge outputs are valid.

The device can also be configured to alert the host when cell removal occurs. When Ber = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after removal. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the IC must be reconfigured at each insertion.

Fast Detection of Cell Removal

The device can be configured to quickly alert the host of impending power loss on cell removal. This fast response allows the system to quickly and gracefully hibernate to prevent power loss during battery swap. When Ber = 1, FTHRM = 1, and ALRTp = 0 in the CONFIG register, an interrupt on the ALRT pin is generated within 100µs after V_{AIN} becomes greater than V_{THRM} - V_{DETR}. If fast detection is used, it is recommended that all other IC interrupts are disabled to prevent the host from spending time determining the cause of the interrupt. Fast detection of cell removal has no affect on fuel-gauge operation, but leaving the external resistor-divider active increases current consumption of the application. See Figure 39.

Modes of Operation

The device operates in one of two power modes: active and shutdown. While in active mode, the device operates as a high-precision battery monitor with temperature, voltage, auxiliary inputs, current, and accumulated current measurements acquired continuously, and the resulting values updated in the measurement registers. READ and WRITE access is allowed only in active mode.

In shutdown mode, the LDO is disabled and all activity stops, although **volatile RAM contents remain preserved.** All A/D register and fuel-gauge output values are maintained. There are several options for entering shutdown:

Entering shutdown:

- **SHUTDOWN command**—Write the CONFIG register SHDN = 1 through the I²C interface; wait for longer than the SHDNTIMER register value.
- **Pack removal**—Pack removal detection is valid for longer than the SHDNTIMER register value and the CONFIG register AINSH = 1.
- **I²C shutdown**—I²C lines both persist low for longer than the SHDNTIMER register value and the CONFIG register I2CSH = 1.
- **ALRT shutdown**—Shutdown occurs when the ALRT line is externally driven low for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 0), or the ALRT line is externally driven high for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 1). See the *CONFIG Register (1Dh)* section.

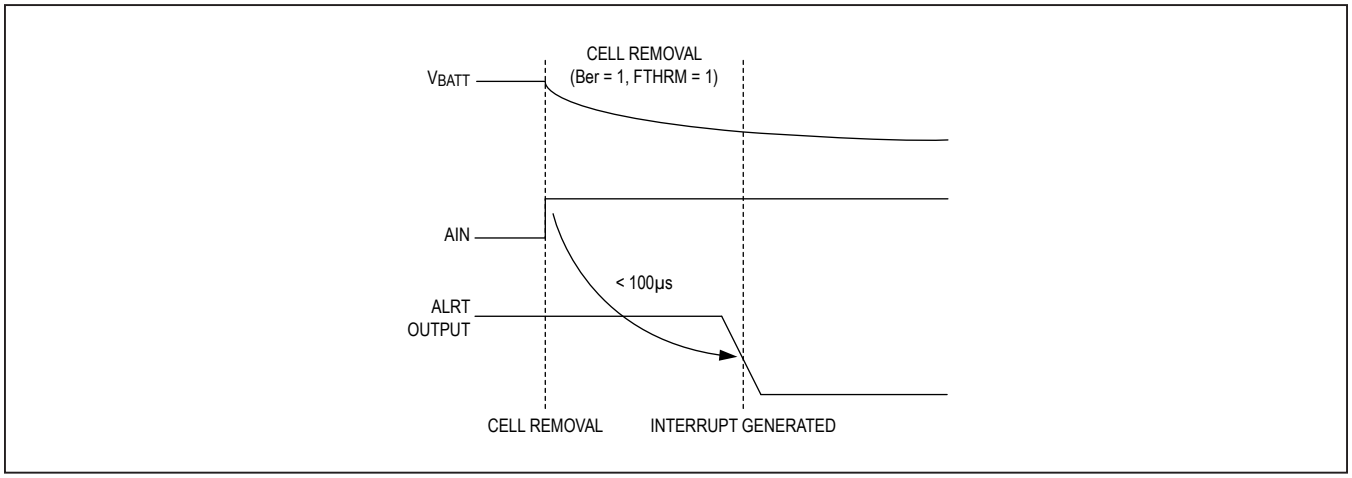


Figure 39. Fast Detection of Cell Removal

These shutdown entry modes are all programmable according to application. Shutdown events are gated by the SHDNTIMER register, which allows a long delay between the shutdown event and the actual shutdown. By behaving this way, the device takes the best reading of the relaxation voltage.

Exiting shutdown:

- **I²C Wakeup**—Any edge on SCL/SDA.
- **ALRT Wakeup**—Any edge on ALRT line and (ALSH = 1 or I2CSH = ALSH = 0).
- **Reset**—IC is power cycled.

See the *Status and Configuration* section for detailed descriptions of the SHDNTIMER and CONFIG registers.

The state of the device when returning to active mode differs depending on the triggering event. See Figure 40. Host software can monitor the POR and Bi status bits to determine what type of event has occurred.

ALRT Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, a high or low temperature, or a high or low SOC. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Note that if the pin is configured to be logic-low when inactive, the external pullup increases current drain.

The ALRTp bit in the CONFIG register sets the polarity of the ALRT pin output. Alerts can be triggered by any of the following conditions:

- **Battery removal**—(V_{AIN} > V_{THRM} - V_{DETR}) and battery removal detection enabled (Ber = 1).
- **Battery insertion**—(V_{AIN} < V_{THRM} - V_{DETF}) and battery insertion detection enabled (Bei = 1).
- **Over-/undervoltage**—V_{ALRT} threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over-/undertemperature**—T_{ALRT} threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over/under SOC**—S_{ALRT} threshold violation (upper or lower) and alerts enabled (Aen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the Status register. Alerts generated by a threshold-level violation can be configured to be cleared only by software, or cleared automatically when the threshold level is no longer violated. See the CONFIG (1Dh) register description for details of the alert function configuration.

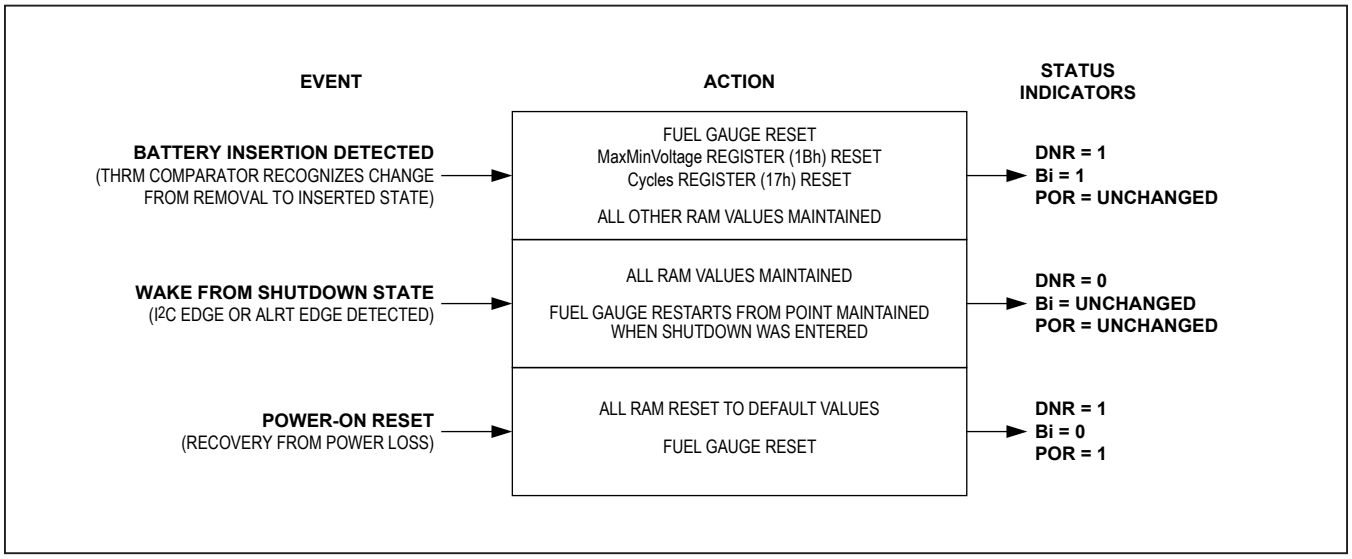


Figure 40. Device State Based on Shutdown Exit Condition

V_{ALRT} Threshold Register (01h)

The V_{ALRT} Threshold register (Figure 41) sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the V_{CELL} register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 20mV resolution over the full operating range of the V_{CELL} register. At power-up, the thresholds default to their maximum settings—FF00h (disabled).

T_{ALRT} Threshold Register (02h)

The T_{ALRT} Threshold register sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the Temperature register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are stored in two's-complement format and are selectable with 1°C resolution over the full operating range of the Temperature register. At power-up, the thresholds default to their maximum settings—7F80h (disabled). Figure 42 shows the T_{ALRT} Threshold register format.

S_{ALRT} Threshold Register (03h)

The S_{ALRT} Threshold register (Figure 43) sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the selected SOC_{REP}, SOC_{AV}, SOC_{MIX}, or SOC_{VF} register values. See the SACFG bits in the MiscCFG register description for details. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 1% resolution over the full operating range of the selected SOC register. At power-up, the thresholds default to their maximum settings—FF00h (disabled).

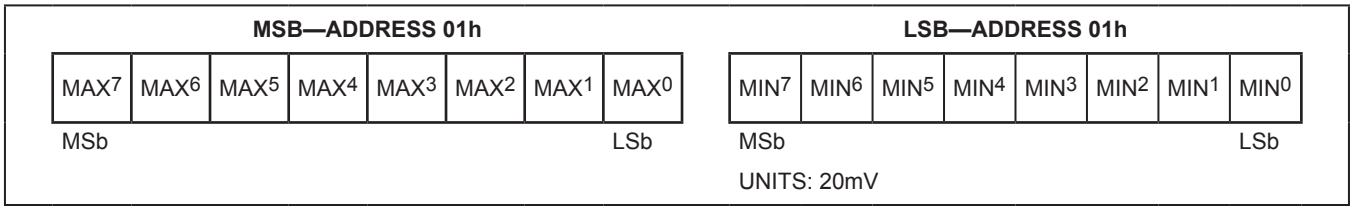


Figure 41. V_{ALRT} Threshold Register Format (Input)

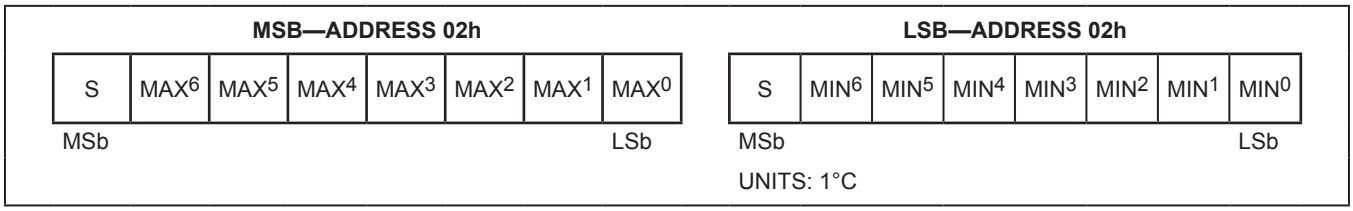


Figure 42. T_{ALRT} Threshold Register Format (Input)

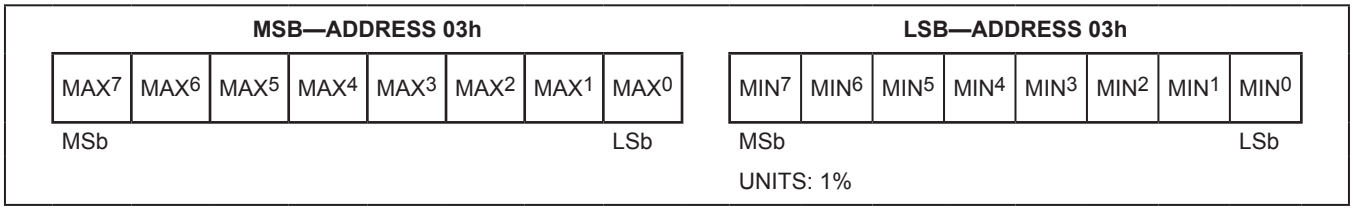


Figure 43. S_{ALRT} Threshold Register Format (Input)

Status and Configuration

The following registers control operation of the ALRT interrupt feature, control transition between active and shutdown modes of operation, and provide status updates to the host processor.

CONFIG Register (1Dh)

The CONFIG register holds all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within a 175.8ms task period. Figure 44 shows the CONFIG register format.

0—Bit must be written 0. Do not write 1.

Ber—Enable alert on battery removal. When Ber = 1, a battery-removal condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

Bei—Enable alert on battery insertion. When Bei = 1, a battery-insertion condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

Aen—Enable alert on fuel-gauge outputs. When Aen = 1, violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit affects the ALRT pin operation only. The Smx, Smn, Tmx, Tmn, Vmx, and Vmn bits are not disabled. This bit is set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

FTHRM—Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal (see the *Fast Detection of Cell Removal* section). Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit. This bit is set to 0 at power-up.

ETHRM—Enable Thermistor. Set to logic 1 to enable the automatic THRM output bias and AIN measurement every 1.4s. This bit is set to 1 at power-up.

ALSH—ALRT Shutdown. Set to logic 1 and clear the Aen, Ber, and Bei bits to configure the ALRT pin as an input to control shutdown mode of the device. The device enters shutdown if the ALRT pin is held active for longer than timeout of the SHDNTIMER register. The device enters active mode immediately on the opposite edge of the ALRT pin. When set to logic 0, the ALRT pin can function as an interrupt output. This bit is set to 0 at power-up. Note that if this bit is set to 1, the Bei, Ber, and Aen bits should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

I2CSH—I^{2}C Shutdown. Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low for more than timeout of the SHDNTIMER register. This also configures the device to wake up on a rising edge of either SDA or SCL. Set to 1 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up an edge of any of the SDA, SCL, or ALRT pins.

SHDN—Shutdown. Write this bit to logic 1 to force a shutdown of the device after timeout of the SHDNTIMER register. SHDN is reset to 0 at power-up and upon exiting shutdown mode.

Tex—Temperature External. When set to 1, the fuel gauge requires external temperature measurements to be written from the host. When set to 0, measurements on the AIN pin are converted to a temperature value and stored in the Temperature register instead. Tex is set to 1 at power-up.

Ten—Enable Temperature Channel. Set to 1 and set ETHRM or FTHRM to 1 to enable measurements on the AIN pin. Ten is set to 1 at power-up.

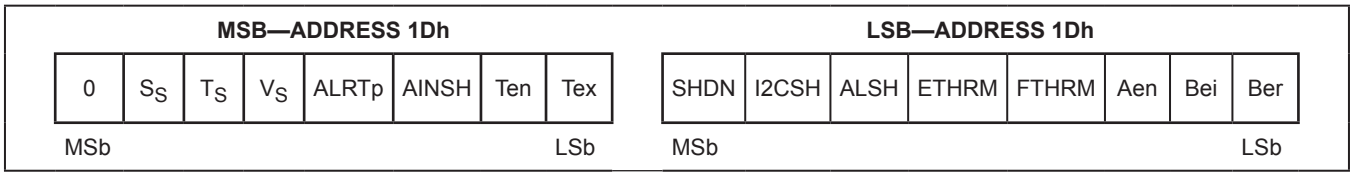


Figure 44. CONFIG Register Format (Input)

AINSH—AIN Pin Shutdown. Set to 1 to enable device shutdown when the battery is removed. The IC enters shutdown if the AIN pin remains high (AIN reading > V_{THRM} - V_{DETR}) for longer than the timeout of the SHDNTIMER register. This also configures the device to wake up when AIN is pulled low on cell insertion. AINSH is set to 0 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up an edge of any of the SDA, SCL, or ALRT pins.

ALRTp—ALRT Pin Polarity. Regardless if ALRT is being used as an input or output, if ALRTp = 0, the ALRT pin is active low; if ALRTp = 1, the ALRT pin is active high. ALRTp must be set to 0 to enable fast detection of cell removal. ALRTp is set to 0 at power-up.

V_S—Voltage ALRT Sticky. When V_S = 1, voltage alerts can only be cleared through software. When V_S = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded. V_S is set to 0 at power-up.

T_S—Temperature ALRT Sticky. When T_S = 1, temperature alerts can only be cleared through software. When T_S = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded. T_S is set to 1 at power-up.

S_S—SOC ALRT Sticky. When S_S = 1, SOC alerts can only be cleared through software. When S_S = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded. S_S is set to 0 at power-up.

TIMER Register (3Eh)

This register holds timing information for the fuel gauge. It is available to the user for debug purposes. Figure 45 shows the TIMER register format.

SHDNTIMER Register (3Fh)

The SHDNTIMER register sets the timeout period from when a shutdown event is detected until the device disables the LDO and enters low-power mode. Figure 46 shows the SHDNTIMER register format.

CTR12:CTR0—Shutdown Counter. This register counts the total amount of elapsed time since the shutdown trigger event. This counter value stops and resets to 0 when the shutdown timeout completes. The counter LSb is 1.4s.

THR2:THR0—Sets the shutdown timeout period from a minimum of 45s to a maximum of 1.6h. The default POR value of 7h gives a shutdown delay of 1.6h. The equation setting the period is:

$$\text{Shutdown Timeout Period} = 175.8\text{ms} \times 2^{(8+THR)}$$

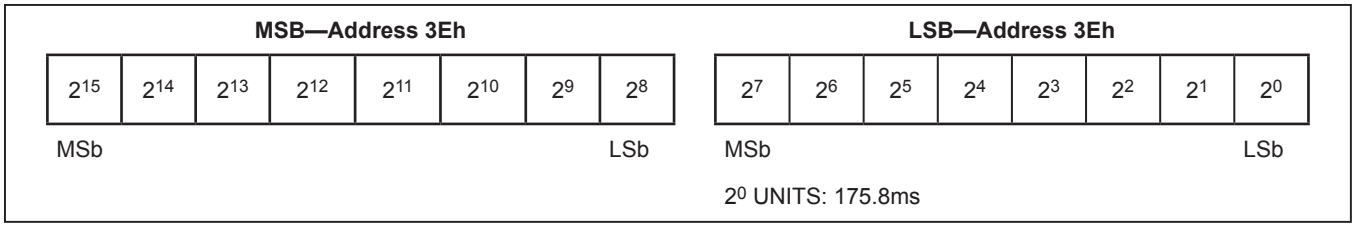


Figure 45. Timer Register Format (Output)

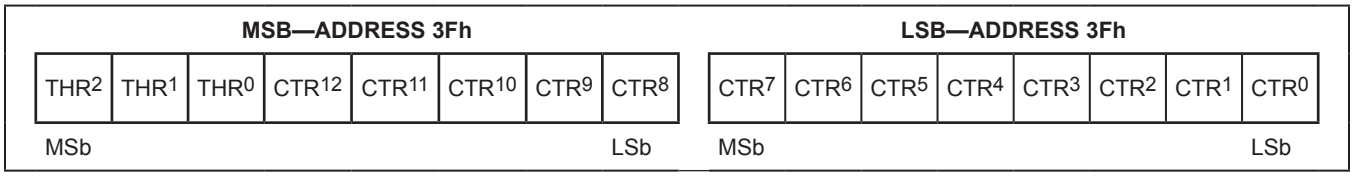


Figure 46. SHDNTIMER Register Format (Input/Output)

Status Register (00h)

The Status register maintains all flags related to alert thresholds and battery insertion or removal. Figure 47 shows the Status register format.

POR—Power-On Reset. This bit is set to a 1 when the device detects that a software or hardware POR event has occurred. If the host detects that the POR bit has been set, the device should be reconfigured. See the *Power-Up and Power-On Reset* section. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.

Bst—Battery Status. This bit is set to 0 when a battery is present in the system and set to 1 when the battery is removed. Bst is set to 0 at power-up.

Vmn—Minimum V_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever a V_{CELL} register reading is below the minimum V_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See V_S in the CONFIG register. Vmn is set to 0 at power-up.

Tmn—Minimum T_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is below the minimum T_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See T_S in the CONFIG register. Tmn is set to 0 at power-up.

Smn—Minimum SOC_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever SOC falls below the minimum SOC_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See S_S in the CONFIG register and SACFG in the MiscCFG register. Smn is set to 0 at power-up.

Bi—Battery Insertion. This bit is set to a 1 when the device detects that a battery has been inserted into the system by monitoring the AIN pin. This bit must be cleared by system software to detect the next insertion event. Bi is set to 0 at power-up.

Vmx—Maximum V_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever a V_{CELL} register reading is above the maximum V_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See V_S in the CONFIG register. Vmx is set to 0 at power-up.

Tmx—Maximum T_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever a Temperature register reading is above the maximum T_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See T_S in the CONFIG register. Tmx is set to 0 at power-up.

Smx—Maximum SOC_{ALRT} Threshold Exceeded. This bit is set to a 1 whenever SOC rises above the maximum SOC_{ALRT} value. This bit may or may not need to be cleared by system software to detect the next event. See S_S in the CONFIG register and SACFG in the MiscCFG register. Smx is set to 0 at power-up.

Br—Battery Removal. This bit is set to a 1 when the device detects that a battery has been removed from the system. This bit must be cleared by system software to detect the next removal event. Br is set to 0 at power-up.

X—Don't Care. This bit is undefined and can be logic 0 or 1.

MSB—ADDRESS 00h

Br	Smx	Tmx	Vmx	Bi	Smn	Tmn	Vmn
MSb							LSb

LSB—ADDRESS 00h

X	X	X	X	Bst	X	POR	X
MSb							LSb

Figure 47. Status Register Format (Input/Output)

Version Register (21h)

The Version register holds a 16-bit value that indicates the version of the device. Figure 48 shows the Version register format.

Voltage Measurement

While in active mode, the device periodically measures the voltage between the V_{BATT} and CSP pins over a 2.5V to 4.98V range. The resulting data is placed in the V_{CELL} register every 175.8ms with an LSb value of 0.625mV. Additionally, the device maintains a record of the minimum and maximum voltage measured by the device, and an average voltage over a time period defined by the host. Contents of the V_{CELL} and AverageV_{CELL} registers are indeterminate for the first conversion cycle time period after device power-up. The last values of the V_{CELL} and AverageV_{CELL} registers are maintained when the device enters shutdown mode.

V_{CELL} Register (09h)

While in active mode, the device periodically measures the voltage between the V_{BATT} and CSP pins over a 0 to 4.98V range. The resulting data is placed in the V_{CELL} register every 175.8ms with an LSb value of 0.625mV. Voltages above the maximum register value are reported as the maximum value. The lower 3 bits of the V_{CELL} register are don't care bits. Figure 49 shows the V_{CELL} register format.

AverageV_{CELL} Register (19h)

The AverageV_{CELL} register reports an average of V_{CELL} register readings over a configurable 12s to 24min time period. See the FilterCFG register description for details on setting the time filter. The resulting average is placed in the AverageV_{CELL} register with an LSb value of 0.625mV. The lower 3 bits of the AverageV_{CELL} register are don't care bits. The first V_{CELL} register reading after device power-up sets the starting point of the AverageV_{CELL} filter. Note that when a cell relaxation event is detected, the averaging period for the AverageV_{CELL} register changes to the period defined by dt3:dt0 in the RelaxCFG register. The AverageV_{CELL} register reverts back to its normal averaging period when a charge or discharge current is detected. Figure 50 shows the AverageV_{CELL} register format.

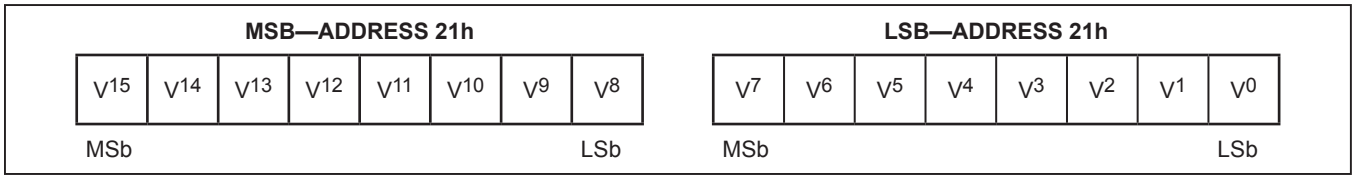


Figure 48. Version Register Format (Output)

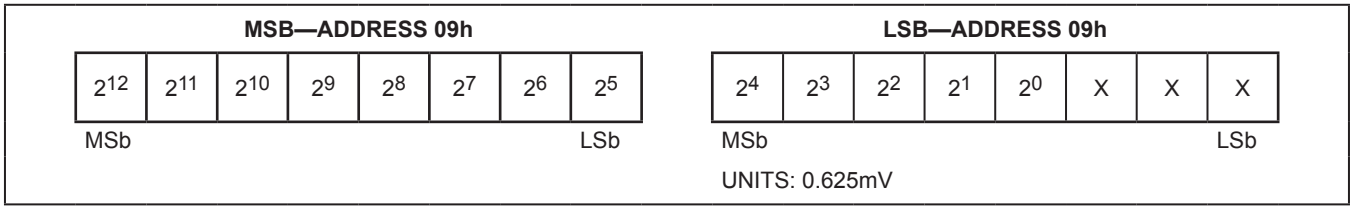


Figure 49. V_{CELL} Register Format (Output)

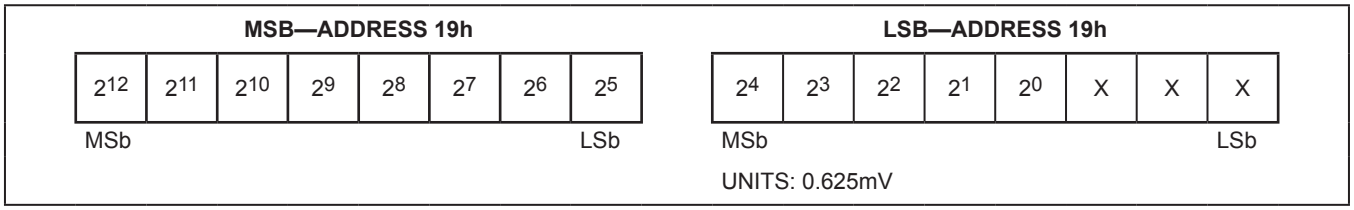


Figure 50. AverageV_{CELL} Register Format (Output)

MaxMinV_{CELL} Register (1Bh)

The MaxMinV_{CELL} register maintains the maximum and minimum V_{CELL} register values since the last fuel-gauge reset or until reset by the host software. Each time the V_{CELL} register updates, it is compared against these values. If V_{CELL} is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the MaxV_{CELL} value is set to 00h (the minimum) and the MinV_{CELL} value is set to FFh (the maximum). Therefore, both values are changed to the V_{CELL} register reading after the first update. Host software can reset this register by writing it to its power-up value of 00FFh. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution. Figure 51 shows the MaxMinV_{CELL} register format.

Current Measurement

While in active mode, the device periodically measures the voltage between the CSN and CSP pins over a ±51.2mV range. The resulting data is stored as a signed two's-complement value in the Current register every 175.8ms with an LSb value of 1.5625µV/R_{SENSE}. All devices are calibrated for current-measurement accuracy at the factory. However, if the application requires, Current Register readings can be adjusted by changing the COFF and CGAIN register settings.

Additionally, the device maintains a record of the minimum and maximum current measured by the device, and an average current over a time period defined by the host. Contents of the Current and AverageCurrent registers are 0000h until the first conversion cycle time period after IC power-up. The last values of the Current and AverageCurrent registers are maintained when the IC enters shutdown mode.

Current Register (0Ah)

While in active mode, the device periodically measures the voltage between the CSN and CSP pins over a ±51.2mV range. The resulting data is stored as a two's-complement value in the Current register every 175.8ms with an LSb value of 1.5625µV/R_{SENSE}. Voltages outside the minimum and maximum register values are reported as the minimum or maximum value. Figure 52 shows the Current register format and Table 3 shows the Sample Current register conversions.

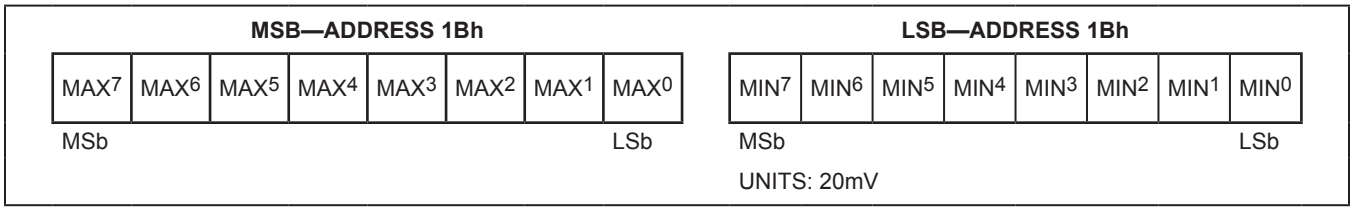


Figure 51. MaxMinV_{CELL} Register Format (Output)

Table 3. Sample Current Register Conversions

FUNCTION	SENSE RESISTOR (Ω)	CGAIN REGISTER	CURRENT REGISTER RESOLUTION (µA)	CURRENT REGISTER RANGE (A)	MAXIMUM CELL CAPACITY (Ah)
Adjusting sense resistor to meet range and accuracy requirements	0.005	4000h	312.50	±10.24	32.768
	0.010	4000h	156.25	±5.12	16.384
	0.020	4000h	78.125	±2.56	8.192
Adjusting CGAIN to keep units constant	0.005	7FFFh	156.25	±5.12	16.384
	0.010	4000h	156.25	±5.12	16.384
	0.020	2000h	156.25	±5.12	16.384

AverageCurrent Register (0Bh)

The AverageCurrent register reports an average of current-register readings over a configurable 0.7s to 6.4h time period. See the FilterCFG register description for details on setting the time filter. The resulting average is placed in the AverageCurrent register with an LSb value of 1.5625µV/R_{SENSE}. The first Current register reading after device power-up sets the starting point of the AverageCurrent filter. The last value of the AverageCurrent register is maintained when the device enters shutdown mode. Figure 53 shows the AverageCurrent register format.

MaxMinCurrent Register (1Ch)

The MaxMinCurrent register maintains the maximum and minimum Current register values since the last fuel gauge reset or until cleared by host software. Each time the Current register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the MaxCurrent value is set to 80h (the minimum) and the MinCurrent value is set to 7Fh (the maximum). Therefore, both values are changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 807Fh. The maximum and minimum voltages are each stored as two's-complement 8-bit values with 0.4mV/R_{SENSE} resolution. Figure 54 shows the MaxMinCurrent register format.

CGAIN Register (2Eh)/COFF Register (2Fh)

The CGAIN and COFF registers adjust the gain and offset of the current measurement result. The current measurement A/D is factory trimmed to data-sheet accuracy without the need for the user to make further adjustments. The default power-up settings for CGAIN and COFF apply no adjustments to the Current register reading. For specific application requirements, the CGAIN and COFF registers can be used to adjust readings as follows:

Current Register = Current A/D Reading x
(CGAIN Register/16384) + (2 x COFF Register)

For easiest software compatibility between systems, configure CGAIN to keep current LSb resolution at 0.15625mA. A minimum sense resistance of 0.005Ω is required due to the maximum range of CGAIN. This preserves resolution of current readings and capacities.

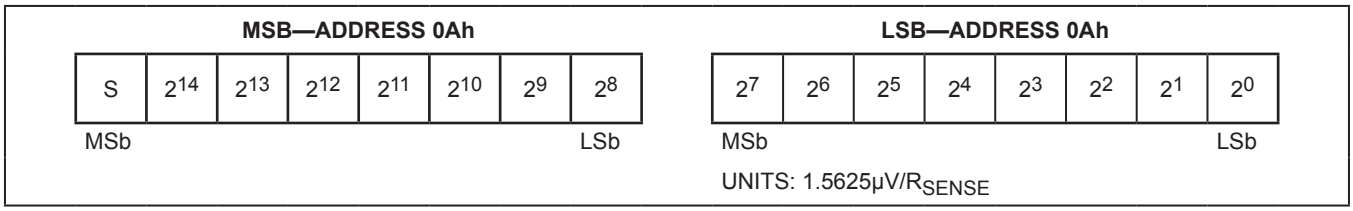


Figure 52. Current Register Format (Output)

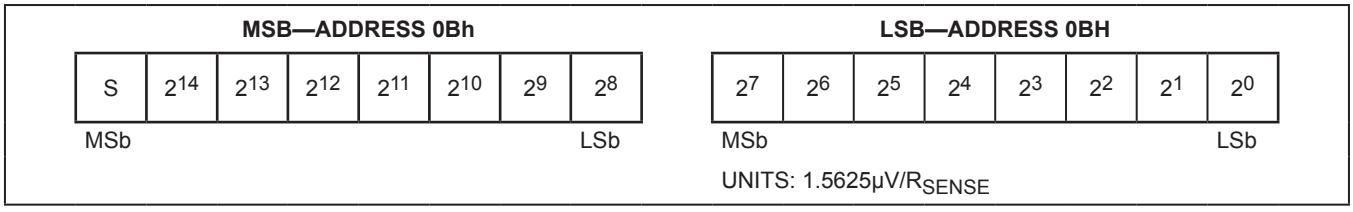


Figure 53. AverageCurrent Register Format (Output)

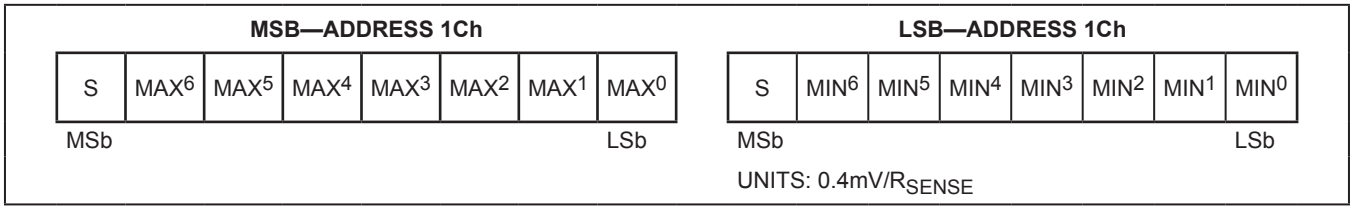


Figure 54. MaxMinCurrent Register Format (Output)

Both these registers are signed two's complement. The default values of 4000h for CGAIN and 0000h for COFF preserve factory calibration and unit values (1.5625µV). Figure 55 shows the CGAIN register format and Figure 56 shows the COFF register format.

Temperature Measurement

While in active mode and Ten = 1 in the CONFIG register, the device periodically measures the voltage between the AIN and CSP pins and compares the result to the voltage of the THRM pin. The device stores the result, a ratiometric value from 0 to 100%. The resulting data is placed in the AIN register every 1.4s with an LSb of 0.0122%.

Conversions are initiated by connecting the THRM and VTT pins internally. This enables the active pullup to the external voltage-divider network. After the pullup is enabled, the device waits for a settling period of t_{PRE} prior to making measurements on the AIN pin. When ETHRM = 1, FTHRM = 0, the active pullup is disabled when temperature measurements are complete. This feature limits the time the external resistor-divider network is active and lowers the total amount of energy used by the system.

When Tex = 0 and Ten = 1 in the CONFIG register, the device converts the AIN register to a temperature using the temperature gain (TGAIN) and temperature offset (TOFF) register values:

Temperature Register = (AIN Register x TGAIN Register/16384) + (TOFF Register x 2)

The resulting value is stored in the Temperature register each time the AIN register is updated. Additionally, the device maintains a record of the minimum and maximum temperature measured by the device, and an average temperature over a time period defined by the host. Table 4 lists the recommended TGAIN and TOFF register values for common NTC thermistors.

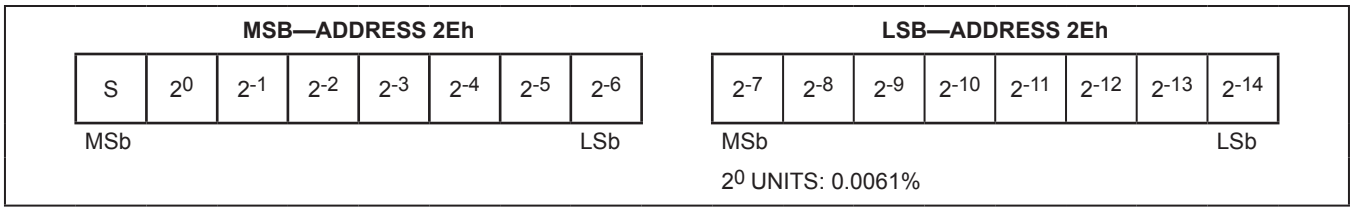


Figure 55. CGAIN Register Format (Input)

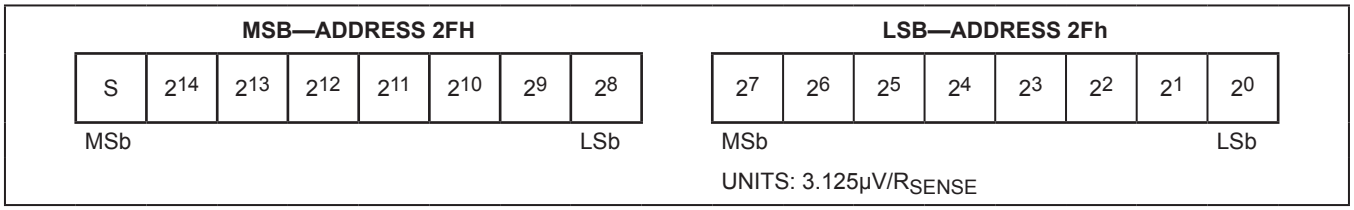


Figure 56. COFF Register Format (Input)

Table 4. Recommended TGAIN and TOFF Register Values for Common NTC Thermistors

THERMISTOR	R_{25C} (kΩ)	BETA	RECOMMENDED TGAIN	RECOMMENDED TOFF
Semitec 103AT-2	10	3435	E3E1h	290Eh
Fenwal 197-103LAG-A01	10	3974	E71Ch	251Ah
TDK Type F	10	4550	E989h	22B1h

When Tex = 1 in the CONFIG register, the device does not update the Temperature register based on results from the AIN pin A/D. Instead, host software must periodically write the Temperature register with the known application temperature to keep the fuel gauge accurate.

AIN Register (27h)

While in active mode and Ten = 1 in the CONFIG register, the device periodically measures the voltage between pins AIN and CSP and compares the result to the voltage of the THRM pin. The device stores the result, a ratiometric value from 0 to 100%. The resulting data is placed in the AIN register every 1.4s with an LSb of 0.0122%. Contents of the AIN register are indeterminate for the first conversion cycle time period after device power-up. The last value of the AIN register is maintained when the device enters shutdown mode or if Ten = 0 in the CONFIG register. Figure 57 shows the AIN register format.

Temperature Register (08h)

While in active mode and Tex = 0 and Ten = 1 in the CONFIG register, the device converts the AIN register value into a signed two's-complement temperature value. See the TGAIN and TOFF configuration registers. The resulting data is placed in the Temperature register every 1.4s with a resolution of +0.0039°C. If an 8-bit temperature reading is desired, the host can read only the upper byte of the Temperature register with a resolution of +1.0°C. Contents of the Temperature register are indeterminate for the first conversion cycle time period after device power-up. The last value of the Temperature register is maintained when the device enters shutdown mode. Figure 58 shows the Temperature register format.

AverageTemperature Register (16h)

The AverageTemperature register reports an average of temperature register readings over a configurable 6min to 12h time period. See the FilterCFG register (29h) description for details on setting the time filter. The resulting average is placed in the AverageTemperature register with an LSb value of 0.0039°C. The first Temperature register reading after device power-up sets the starting point of the AverageTemperature filter. The last value of the AverageTemperature register is maintained when the device enters shutdown mode. Figure 59 shows the AverageTemperature register format.

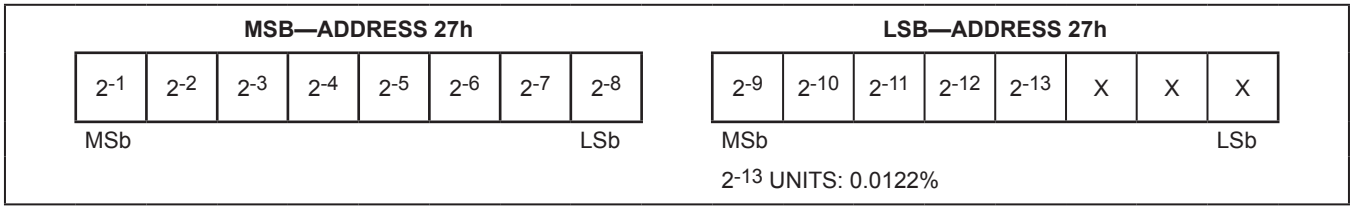


Figure 57. AIN Register Format (Output)

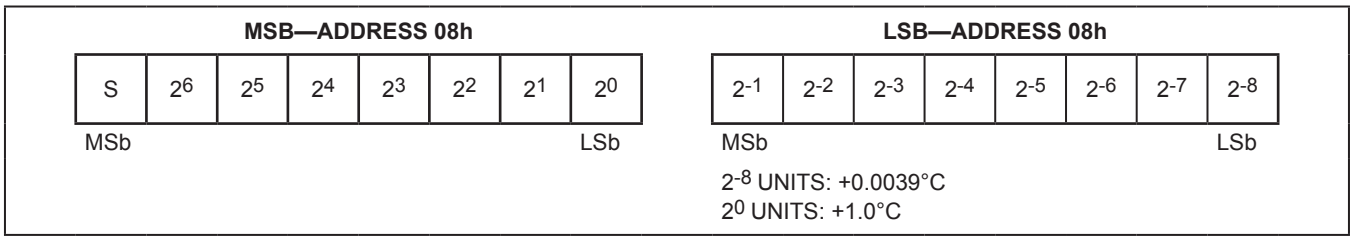


Figure 58. Temperature Register Format (Input/Output)

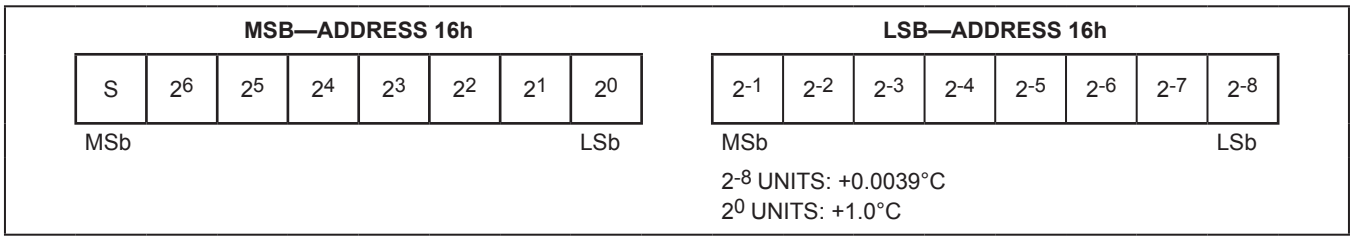


Figure 59. AverageTemperature Register Format (Output)

MaxMinTemperature Register (1Ah)

The MaxMinTemperature register maintains the maximum and minimum Temperature register values since the last fuel-gauge reset or until cleared by host software. Each time the Temperature register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding values are replaced with the new reading. At power-up, the MaxTemperature value is set to 80h (minimum) and the MinTemperature value is set to 7Fh (maximum). Therefore, both values are changed to the Temperature register reading after the first update. Host software can reset this register by writing it to its power-up value of 807Fh. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution. Figure 60 shows the MaxMinTemperature register format.

TGAIN Register (2Ch)/TOFF Register (2Dh)

The TGAIN and TOFF registers adjust the gain and offset of the temperature measurement A/D on the AIN pin to convert the result to a temperature value by the following equation:

Temperature Register = (AIN Register x TGAIN Register/16384) + (TOFF Register x 2)

Both these registers are signed two's complement. These registers allow for accurate temperature conversions when using a variety of external NTC thermistors (see Table 4). Figure 61 shows the TGAIN register format and Figure 62 shows the TOFF register format.

IC Memory Map

The device has a 256- word linear memory space containing all user-accessible registers. All registers are 16 bits wide and are read and written as 2-byte values. When the MSB of a register is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data command. This prevents updates to the LSB during the read, ensuring synchronization between the 2 register bytes.

All locations are volatile RAM and lose their data in the event of power loss. Data is retained during device shutdown. Each register has a power-on-reset value that it defaults to at power-up. Word addresses designated as reserved return an undetermined when read. These locations should not be written.

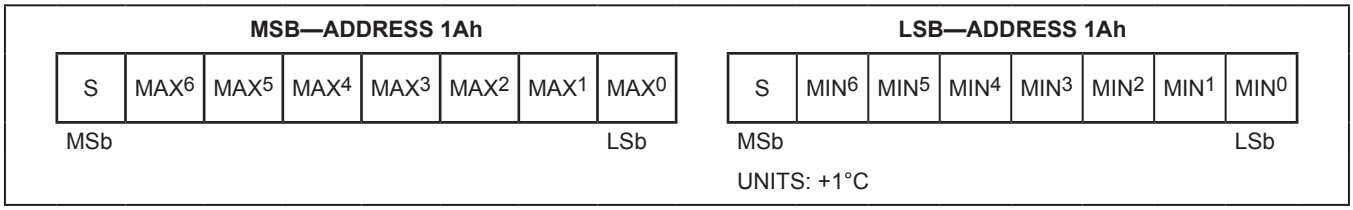


Figure 60. MaxMinTemperature Register Format (Output)

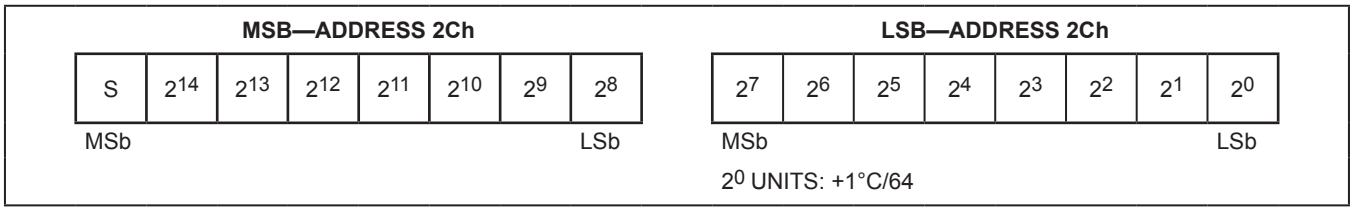


Figure 61. TGAIN Register Format (Input)

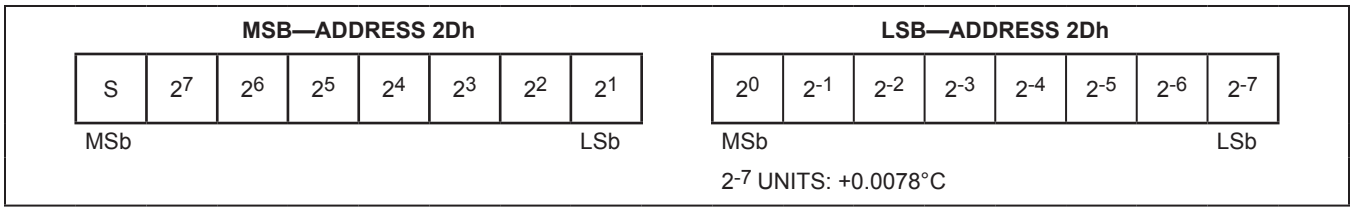


Figure 62. TOFF Register Format (Input)

Table 5. Device Memory Map

ADDRESS (HEX)	REGISTER NAME	A/D MEASURE	ALERT/ STATUS	MG m3 APP DATA	MG m3 CELL DATA	MG m3 CONFIG	MG m3 SAVE AND RESTORE	MG m3 OUTPUT	POR VALUE	READ/ WRITE
00h	Status		✓						0002h	R/W
01h	V_{ALRT} Threshold		✓						FF00h	R/W
02h	T_{ALRT} Threshold		✓						7F80h	R/W
03h	S_{ALRT} Threshold		✓						FF00h	R/W
04h	AtRate					✓			0000h	R/W
05h	$RemCap_{REP}$							✓	03E8h	R
06h	SOC_{REP}							✓	3200h	R
07h	Age							✓	6400h	R
08h	Temperature	✓							1600h	R/W
09h	V_{CELL}	✓							B400h	R
0Ah	Current	✓							0000h	R
0Bh	AverageCurrent	✓							0000h	R
0Ch	**RESERVED**								—	—
0Dh	SOC_{MIX}							✓	3200h	R
0Eh	SOC_{AV}							✓	3200h	R
0Fh	$RemCap_{MIX}$							✓	03E8h	R
10h	FullCAP						✓	✓	07D0h	R/W
11h	TTE							✓	0000h	R
12h	QResidual 00				✓		✓		1E2Fh	R/W
13h	FullSOCThr			✓					4600h	R/W
14h–15h	**RESERVED**								—	—
16h	AverageTemperature	✓							1600h	R
17h	Cycles						✓	✓	0000h	R/W
18h	DesignCap			✓					07D0h	R/W
19h	$AverageV_{CELL}$	✓							B400h	R
1Ah	MaxMinTemperature	✓							807Fh	R/W
1Bh	$MaxMinV_{CELL}$	✓							00FFh	R/W
1Ch	MaxMinCurrent	✓							807Fh	R/W
1Dh	CONFIG		✓						2350h	R/W
1Eh	ICHGTerm			✓					03C0h	R/W
1Fh	$RemCap_{AV}$							✓	03E8h	R
20h	**RESERVED**								—	—
21h	Version		✓						00ACh	R

Table 5. Device Memory Map (continued)

ADDRESS (HEX)	REGISTER NAME	A/D MEASURE	ALERT/ STATUS	MG m3 APP DATA	MG m3 CELL DATA	MG m3 CONFIG	MG m3 SAVE AND RESTORE	MG m3 OUTPUT	POR VALUE	READ/ WRITE
22h	QResidual 10				✓		✓		1E00h	R/W
23h	FullCapNom				✓			✓	07D0h	R/W
24h	TempNom				✓				1400h	R/W
25h	TempLim				✓				2305h	R/W
26h	**RESERVED**								—	—
27h	AIN	✓							88D0h	R
28h	LearnCFG					✓			2602h	R/W
29h	FilterCFG					✓			4EA4h	R/W
2Ah	RelaxCFG					✓			203Bh	R/W
2Bh	MiscCFG					✓			0870h	R/W
2Ch	TGAIN	✓							E3E1h	R/W
2Dh	TOFF	✓							290Eh	R/W
2Eh	CGAIN	✓							4000h	R/W
2Fh	COFF	✓							0000h	R/W
30h–31h	**RESERVED**								—	—
32h	QResidual 20				✓		✓		1306h	R/W
33h–35h	**RESERVED**								—	—
36h	Iavg_empty				✓				0780h	R/W
37h	FCTC				✓				05E0h	R/W
38h	RCOMP0				✓		✓		004Bh	R/W
39h	TempCo				✓		✓		262Bh	R/W
3Ah	V_empty			✓					9C5Ch	R/W
3Bh	**RESERVED**								—	—
3Ch	**RESERVED**								—	—
3Dh	FSTAT							✓	0001h	R
3Eh	TIMER		✓						0000h	R
3Fh	SHDNTIMER		✓						E000h	R/W
40h–41h	**RESERVED**								—	—
42h	QResidual 30				✓		✓		0C00h	R/W
43h–44h	**RESERVED**								—	—
45h	dQacc						✓		007Dh	R/W
46h	dPacc						✓		0C80h	R/W
47h–4Ch	**RESERVED**								—	—
4Dh	QH							✓	0000h	R/W
4Eh–7Fh	**RESERVED**								—	—
80h–AFh	Characterization Table				✓				N/A	R/W
B0h–FAh	**RESERVED**								—	—
FBh	VFOCV							✓	0000h	R
FCh–FEh	**RESERVED**								—	—
FFh	SOC_{VF}							✓	0000h	R

2-Wire Bus System

The 2-wire bus system supports operation as a slave-only device in a single or multislave, and single or multimaster system. Up to 128 slave devices may share the bus by uniquely setting the 7-bit slave address. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the IC (slave device) and a master device at speeds up to 400kHz. The device's SDA pin operates bidirectionally, that is, when the device receives data, SDA operates as an input, and when the device returns data, SDA operates as an open-drain output, with the host system providing a resistive pullup. The device always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits, which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low to high and then high to low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S), by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the device slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge (also called NACK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

Data Order

A byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSb) of each byte is followed by the Acknowledge bit. Device registers composed of multibyte values are ordered least significant byte (LSB) first.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address (SAddr) and the read/write (R/W) bit. When the bus is idle, the device continuously monitors for a START condition followed by its slave address. When the device receives a slave address that matches the value in its Programmable Slave Address register, it responds with an Acknowledge bit during the clock period following the R/W bit. The 7-bit Programmable Slave Address register is factory programmed and cannot be changed by the user.

IC SLAVE ADDRESS	0110110

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the slave by the master.

Bus Timing

The device is compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitor-

ing the acknowledge bit for presence of the device. More complex formats such as the write Data, read Data, and Function command protocols write data, read data, and execute device-specific operations, respectively. All bytes in each command format require the slave or the host system to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. Table 6 applies to the transaction formats.

Basic Transaction Formats

Write: S SAddr W A MAddr A DataL A DataH A P

A write transaction transfers 1 or more data bytes to the device. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

Read: S SAddr W A MAddr A Sr SAddr R A DataL A DataH N P

write Portion read Portion

A read transaction transfers one or more words from the IC. Read transactions are composed of two parts, a write portion followed by a read portion, and are therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to a 1. Control of SDA is assumed by the IC beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the device throughout the transaction, except for the Acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a No Acknowledge. This signals the device that control of SDA is to remain with the master following the Acknowledge clock.

Table 6. 2-Wire Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7 bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by Master	Data	Data byte returned by Slave
A	Acknowledge bit—Master	A	Acknowledge bit—Slave
N	No Acknowledge—Master	N	No Acknowledge—Slave

Write Data Protocol

The write Data protocol is used to write to register and shadow RAM data to the IC starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1, and DataN represents the last data byte written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit:

S SAddr W A MAddr A DataL0 A DataH0 A DataL1 A DataH1 A … DataLN A DataHN A P

The MSb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (LSb) of each byte is received by the device, the MSb of the data at address MAddr + 1 can be written immediately after the acknowledgment of the data at address MAddr. If the bus master continues an autoincremented write transaction beyond address FFh, the device ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations.

Read Data Protocol

The read data protocol is used to read register and shadow RAM data from the device starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1, and DataN represents the last byte read by the master:

S SAddr W A MAddr A Sr SAddr R A DataL0 A DataH0 A DataL1 A DataH1 A …DataLN N DataHN N P

Data is returned beginning with the most significant bit (MSb) of the data in MAddr. Because the address is automatically incremented after the LSb of each byte is returned, the MSb of the data at address MAddr +1 is available to the host system immediately after the acknowledgment of the data at address MAddr. If the bus master continues to read beyond address FFh, the device outputs data values of FFh. Addresses labeled Reserved in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or Repeated START.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17047G+	-40°C to +85°C	10 TDFN-EP*
MAX17047G+T10	-40°C to +85°C	10 TDFN-EP*
MAX17050X+	-40°C to +85°C	9 WLP
MAX17050X+T10	-40°C to +85°C	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1033+1	**21-0137**	**90-0003**
9 WLP	W91G1+1	**21-0755**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	12/11	Added MAX17050 and added multicell application circuit information, updated schematics, *Ordering Information*, layout guideline, and *Thermistor Sharing Circuit* section	1, 7, 8, 11–41, 43, 45
2	4/12	Corrected error on TDFN layout diagram in Figure 8 and corrected error of hard-coded bits of the LearnCFG register	14, 25, 43
3	8/12	Corrected error with FullSOCThr register formatting in Figure 25; corrected error with TOFF register formatting in Figure 62; added clarification that ALRTp bit must equal 0 to enable fast detection of cell removal	20, 30, 34, 42
4	12/14	Updated Figure 6	12
5	4/15	Updated the *Fuel-Gauge Learning and Age Support* and *LearnCFG Register (28h)* sections and Figure 33	11, 12, 25, 26
6	3/16	Corrected WLP package outline number	46
7	11/16	Updated front page title and applications	1

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