19-5036; Rev 0; 10/09

EVALUATION KIT AVAILABLE

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

General Description

The MAX11044/MAX11045/MAX11046† 16-bit ADCs offer 4, 6, or 8 independent input channels. Featuring independent track and hold (T/H) and SAR circuitry, these parts provide simultaneous sampling at 250ksps for each channel.

The MAX11044/MAX11045/MAX11046 accept a ±5V input. All inputs are overrange protected with internal ±20mA input clamps providing overrange protection with a simple external resistor. Other features include a 4MHz T/H input bandwidth, internal clock, and internal or external reference. A 20MHz, 16-bit, bidirectional, parallel interface provides the conversion results and accepts digital configuration inputs.

The MAX11044/MAX11045/MAX11046 operate with a 4.75V to 5.25V analog supply and a separate flexible 2.7V to 5.25V digital supply for interfacing with the host without a level shifter. The MAX11044/MAX11045/MAX11046 are available in a 56-pin TQFN package and operate over the extended -40°C to +85°C temperature range.

Applications

Automatic Test Equipment

Power-Factor Monitoring and Correction

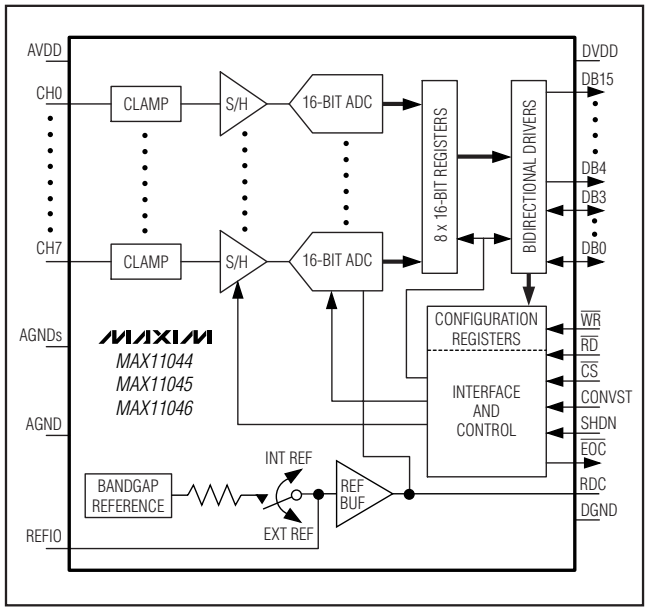
Power-Grid Protection

Multiphase Motor Control

Vibration and Waveform Analysis

†*Patent pending.*

Functional Diagram



Features

- ♦ **4-/6-/8-Channel 16-Bit ADC**
- ♦ **Single Analog and Digital Supply**
- ♦ **High-Impedance Inputs Up to 1GΩ**
- ♦ **On-Chip T/H Circuit for Each Channel**
- ♦ **Fast 3µs Conversion Time**
- ♦ **High Throughput: 250ksps for All 8 Channels**
- ♦ **16-Bit, High-Speed, Parallel Interface**
- ♦ **Internal Clocked Conversions**
- ♦ **10ns Aperture Delay**
- ♦ **100ps Channel-to-Channel T/H Matching**
- ♦ **Low Drift, Accurate 4.096V Internal Reference Providing an Input Range of ±5V**
- ♦ **External Reference Range of 3.0V to 4.25V, Allowing Full-Scale Input Ranges of ±4.0V to ±5.2V**
- ♦ **56-Pin TQFN Package (8mm x 8mm)**
- ♦ **Evaluation Kit Available**

Ordering Information

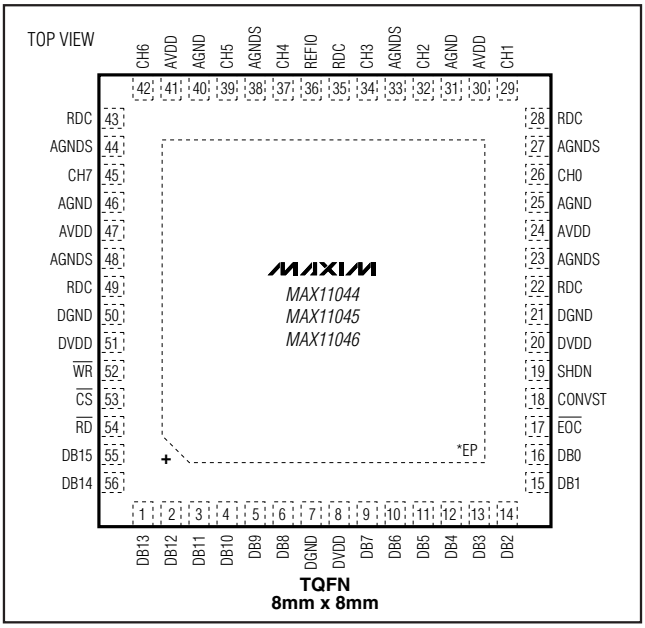
PART	PIN-PACKAGE	CHANNELS
MAX11044ETN+	56 TQFN-EP*	4
MAX11045ETN+	56 TQFN-EP*	6
MAX11046ETN+	56 TQFN-EP*	8

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +6V
DVDD to AGND and DGND .....-0.3V to +6V
DGND to AGND.....-0.3V to +0.3V
AGNDS to AGND.....-0.3V to +0.3V
CH0–CH7 to AGND .....-7.5V to +7.5V
REFIO, RDC to AGND .....-0.3V to the lower of (AVDD + 0.3V) and +6V
$\overline{EOC}$, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, CONVST to AGND.....-0.3V to the lower of (DVDD + 0.3V) and +6V
DB0–DB15 to AGND .....-0.3V to the lower of (DVDD + 0.3V) and +6V
Maximum Current into Any Pin Except AVDD, DVDD, AGND, DGND .....±50mA
Continuous Power Dissipation
56-Pin TQFN (derate 36mW/°C above +70°C) 2222mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AVDD = +4.75V to +5.25V, DVDD = +2.70V to +5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF || 10µF, C_{DVDD} = 3 x 0.1µF || 10µF; all digital inputs at DVDD or DGND, unless otherwise noted, f_{SAMPLE} = 250ksps. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		16			Bits
Integral Nonlinearity	INL	(Note 2)	>-2	±0.8	<+2	LSB
		(Note 3)		±0.7		
Differential Nonlinearity	DNL	(Note 4)	> -1	±0.5	< +1.2	LSB
		(Note 5)	> -1	±0.7	< +1.5	
		(Note 3)		±0.45		
No Missing Codes			16			Bits
Offset Error				±0.002	±0.01	%FSR
Channel Offset Matching					±0.01	%FSR
Offset Temperature Coefficient				±2.4		µV/°C
Gain Error					±0.03	%FSR
Positive Full-Scale Error					±0.02	%FSR
Negative Full-Scale Error					±0.02	%FSR
Positive Full-Scale Error Matching					±0.02	%FSR
Negative Full-Scale Error Matching					±0.02	%FSR
Channel Gain-Error Matching		Between all channels			±0.03	%FSR
Gain Temperature Coefficient				±0.8		ppm/°C
DYNAMIC PERFORMANCE (Note 6)						
Signal-to-Noise Ratio	SNR	f_{IN} = 10kHz, full-scale input	91	92.3		dB
Signal-to-Noise and Distortion Ratio	SINAD	f_{IN} = 10kHz, full-scale input	90.5	92		dB
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10kHz, full-scale input	95	106		dB
Total Harmonic Distortion	THD	f_{IN} = 10kHz, full-scale input		-105	-95	dB
Channel-to-Channel Crosstalk		f_{IN} = 60Hz, full scale and ground on adjacent channel (Note 7)		-126	-100	dB

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +4.75V to +5.25V, DVDD = +2.70V to +5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ll 10µF, C_{DVDD} = 3 x 0.1µF ll 10µF; all digital inputs at DVDD or DGND, unless otherwise noted, f_{SAMPLE} = 250ksps. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS (CH0–CH7)						
Input-Voltage Range		(Note 8)			±1.22 x V_{REFIO}	V
Input Leakage Current			-1		+1	µA
Input Capacitance				15		pF
Input-Clamp Protection Current		Each input simultaneously	-20		+20	mA
TRACK AND HOLD						
Throughput Rate		Per channel, 8 channels in 4µs	1		250	ksps
Acquisition Time	t_{ACQ}		1		1000	µs
Full-Power Bandwidth		-3dB point		4		MHz
		-0.1dB point		> 0.2		
Aperture Delay				10		ns
Aperture-Delay Matching				100		ps
Aperture Jitter				50		ps_{RMS}
INTERNAL REFERENCE						
REFIO Voltage	V_{REF}		4.073	4.096	4.119	V
REFIO Temperature Coefficient				±5		ppm/°C
EXTERNAL REFERENCE						
Input Current			-10		+10	µA
REF Voltage-Input Range	V_{REF}		3.00		4.25	V
REF Input Capacitance				15		pF
DIGITAL INPUTS (DB0–DB15, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CONVST)						
Input Voltage High	V_{IH}	V_{DVDD} = 2.7V to 5.25V	2			V
Input Voltage Low	V_{IL}	V_{DVDD} = 2.7V to 5.25V			0.8	V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{DVDD}			±10	µA
DIGITAL OUTPUTS (DB0–DB15, $\overline{EOC}$)						
Output Voltage High	V_{OH}	I_{SOURCE} = 1.2mA	V_{DVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA		0.25	0.4	V
Three-State Leakage Current		DB0–DB15, $V_{\overline{RD}} \geq V_{IH}$ or $V_{\overline{CS}} \geq V_{IH}$			10	µA
Three-State Output Capacitance		DB0–DB15, $V_{\overline{RD}} \geq V_{IH}$ or $V_{\overline{CS}} \geq V_{IH}$		15		pF
POWER SUPPLIES						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	I_{AVDD}	MAX11046, AVDD = 5V			48	mA
		MAX11045, AVDD = 5V			42	
		MAX11044, AVDD = 5V			36	

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +4.75V to +5.25V, DVDD = +2.70V to +5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ll 10µF, C_{DVDD} = 3 x 0.1µF ll 10µF; all digital inputs at DVDD or DGND, unless otherwise noted, f_{SAMPLE} = 250ksps. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Current	I_{DVDD}	MAX11046, DVDD = 3.3V (Note 9)			7.3	mA
		MAX11045, DVDD = 3.3V (Note 9)			6.3	mA
		MAX11044, DVDD = 3.3V (Note 9)			5.5	mA
Shutdown Current	I_{DVDD}				10	µA
	I_{AVDD}				12	
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 4.9V to 5.1V (Note 10)		±3		LSB
TIMING CHARACTERISTICS (Note 9)						
CONVST Rise to $\overline{EOC}$	t_{CON}	Conversion time (Note 11)			3	µs
Acquisition Time	t_{ACQ}		1		1000	µs
$\overline{CS}$ Rise to CONVST Rise	t_Q	Sample quiet time (Note 11)	500			ns
CONVST Rise to $\overline{EOC}$ Rise	t_0			47	140	ns
$\overline{EOC}$ Fall to CONVST Fall	t_1	CONVST mode B0 = 0 only (Note 12)	0			ns
CONVST Low Time	t_2	CONVST mode B0 = 1 only	20			ns
$\overline{CS}$ Fall to $\overline{WR}$ Fall	t_3		0			ns
$\overline{WR}$ Low Time	t_4		20			ns
$\overline{CS}$ Rise to $\overline{WR}$ Rise	t_5		0			ns
Input Data Setup Time	t_6		10			ns
Input Data Hold Time	t_7		1			ns
$\overline{CS}$ Fall to $\overline{RD}$ Fall	t_8		0			ns
$\overline{RD}$ Low Time	t_9		30			ns
$\overline{RD}$ Rise to $\overline{CS}$ Rise	t_{10}		0			ns
$\overline{RD}$ High Time	t_{11}		10			ns
$\overline{RD}$ Fall to Data Valid	t_{12}				35	ns
$\overline{RD}$ Rise to Data Hold Time	t_{13}	(Note 12)	5			ns

Note 1: See the *Definitions* section at the end of the data sheet.

Note 2: INL is guaranteed at AVDD = 5.25V, for +25°C < T_A < +85°C. See the *Input Range and Protection* section and *Typical Operating Characteristics.*

Note 3: T_A = -40°C.

Note 4: DNL at code > 8192 or < 57343 (offset binary encoded), or code > -24576 or < +24575 (two's complement), is guaranteed at AVDD = 5.25V, for +25°C < T_A < +85°C. See the *Input Range and Protection* section and *Typical Operating Characteristics.*

Note 5: DNL at code ≤ 8192 or ≥ 57343 (offset binary encoded), or code ≤ -24576 or ≥ +24575 (2's complements), is guaranteed at AVDD = 5.25V, for +25°C < T_A < +85°C. See the I*nput Range and Protection* section and *Typical Operating Characteristics.*

Note 6: AC dynamics are guaranteed at AVDD = 5.25V, for +25°C < T_A < +85°C. See the *Input Range and Protection* section and *Typical Operating Characteristics.*

Note 7: Tested with alternating channels modulated at full scale and ground.

Note 8: See the *Input Range and Protection* section for more details.

Note 9: C_{LOAD} = 30pF on DB0–DB15 and EOC. Inputs (CH0–CH7) alternate between full scale and zero scale. f_{CONV} = 250ksps. All data is read out.

Note 10: Defined as the change in positive full scale caused by a ±2% variation in the nominal supply voltage.

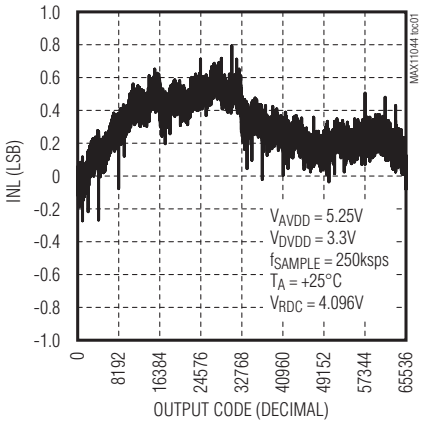
Note 11: It is recommended that $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are kept high for the quiet time (t_Q) and conversion time (t_{CON}).

Note 12: Guaranteed by design.

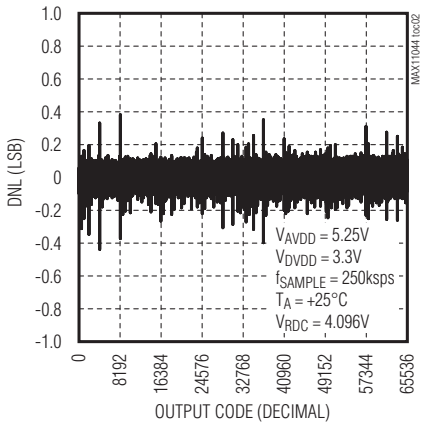
Typical Operating Characteristics

(AVDD = 5V, DVDD = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

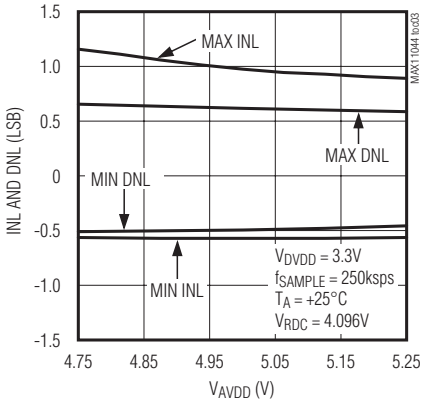
INTEGRAL NONLINEARITY vs. CODE



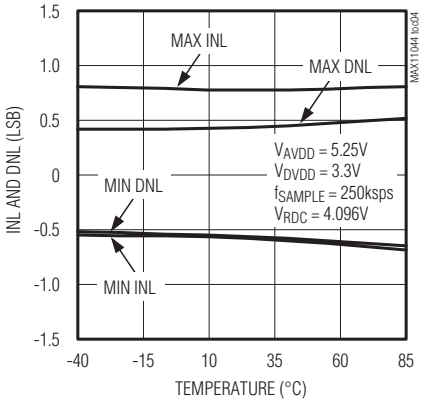
DIFFERENTIAL NONLINEARITY vs. CODE



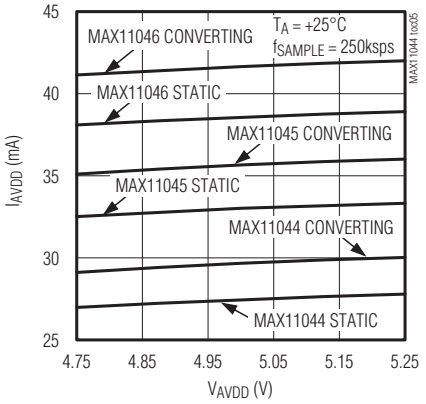
INL AND DNL vs. ANALOG SUPPLY VOLTAGE



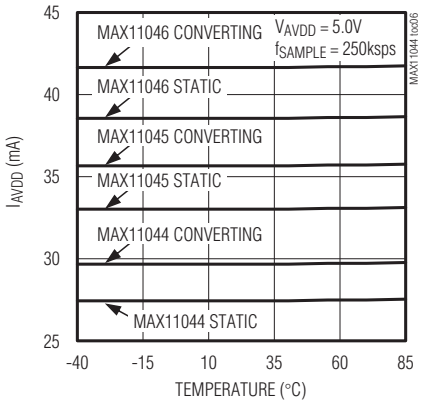
INL AND DNL vs. TEMPERATURE



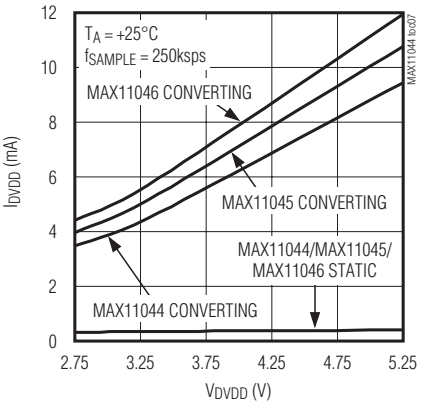
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. TEMPERATURE



DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE

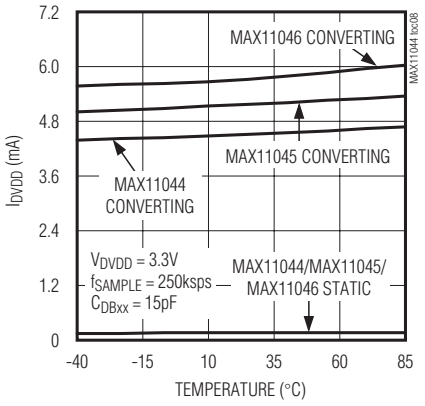


4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

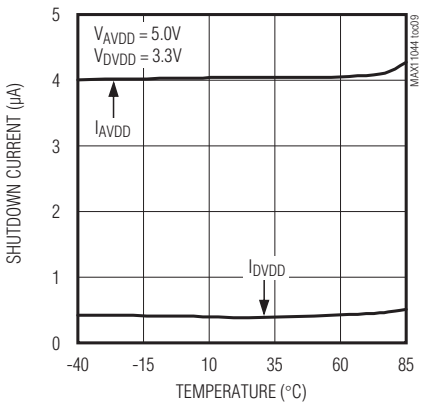
Typical Operating Characteristics (continued)

(AVDD = 5V, DVDD = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

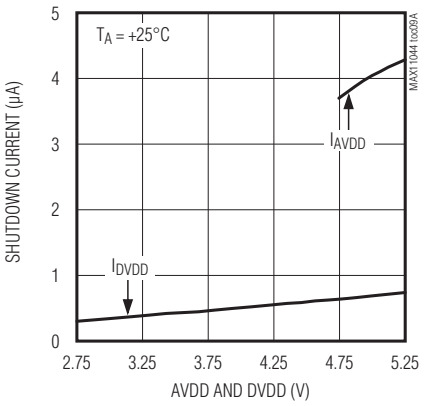
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



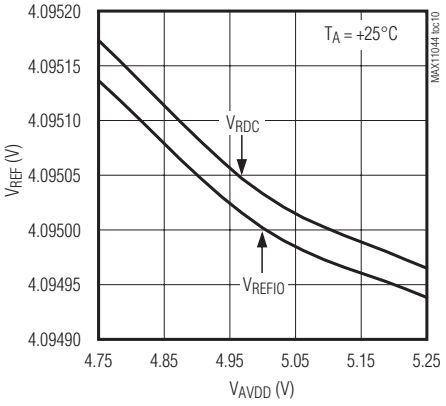
ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE



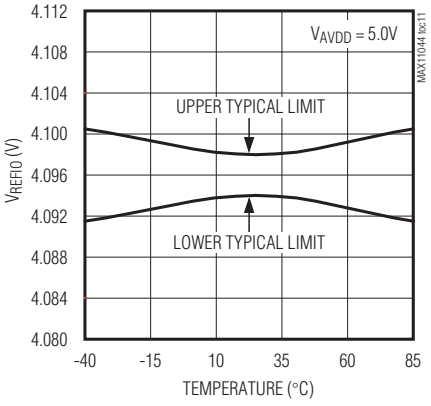
ANALOG AND DIGITAL SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



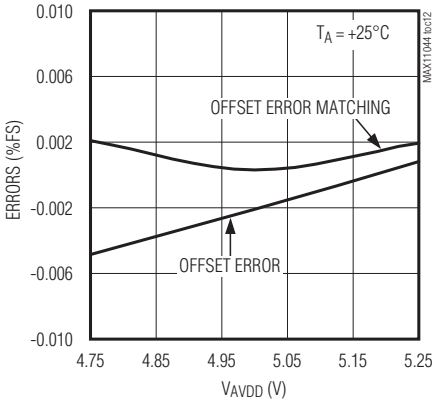
INTERNAL REFERENCE VOLTAGES vs. SUPPLY VOLTAGE



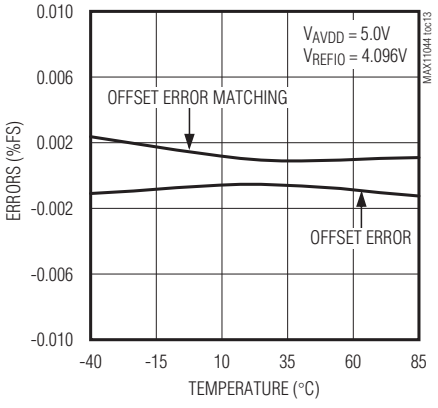
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



OFFSET ERROR AND OFFSET ERROR MATCHING vs. SUPPLY VOLTAGE



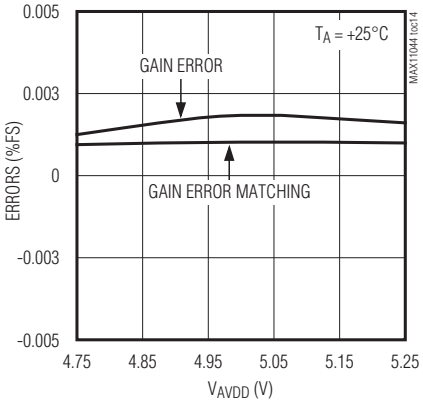
OFFSET ERROR AND OFFSET ERROR MATCHING vs. TEMPERATURE



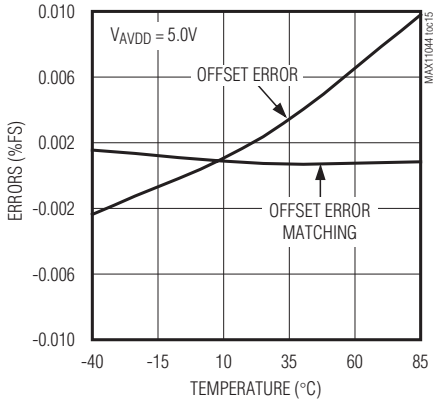
Typical Operating Characteristics (continued)

(AVDD = 5V, DVDD = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

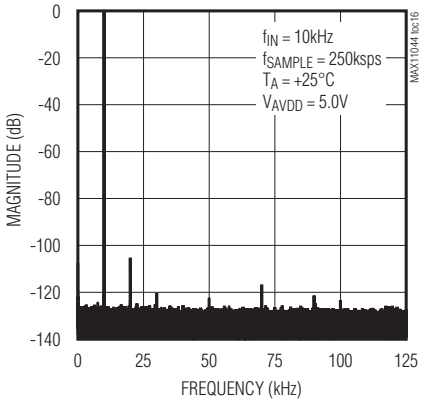
GAIN ERROR AND GAIN ERROR MATCHING vs. SUPPLY VOLTAGE



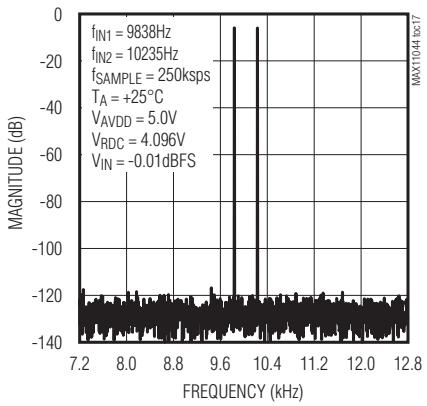
GAIN ERROR AND GAIN ERROR MATCHING vs. TEMPERATURE



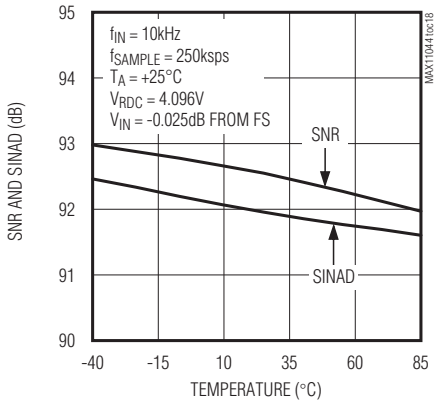
FFT PLOT



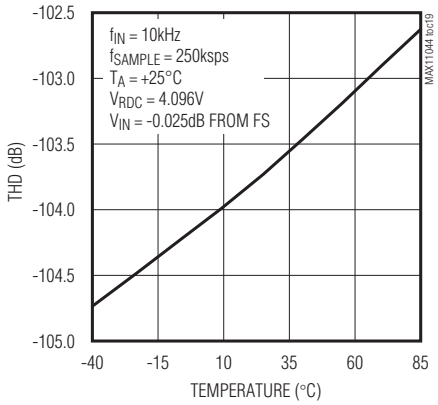
TWO-TONE IMD PLOT



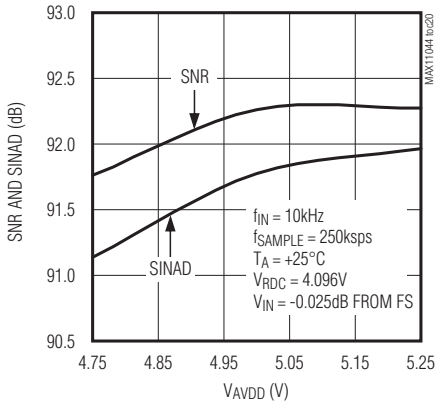
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE AND DISTORTION RATIO vs. TEMPERATURE



TOTAL HARMONIC DISTORTION vs. TEMPERATURE



SNR AND SINAD vs. ANALOG SUPPLY VOLTAGE

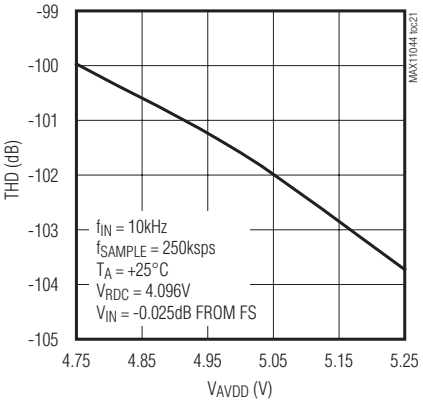


4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

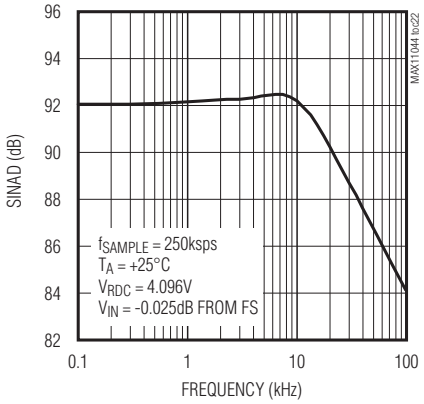
Typical Operating Characteristics (continued)

(AVDD = 5V, DVDD = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

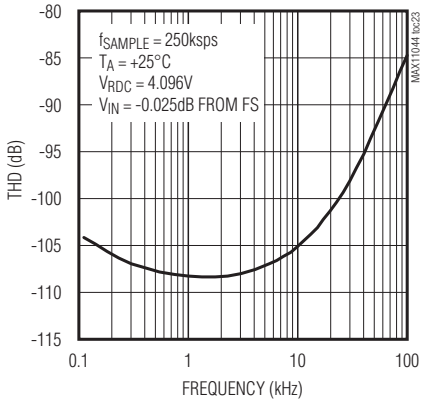
TOTAL HARMONIC DISTORTION vs. ANALOG SUPPLY VOLTAGE



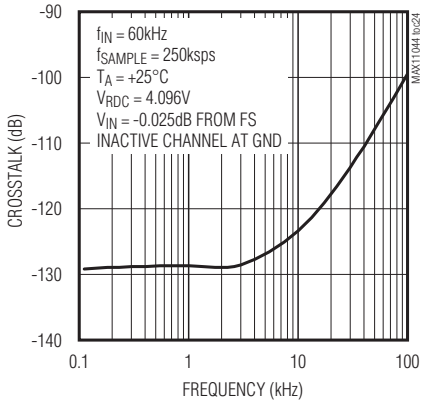
SIGNAL-TO-NOISE AND DISTORTION RATIO vs. FREQUENCY



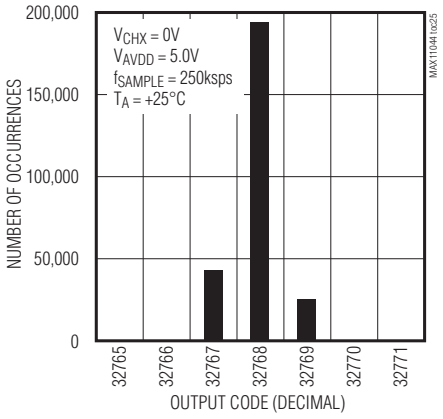
THD vs. INPUT FREQUENCY



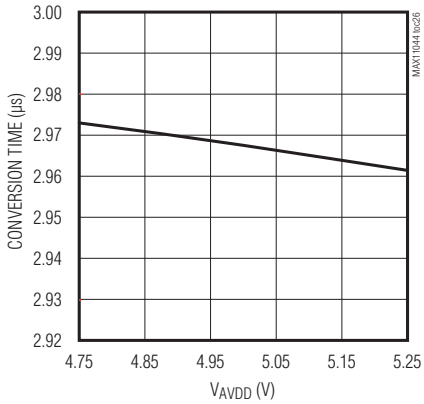
CROSSTALK vs. FREQUENCY



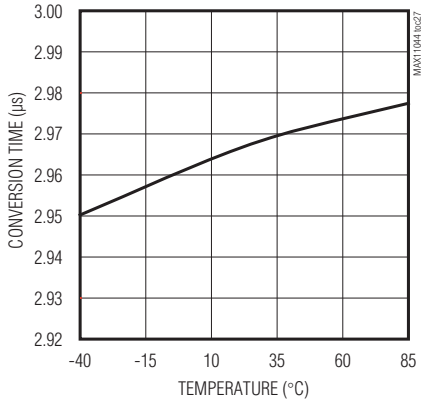
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO GND



CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE



CONVERSION TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	DB13	16-Bit Parallel Data Bus Digital Output Bit 13
2	DB12	16-Bit Parallel Data Bus Digital Output Bit 12
3	DB11	16-Bit Parallel Data Bus Digital Output Bit 11
4	DB10	16-Bit Parallel Data Bus Digital Output Bit 10
5	DB9	16-Bit Parallel Data Bus Digital Output Bit 9
6	DB8	16-Bit Parallel Data Bus Digital Output Bit 8
7, 21, 50	DGND	Digital Ground
8, 20, 51	DVDD	Digital Supply. Bypass to DGND with a 0.1µF capacitor at each DVDD input.
9	DB7	16-Bit Parallel Data Bus Digital Output Bit 7
10	DB6	16-Bit Parallel Data Bus Digital Output Bit 6
11	DB5	16-Bit Parallel Data Bus Digital Output Bit 5
12	DB4	16-Bit Parallel Data Bus Digital Output Bit 4
13	DB3	16-Bit Parallel Data Bus Digital I/O Bit 3
14	DB2	16-Bit Parallel Data Bus Digital I/O Bit 2
15	DB1	16-Bit Parallel Data Bus Digital I/O Bit 1
16	DB0	16-Bit Parallel Data Bus Digital I/O Bit 0
17	$\overline{EOC}$	Active-Low, End-of-Conversion Output. $\overline{EOC}$ goes low when a conversion is completed. $\overline{EOC}$ goes high when a conversion is initiated.
18	CONVST	Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0.
19	SHDN	Shutdown Input. If SHDN is held high, the entire device will enter and stay in a low-current state. Contents of the configuration register are not lost when in the shutdown state.
22, 28, 35, 43, 49	RDC	Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least a 80µF total capacitance. See the *Layout, Grounding, and Bypassing* section.
23, 27, 33, 38, 44, 48	AGNDS	Signal Ground. Connect all AGND and AGNDS inputs together.
24, 30, 41, 47	AVDD	Analog Supply Input. Bypass AVDD to AGND with a 0.1µF capacitor at each AVDD input.
25, 31, 40, 46	AGND	Analog Ground. Connect all AGND inputs together.
26	CH0	Channel 0 Analog Input
29	CH1	Channel 1 Analog Input
32	CH2	Channel 2 Analog Input
34	CH3	Channel 3 Analog Input
36	REFIO	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND.
37	CH4	Channel 4 Analog Input
39	CH5	Channel 5 Analog Input

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

Pin Description (continued)

PIN	NAME	FUNCTION
42	CH6	Channel 6 Analog Input
45	CH7	Channel 7 Analog Input
52	$\overline{WR}$	Active-Low Write Input. Drive $\overline{WR}$ low to write to the ADC. Configuration registers are loaded on the rising edge of $\overline{WR}$.
53	$\overline{CS}$	Active-Low Chip-Select Input. Drive $\overline{CS}$ low when reading from or writing to the ADC.
54	$\overline{RD}$	Active-Low Read Input. Drive $\overline{RD}$ low to read from the ADC. Each rising edge of $\overline{RD}$ advances the channel output on the data bus.
55	DB15	16-Bit Parallel Data Bus Digital Out Bit 15
56	DB14	16-Bit Parallel Data Bus Digital Out Bit 14
—	EP	Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX11044/MAX11045/MAX11046 are fast, low-power ADCs that combine 4, 6, or 8 independent ADC channels in a single IC. Each channel includes simultaneously sampling independent T/H circuitry that preserves relative phase information between inputs making the MAX11044/MAX11045/MAX11046 ideal for motor control and power monitoring. The MAX11044/MAX11045/MAX11046 are available with ±5V input ranges that feature ±20mA overrange, fault-tolerant inputs. The MAX11044/MAX11045/MAX11046 operate with a single 4.75V to 5.25V supply. A separate 2.7V to 5.25V supply for digital circuitry makes the devices compatible with low-voltage processors.

The MAX11044/MAX11045/MAX11046 perform conversions for all channels in parallel by activating independent ADCs. Results are available through a high-speed, 20MHz, parallel data bus after a conversion time of 3µs following the end of a sample. The data bus is bidirectional and allows for easy programming of the configuration register. The MAX11044/MAX11045/MAX11046 feature a reference buffer, which is driven by an internal bandgap reference circuit (V_{REFIO} = 4.096V). Drive REFIO with an external reference or bypass with 0.1µF capacitor to ground when using the internal reference.

Analog Inputs

Track and Hold (T/H)

To preserve phase information across all channels, each input includes a dedicated T/H circuitry. The input tracking circuitry provides a 4MHz small-signal bandwidth, enabling the device to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

Input Range and Protection

The full-scale analog input voltage is a product of the reference voltage. For the MAX11044/MAX11045/MAX11046, the full-scale input is bipolar in the range of:

$$\pm(V_{REFIO} \times \frac{5}{4.096})$$

When in external reference mode, drive V_{REFIO} with a 3.0V to 4.25V source, resulting in an input range of ±3.662V to ±5.188V, respectively.

All analog inputs are fault-protected to up to ±20mA. The MAX11044/MAX11045/MAX11046 include an input clamping circuit that activates when the input voltage at the analog input is above (V_{AVDD} + 300mV) or below –(V_{AVDD} + 300mV). The clamp circuit remains high impedance while the input signal is within the range of ±V_{AVDD} and draws little or almost no current. However, when the input signal exceeds ±V_{AVDD}, the clamps begin to turn on and shunt current to/from the AVDD supply. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed ±V_{AVDD}.

Note that the input clamp circuit also has a small amount of hysteresis and once triggered remains engaged, shunting current to/from AVDD until the input returns to within the convertible range by several hundredths of a volt. This effect can cause some errors at the extremes of the transfer function if V_{IN} is driven beyond ±V_{AVDD}.

To make use of the input clamps (see Figure 1), connect a resistor (R_S) between the analog input and the voltage source to limit the voltage at the analog input so that the fault current into the MAX11044/MAX11045/MAX11046 does not exceed ±20mA. Note that the voltage at the analog input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$R_S = \frac{V_{FAULT_MAX} - 7V}{20mA}$$

where V_{FAULT_MAX} is the maximum voltage that the source produces during a fault condition.

Figures 2 and 3 illustrate the clamp circuit voltage-current characteristics for a source impedance R_S = 1280Ω. While the input voltage is within the ±(V_{AVDD} + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

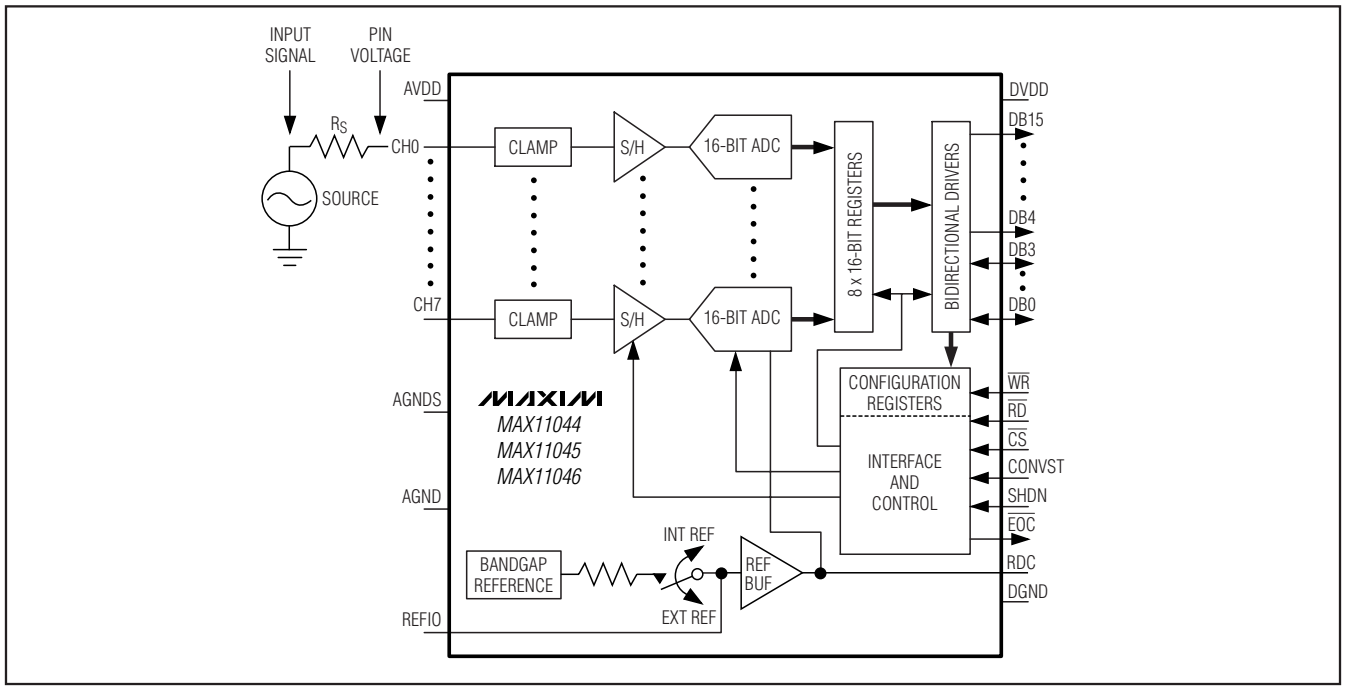


Figure 1. Required Setup for Clamp Circuit

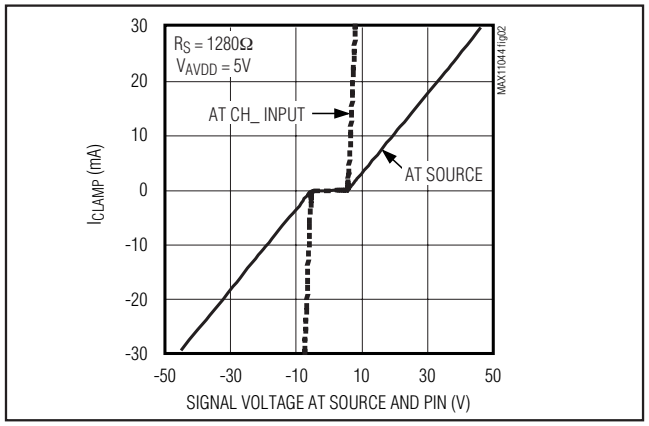


Figure 2. Input Clamp Characteristics

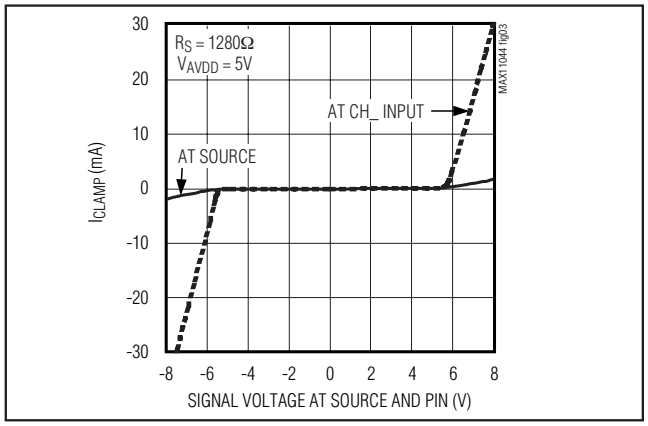


Figure 3. Input Clamp Characteristics (Zoom In)

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

Applications Information

Digital Interface

The bidirectional, parallel, digital interface, DB0–DB3, sets the 4-bit configuration register. This interface configures the following control signals: chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), end of conversion ($\overline{EOC}$), and convert start (CONVST). Figures 6 and 7 and the Timing Characteristics in the *Electrical Characteristics* table show the operation of the interface. DB0–DB3, together with the output-only DB4–DB15, also output the 16-bit conversion result. All bits are high impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.

DB3 (Int/Ext Reference)

DB3 selects the internal or external reference. The POR default = 0.

0 = internal reference, REFIO internally driven through a 10kΩ resistor, bypass with 0.1µF capacitor to AGND.

1 = external reference, drive REFIO with a high-quality reference.

DB2 (Output Data Format)

DB2 selects the output data format. The POR default = 0.

0 = offset binary.

1 = two's complement.

DB1 (Reserved)

Set to 0 for normal operation.

0 = normal operation.

1 = reserved; do not use.

DB0 (CONVST Mode)

DB0 selects the acquisition mode. The POR default = 0.

0 = CONVST controls the acquisition and conversion. Drive CONVST low to start acquisition. The rising edge of CONVST begins the conversion.

1 = acquisition mode starts as soon as the previous conversion is complete. The rising edge of CONVST begins the conversion.

Programming the Configuration Register

To program the configuration register, bring the $\overline{CS}$ and $\overline{WR}$ low and apply the required configuration data on DB3–DB0 of the bus and then raise $\overline{WR}$ once to save changes.

Table 1. Configuration Register

DB3	DB2	DB1	DB0
Int/Ext Reference	Output Data Format	Reserved	CONVST Mode

Starting a Conversion

CONVST initiates conversions. The MAX11044/MAX11045/MAX11046 provide two acquisition modes set through the configuration register. Allow a quiet time (t_Q) of 500ns prior to the start of conversion to avoid any noise interference during readout or write operations from corrupting a sample.

In default mode (DB0 = 0), drive CONVST low to place the MAX11044/MAX11045/MAX11046 into acquisition mode. All the input switches are closed and the internal T/H circuits track the respective input voltage. Keep the CONVST signal low for at least 1µs (t_{ACQ}) to enable proper settling of the sampled voltages. On the rising edge of CONVST, the switches are opened and the MAX11044/MAX11045/MAX11046 begin the conversion on all the samples in parallel. $\overline{EOC}$ remains high until the conversion is completed.

In the second mode (DB0 = 1), the MAX11044/MAX11045/MAX11046 enter acquisition mode as soon as the previous conversion is completed. CONVST rising edge initiates the next sample and conversion sequence. CONVST needs to be low for at least 20ns to be valid.

Provide adequate time for acquisition and the requisite quiet time in both modes to achieve accurate sampling and maximum performance of the MAX11044/MAX11045/MAX11046.

Reading Conversion Results

The $\overline{CS}$ and $\overline{RD}$ are active-low, digital inputs that control the readout through the 16-bit, parallel, 20MHz data bus (D0–D15). After $\overline{EOC}$ transitions low, read the conversion data by driving $\overline{CS}$ and $\overline{RD}$ low. Each low period of $\overline{RD}$ presents the next channel's result. When $\overline{CS}$ and $\overline{RD}$ are high, the data bus is high impedance. $\overline{CS}$ may be driven high between individual channel readouts or left low during the entire 8-channel readout.

Reference

Internal Reference

The MAX11044/MAX11045/MAX11046 feature a precision, low-drift, internal bandgap reference. Bypass REFIO with a 0.1µF capacitor to AGND to reduce noise. The REFIO output voltage may be used as a reference for other circuits. The output impedance of REFIO is 10kΩ. Drive only high impedance circuits or buffer externally when using REFIO to drive external circuitry.

External Reference

Set the configuration register to disable the internal reference and drive REFIO with a high-quality external reference. To avoid signal degradation, ensure that the integrated reference noise applied to REFIO is less than 10µV in the bandwidth of up to 50kHz.

Reference Buffer

The MAX11044/MAX11045/MAX11046 have a built-in reference buffer to provide a low-impedance reference source to the SAR converters. This buffer is used in both internal and external reference mode. The reference buffer output feeds five RDC pins. The RDC pins should be all connected together on the PCB. The reference buffer is externally compensated and requires at least 10µF on the RDC node. For best performance, provide a total of at least 80µF on the RDC outputs.

Transfer Functions

Figures 8 and 9 show the transfer functions for all the formats and devices. Code transitions occur halfway between successive-integer LSB values.

Layout, Grounding, and Bypassing

For best performance use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect DGND, AGND, and AGNDS pins on the MAX11044/MAX11045/MAX11046 to this ground plane. Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

To achieve the highest performance, connect all the RDC pins (22, 28, 36, 43, and 49) to a local RDC plane on the PCB. A total of at least 80µF of capacitance should be placed on this RDC plane. If two capacitors are used, place each as close as possible to pins 22 and 49. If four capacitors are used, place each as close as possible to pins 22, 28, 43, and 49. For example, two 47µF, 10V X5R capacitors in 1210 case size can be placed as close as possible to pins 22 and 49 will provide excellent performance. Alternatively, four 22µF, 10V X5R capacitors in 1210 case size placed as close as possible to pins 22, 28, 43, and 49 will also provide good performance. Ensure that each capacitor is connected directly into the GND plane with an independent via.

If Y5U or Z5U ceramics are used, be aware of the high-voltage coefficient these capacitors exhibit and select higher voltage rating capacitors to ensure that at least 80µF of capacitance is on the RDC plane when the plane is driven to 4.096V by the built-in reference buffer. For example, a 22µF X5R with a 10V rating is approximately 20µF at 4.096V, whereas, the same capacitor in Y5U ceramic is just 13µF. However, a Y5U 22µF capacitor with a 25V rating cap is approximately 20µF at 4.096V.

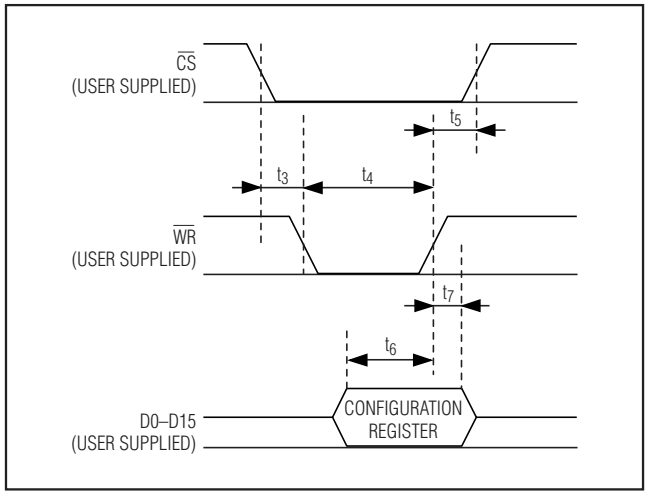


Figure 4. Programming Configuration-Register Timing Requirements

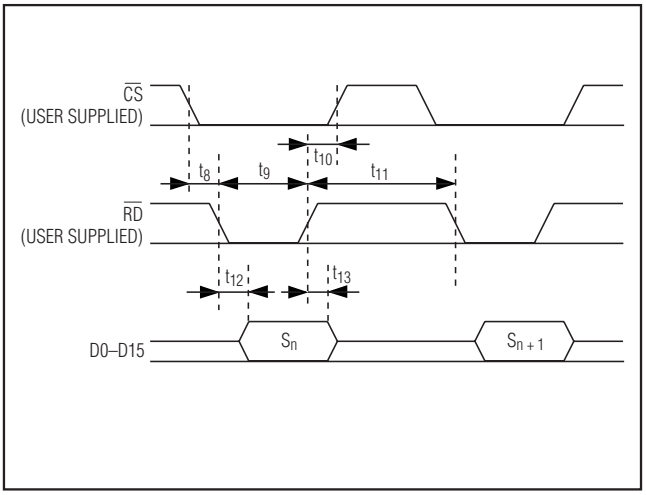


Figure 5. Readout Timing Requirements

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

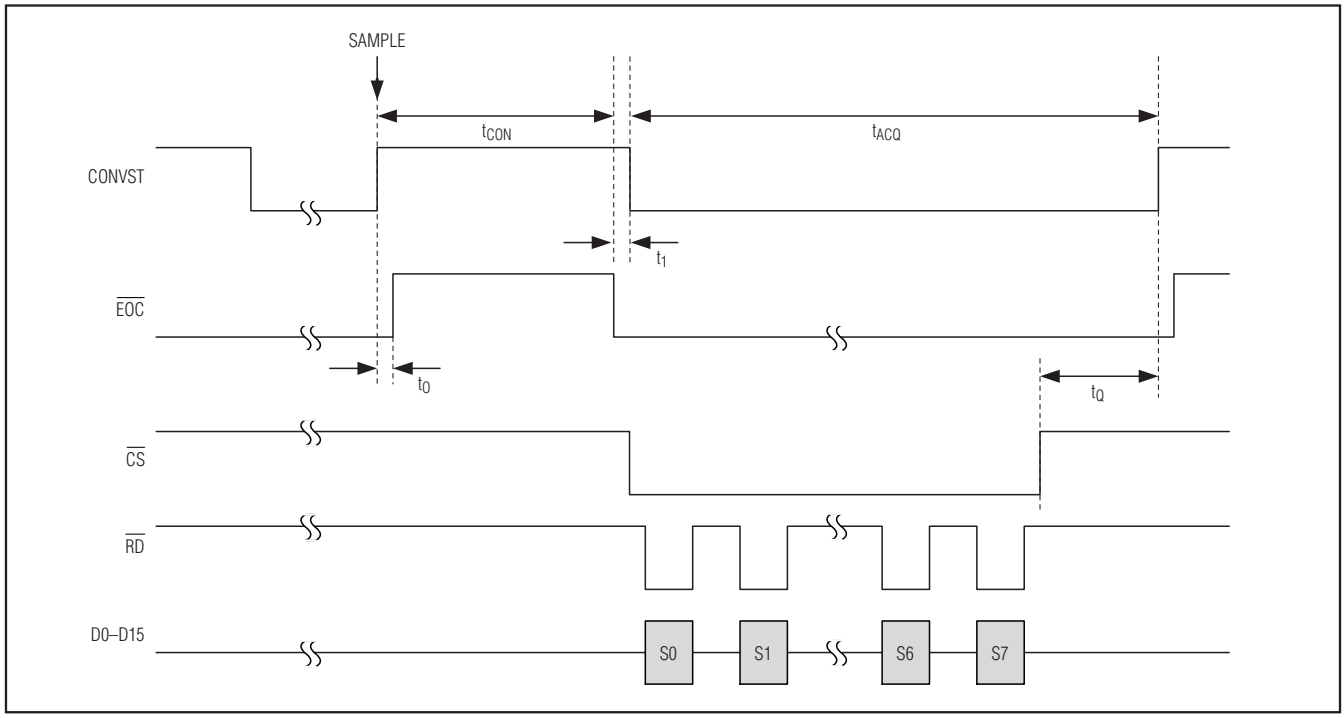


Figure 6. Conversion Timing Diagram (DB0 = 0)

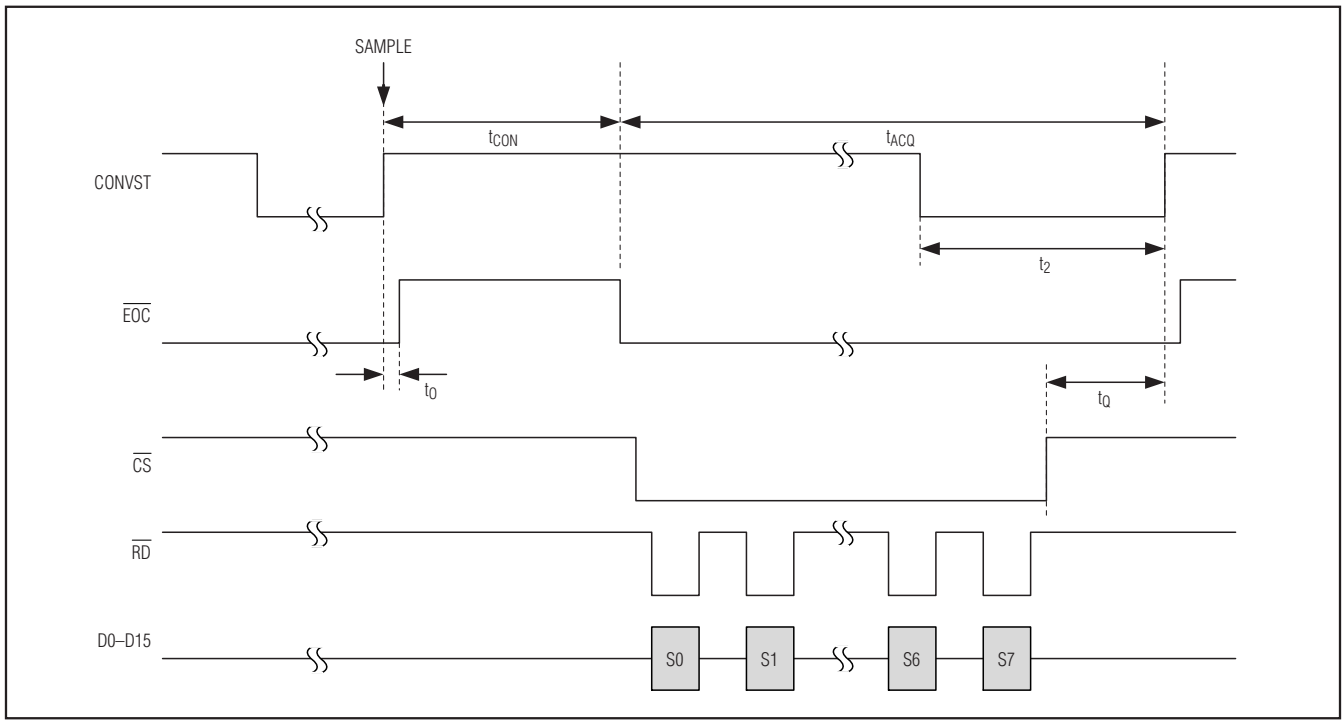


Figure 7. Conversion Timing Diagram (DB0 = 1)

Bypass AVDD and DVDD to the ground plane with 0.1µF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10µF decoupling capacitor to AVDD and DVDD per PCB. Interconnect all of the AVDD inputs and DVDD inputs using two solid power planes. For best performance, bring the AVDD power plane in on the analog interface side of the MAX11044/MAX11045/MAX11046 and the DVDD power plane from the digital interface side of the device.

For acquisition periods near minimum (1µs) use a 1nF C0G ceramic chip capacitor between each of the channel inputs to the ground plane as close as possible to the MAX11044/MAX11045/MAX11046. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.

Typical Application Circuits

Power-Grid Protection

Figure 10 shows a typical power-grid protection application.

DSP Motor Control

Figure 11 shows a typical DSP motor control application.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function. For example, -0.9 LSB guarantees no missing code while -1.1 LSB results in missing code.

Offset Error

For the MAX11044/MAX11045/MAX11046, the offset error is defined at code transition 0x8000 to 0x8001 in offset binary encoding and 0x0000 to 0x0001 for two's complement encoding. The offset code transitions should occur with an analog input voltage of exactly 0.5 x (10/4.096) x V_{REF}/65,536 above GND. The offset error is defined as the deviation between the actual analog input voltage required to produce the offset code transition and the ideal analog input of 0.5 x (10/4.096) x V_{REF}/65,536 above GND, expressed in LSBs.

Gain Error

Gain error is defined as the difference between the change in analog input voltage required to produce a top code transition minus a bottom code transition, subtracted from the ideal change in analog input voltage on (10/4.096) x V_{REF} x (65,534/65,536). For the MAX11044/MAX11045/MAX11046, top code transition is 0x7FFE to 0x7FFF in two's complement mode and 0xFFFE to 0xFFFF in offset binary mode. The bottom code transition is 0x8000 and 0x8001 in two's complement

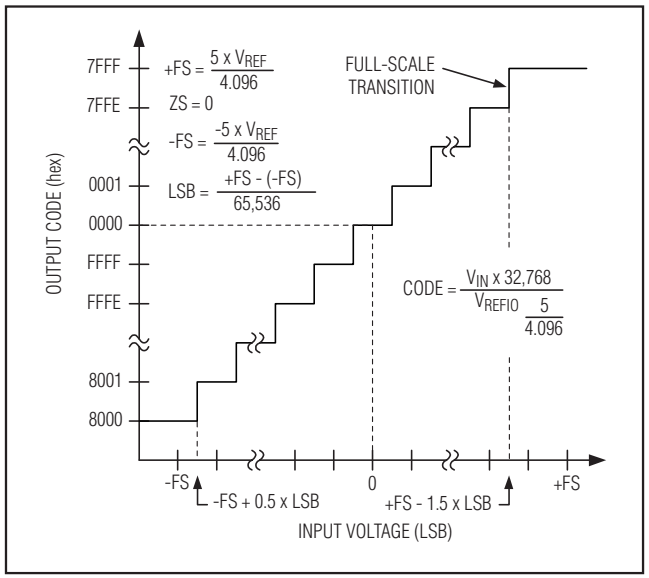


Figure 8. Two's Complement Transfer Function

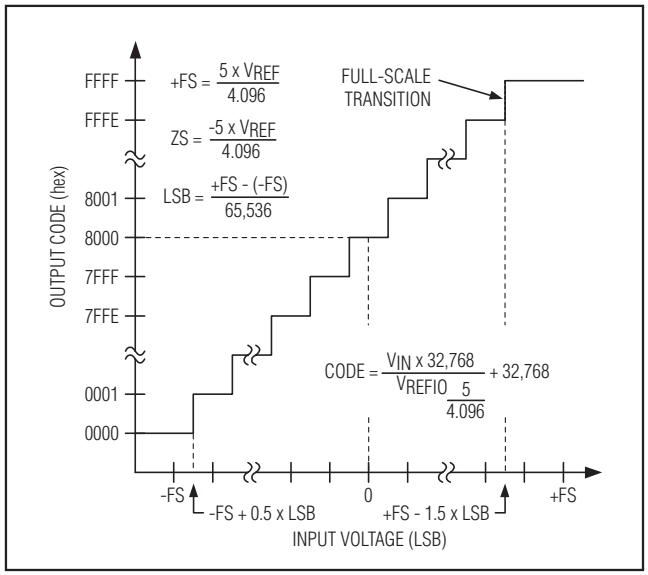


Figure 9. Offset-Binary Transfer Function

4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

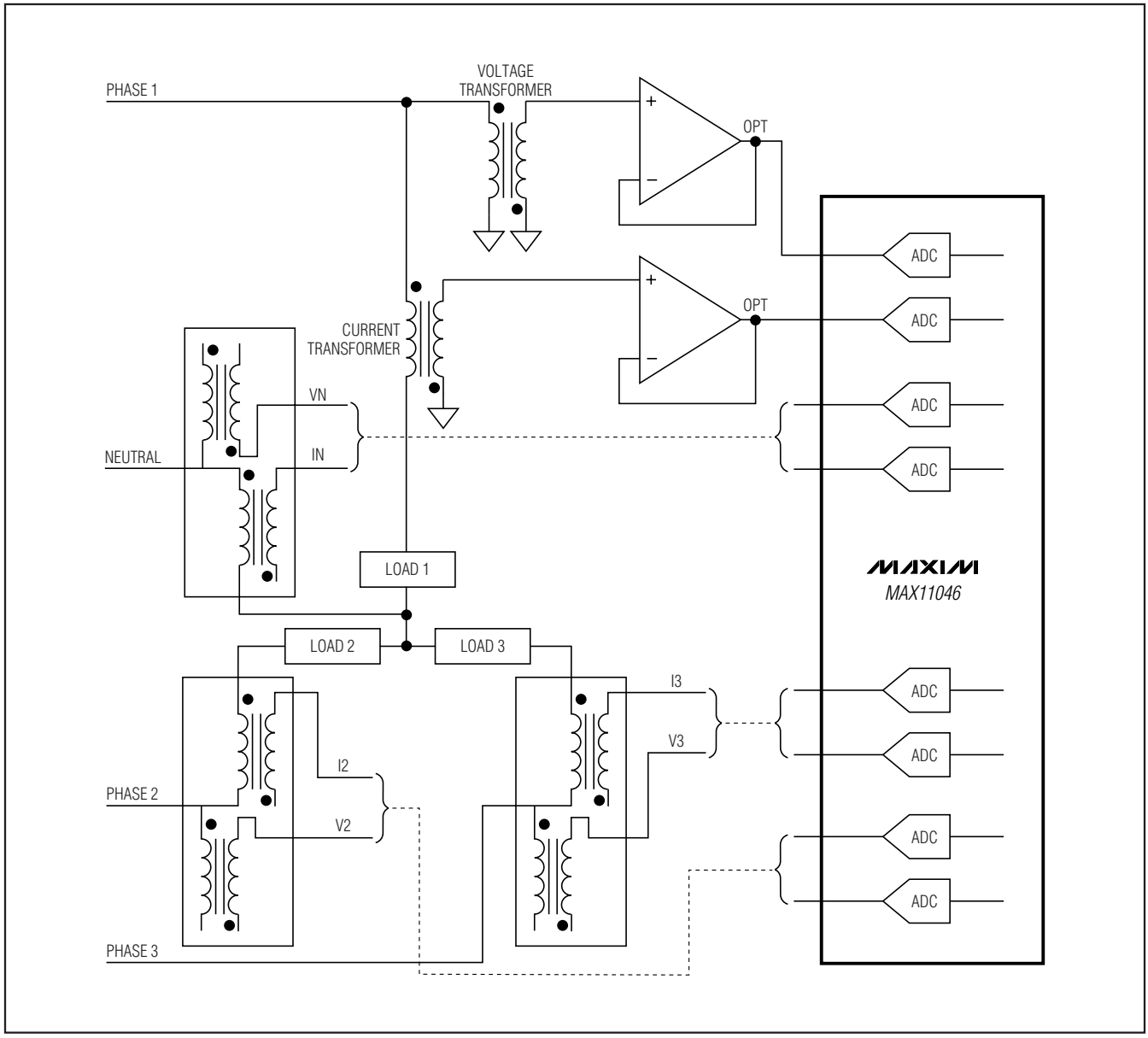


Figure 10. Power-Grid Protection

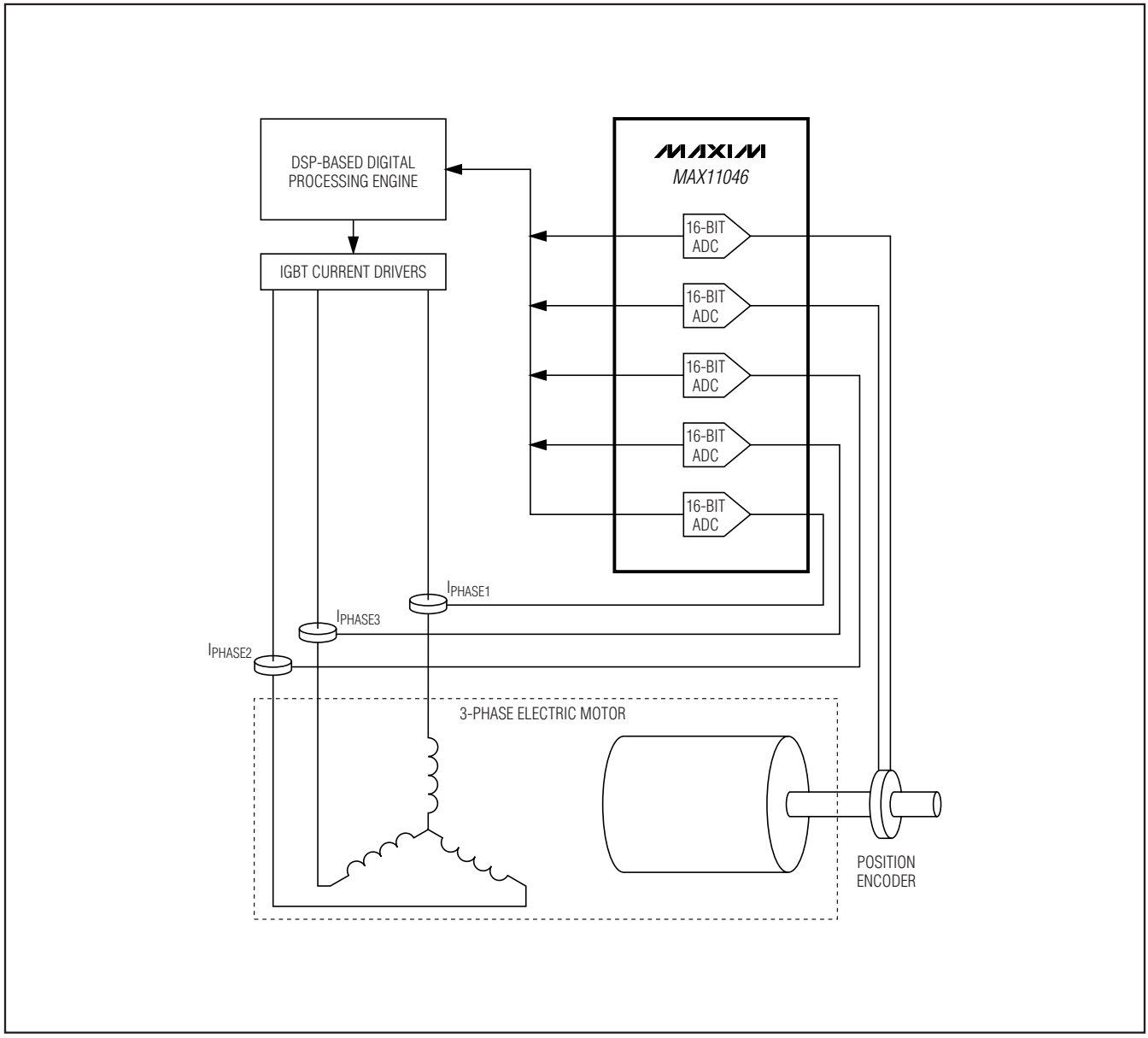


Figure 11. DSP Motor Control

mode and 0x0000 and 0x0001 in offset binary mode. For the MAX11044/MAX11045/MAX11046, the analog input voltage to produce these code transitions is measured and the gain error is computed by subtracting (10/4.096) x V_{REF} x (65,534/65,536) from this measurement.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 16 bits. In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$SINAD(dB) = 10 \times \log \left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}} \right]$$

Effective Number of Bits (ENOB)

The ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS of the first five harmonics of the input signal to the fundamental itself. This is:

$$THD = 20 \times \log \left[\frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2}}{V_1} \right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the other channels. Channel-to-channel isolation is measured by applying DC to channels 1 to 7, while a -0.4dBFS sine wave at 60Hz is applied to channel 0. A 10ksps FFT is taken for channel 0 and channel 1. Channel-to-channel isolation is expressed in dB as the power ratio of the two 60Hz magnitudes.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Positive Full-Scale Error

The error in the input voltage that causes the last code transition of FFFE to FFFF (hex) (in default offset binary mode) or 7FFE to 7FFF (hex) (in two's complement mode) from the ideal input voltage of 32,766.5 x (5/4.096) x (V_{REFIO}/65,536) after correction for offset error.

Negative Full-Scale Error

The error in the input voltage that causes the first code transition of 0000 to 0001 (hex) (in default offset binary mode) or 8000 to 8001 (hex) (in two's complement mode) from the ideal input voltage of -32,767.5 x (5/4.096) x (V_{REFIO}/65,536) after correction for offset error.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5688+2	**21-0135**

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