ADS1115-Q1 Low-Power, 16-Bit Analog-to-Digital Converter With Internal Reference

1 Features

- Wide Supply Range: 2 V to 5.5 V
- Low-Current Consumption:
  Continuous Mode: Only 150 µA
  Single-Shot Mode: Auto Shut-Down
- Programmable Data Rate:
  8 SPS to 860 SPS
- Internal Low-Drift Voltage Reference
- Internal Oscillator
- Internal PGA
- I^2C Interface: Pin-Selectable Addresses
- Four Single-Ended or Two Differential Inputs
- Programmable Comparator

2 Applications

- Automotive Head Units
- Heads-Up Display (HUD)
- Automotive Battery Management Systems
- Automotive On-Board Chargers
- NOx Sensors
- Soot and Particulate Matter (PM) Sensors
- Oxygen (O2, Lambda, A/F) Sensors
- Ammonia (NH3) Sensors
- Other Emissions and Gas Sensors
- Temperature Measurement
- Voltage Monitoring

3 Description

The ADS1115-Q1 device is a precision analog-to-digital converter (ADC) with 16 bits of resolution offered in a 10-pin VSSOP package. The design of the ADS1115-Q1 device considers precision, power, and ease of implementation. The ADS1115-Q1 device features an onboard reference and oscillator. Data are transferred through an I^2C-compatible serial interface. Four I^2C slave addresses can be selected. The ADS1115-Q1 device operates from a single power supply ranging from 2 V to 5.5 V.

The ADS1115-Q1 device can perform conversions at rates up to 860 samples per second (SPS). An onboard PGA is available on the ADS1115-Q1 device that offers input ranges from the supply to as low as ±256 mV, allowing both large and small signals to be measured with high resolution. The ADS1115-Q1 device also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

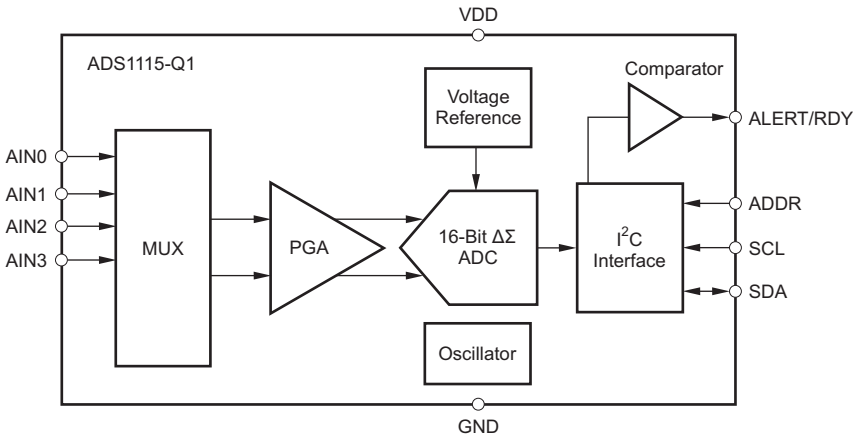
The ADS1115-Q1 device operates either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1115-Q1 device is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1115-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADS1115-Q1 Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2015) to Revision B — **Page**

- Deleted references to the QFN package ... 1
- Restructured the I^2C and some register content into the new *Programming* section ... 17
- Deleted the DAC8574 and TMP421 devices from the *Connecting Multiple Devices* section ... 27
- Changed the *ADC Code vs Voltage Across Current-Shunt Resistor* curve in the *Application Curve* section ... 31

Changes from Original (December 2011) to Revision A — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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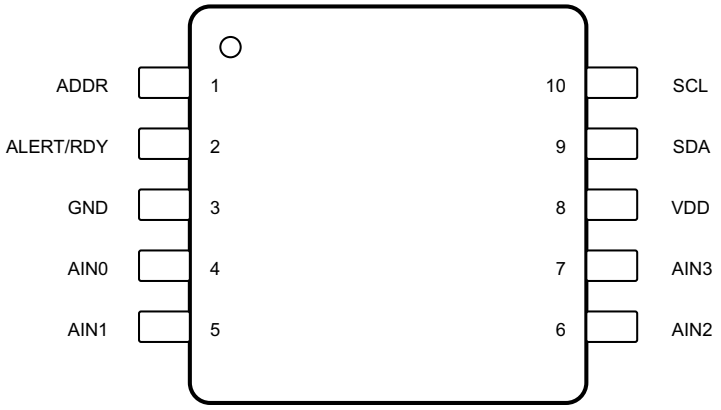
5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	ADDR	Digital Input	I^2C slave address select
2	ALERT/RDY	Digital Output	Digital comparator output or conversion ready
3	GND	Analog	Ground
4	AIN0	Analog Input	Differential channel 1: Positive input or single-ended channel 1 input
5	AIN1	Analog Input	Differential channel 1: Negative input or single-ended channel 2 input
6	AIN2	Analog Input	Differential channel 2: Positive input or single-ended channel 3 input
7	AIN3	Analog Input	Differential channel 2: Negative input or single-ended channel 4 input
8	VDD	Analog	Power supply: 2 V to 5.5 V
9	SDA	Digital I/O	Serial data: Transmits and receives data
10	SCL	Digital Input	Serial clock input: Clocks data on SDA

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD to GND	–0.3	5.5	V
Analog input current, momentary		100	mA
Analog input current, continuous		10	mA
Analog input voltage to GND	–0.3	VDD + 0.3	V
SDA, SCL, ADDR, ALERT/RDY voltage to GND	–0.5	5.5	V
Maximum junction temperature		150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)	±750	
			All other pins	±500	
		Machine Model (MM), per AEC-Q100-003		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Power-supply voltage		2		5.5	V
Supply Current	Power-down current at 25ºC		0.5	2	µA
	Power-down current up to 125ºC			5	
	Operating current at 25ºC		150	200	
	Operating current up to 125ºC			300	
Power Dissipation	VDD = 5 V		0.9		mW
	VDD = 3.3 V		0.5		
	VDD = 2 V		0.3		
Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Full-scale input voltage[1]	$V_{IN} = (AIN_P) – (AIN_N)$		±4.096/PGA		V
Specified ambient temperature		–40		125	°C

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

6.4 Thermal Information

THERMAL METRIC[1]		ADS1115-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.44	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.25	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.97	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.78	°C/W
ψ_{JB}	Junction-to-board characterization parameter	107.11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

All specifications at –40°C to +125°C, VDD = 3.3 V, and Full-Scale (FS) = ±2.048 V, unless otherwise noted. Typical values are at 25°C, $T_A = T_J$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Differential input impedance		See Table 1			
	Common-mode input impedance	FS = ±6.144 V(1)		10		MΩ
		FS = ±4.096 V(1), ±2.048 V		6		MΩ
		FS = ±1.024 V		3		MΩ
		FS = ±0.512 V, ±0.256 V		100		MΩ
SYSTEM PERFORMANCE						
	Resolution	No missing codes	16			Bits
	Data rate (DR)			8, 16, 32, 64, 128, 250, 475, 860		SPS
	Data rate variation	All data rates	–10%		10%	
	Output noise		See *Typical Characteristics*			
	Integral nonlinearity	DR = 8 SPS, FS = ±2.048 V, best fit(2)			1	LSB
	Offset error	FS = ±2.048 V, differential inputs		±1	±3	LSB
		FS = ±2.048 V, single-ended inputs		±3		LSB
	Offset drift	FS = ±2.048 V		0.005		LSB/°C
	Offset power-supply rejection	FS = ±2.048 V		1		LSB/V
	Gain error(3)	FS = ±2.048 V at 25°C		0.01%	0.15%	
	Gain drift(3)	FS = ±0.256 V		7		ppm/°C
		FS = ±2.048 V		5	40	ppm/°C
		FS = ±6.144 V(1)		5		ppm/°C
	Gain power-supply rejection			80		ppm/V
	PGA gain match(3)	Match between any two PGA gains		0.02%	0.1%	
	Gain match	Match between any two inputs		0.05%	0.1%	
	Offset match	Match between any two inputs		3		LSB
	Common-mode rejection	At dc and FS = ±0.256 V		105		dB
		At dc and FS = ±2.048 V		100		dB
		At dc and FS = ±6.144 V(1)		90		dB
		f_{CM} = 60 Hz, DR = 8 SPS		105		dB
		f_{CM} = 50 Hz, DR = 8 SPS		105		dB
DIGITAL INPUT/OUTPUT						
V_{IH}	High logic-level input voltage		0.7 VDD		5.5	V
V_{IL}	Low logic-level input voltage		GND – 0.5		0.3 VDD	V
V_{OL}	Low logic-level output voltage	I_{OL} = 3 mA	GND	0.15	0.4	V
I_H	Input leakage, high	V_{IH} = 5.5 V			10	µA
I_L	Input leakage, low	V_{IL} = GND	10			µA

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.
(2) 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.

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6.6 Timing Requirements

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	0.01	0.4	0.01	3.4	MHz
t_{BUF}	Bus free time between START and STOP condition	600		160		ns
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
t_{SUSTA}	Repeated START condition setup time	600		160		ns
t_{SUSTO}	Stop condition setup time	600		160		ns
t_{HDDAT}	Data hold time	0		0		ns
t_{SUDAT}	Data setup time	100		10		ns
t_{LOW}	SCL clock low period	1300		160		ns
t_{HIGH}	SCL clock high period	600		60		ns
t_F	Clock/data fall time		300		160	ns
t_R	Clock/data rise time		300		160	ns

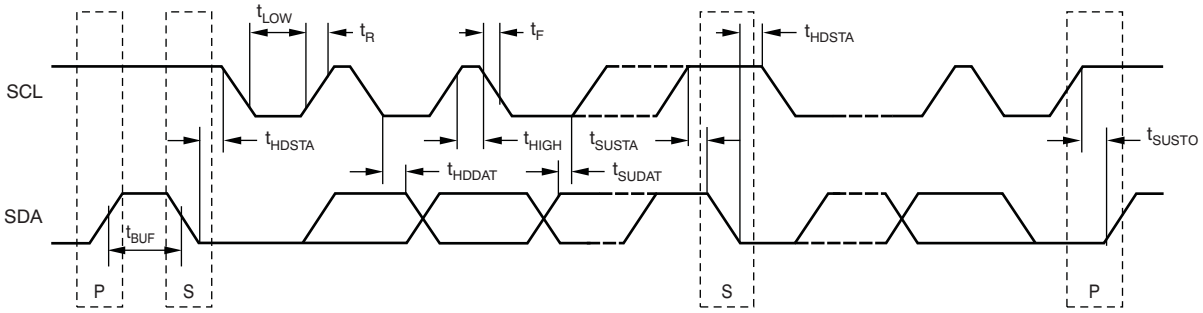

Figure 1. I²C Timing Diagram

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6.7 Typical Characteristics

At T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

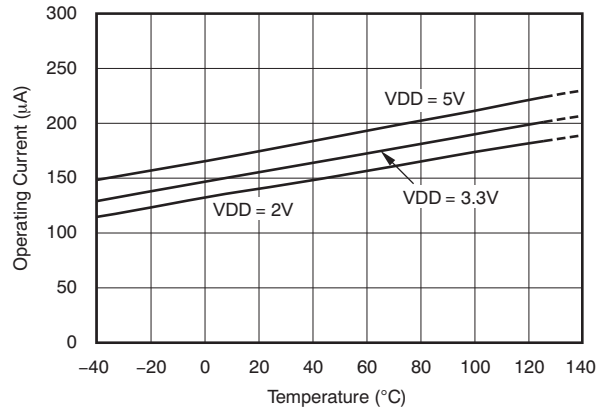

Figure 2. Operating Current vs Temperature

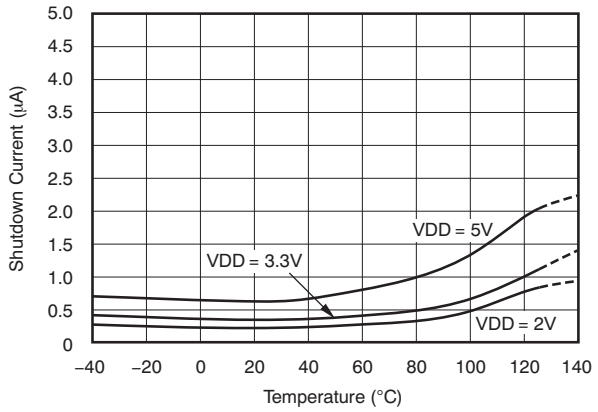

Figure 3. Shutdown Current vs Temperature

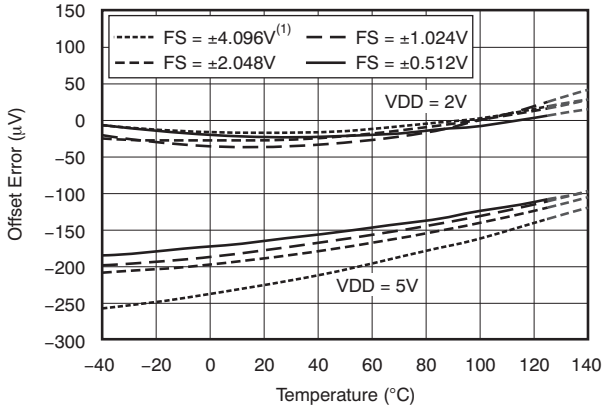

Figure 4. Single-Ended Offset Error vs Temperature

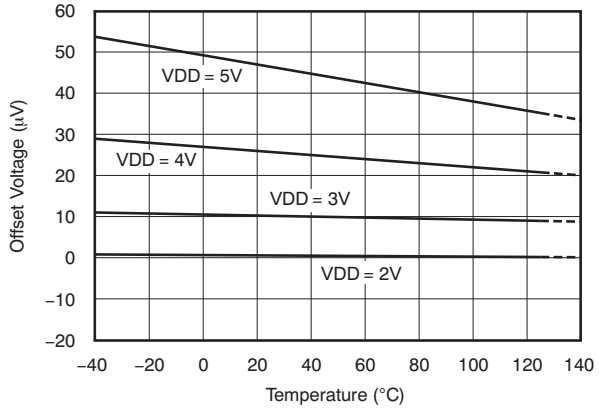

Figure 5. Differential Offset vs Temperature

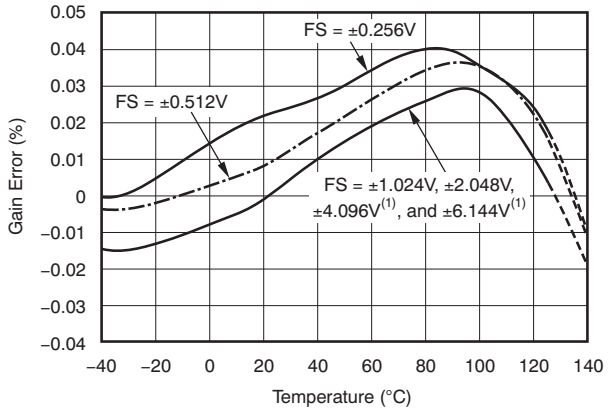

Figure 6. Gain Error vs Temperature

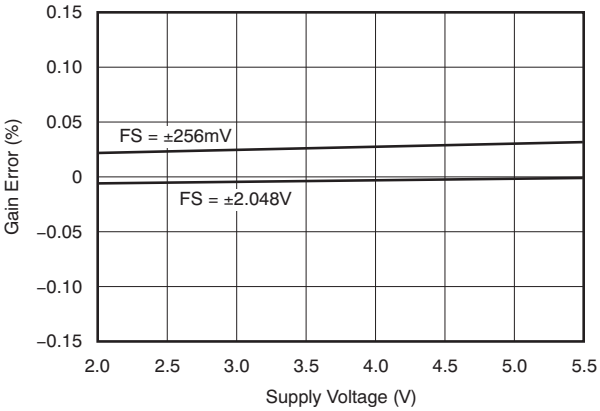

Figure 7. Gain Error vs Supply (1)

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

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Typical Characteristics (continued)

At T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

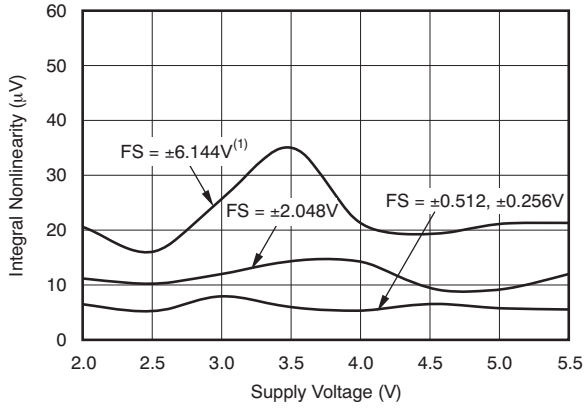

Figure 8. INL vs Supply Voltage (2)

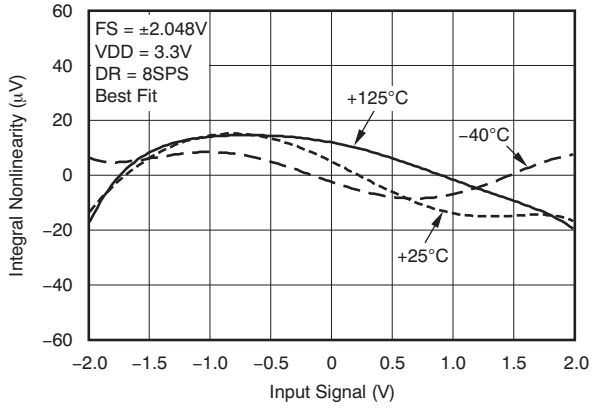

Figure 9. INL vs Input Signal

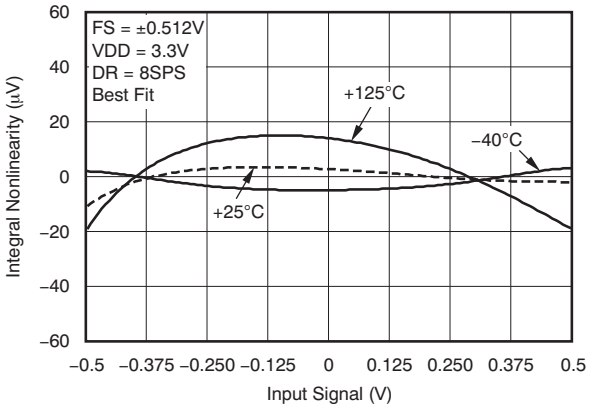

Figure 10. INL vs Input Signal

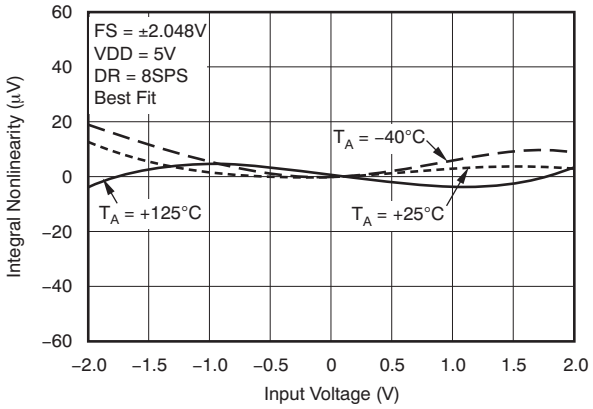

Figure 11. INL vs Input Signal

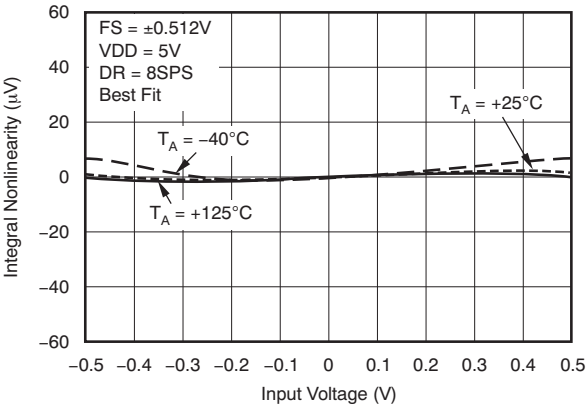

Figure 12. INL vs Input Signal

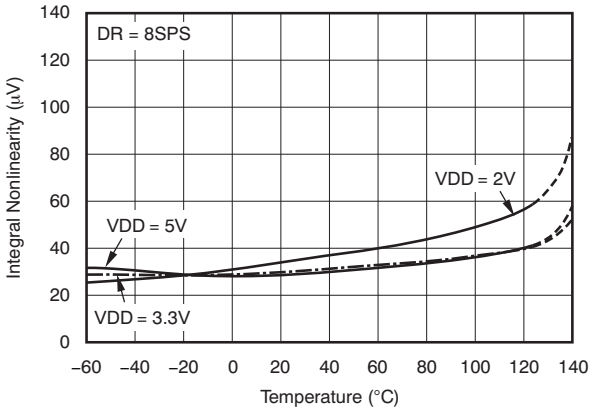

Figure 13. INL vs Temperature

(2) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

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Typical Characteristics (continued)

At T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

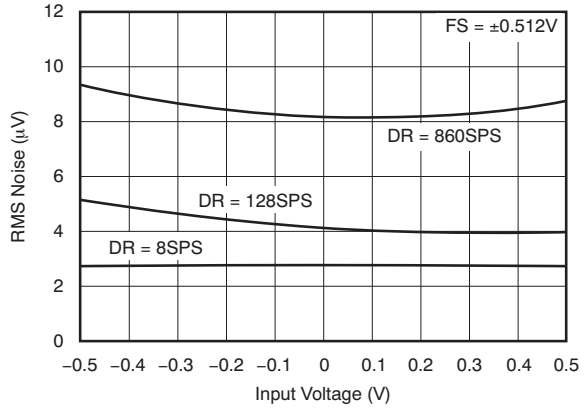

Figure 14. Noise vs Input Signal

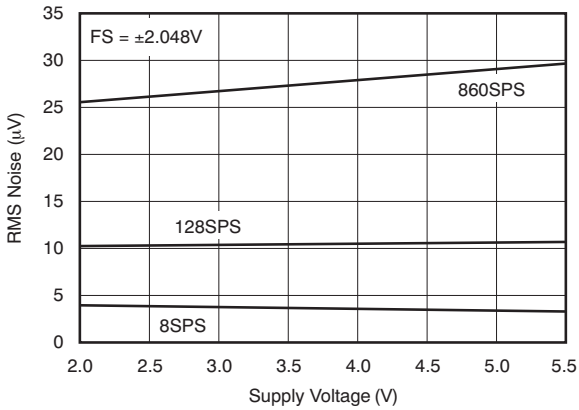

Figure 15. Noise vs Supply Voltage

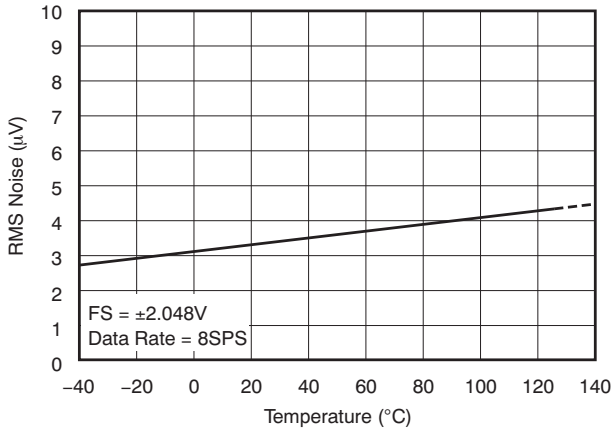

Figure 16. Noise vs Temperature

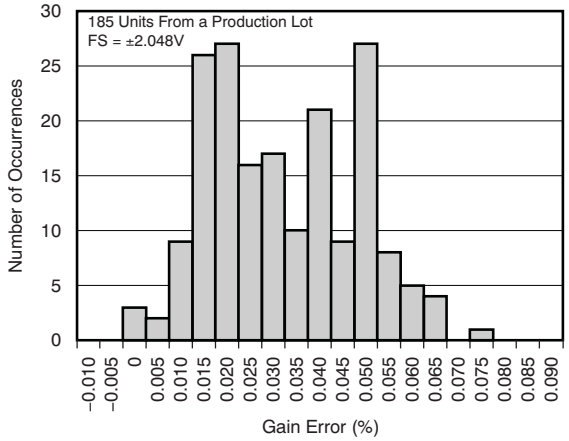

Figure 17. Gain Error Histogram

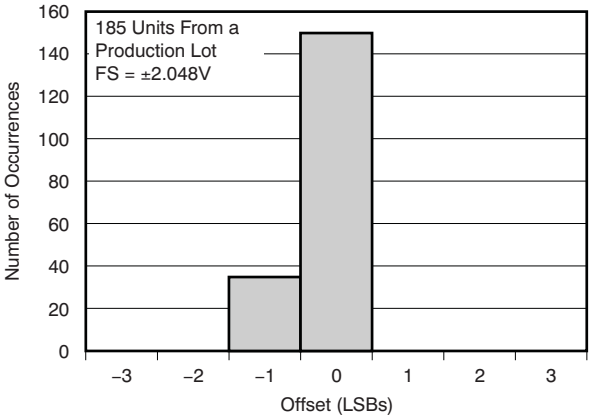

Figure 18. Offset Histogram

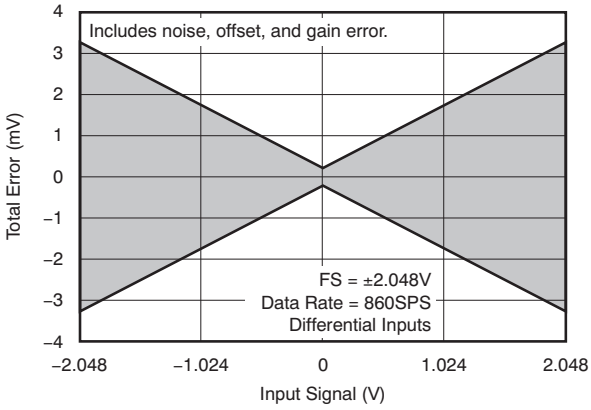

Figure 19. Total Error vs Input Signal

Typical Characteristics (continued)

At T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

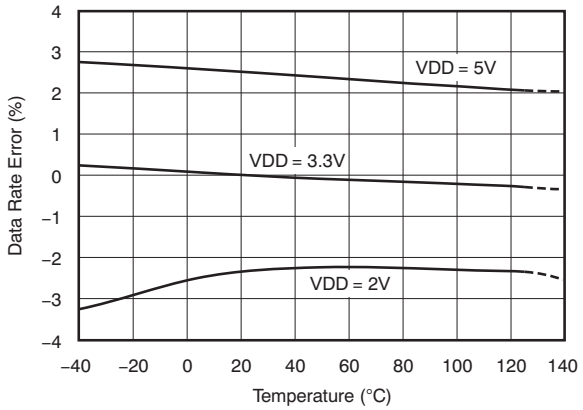

Figure 20. Data Rate vs Temperature

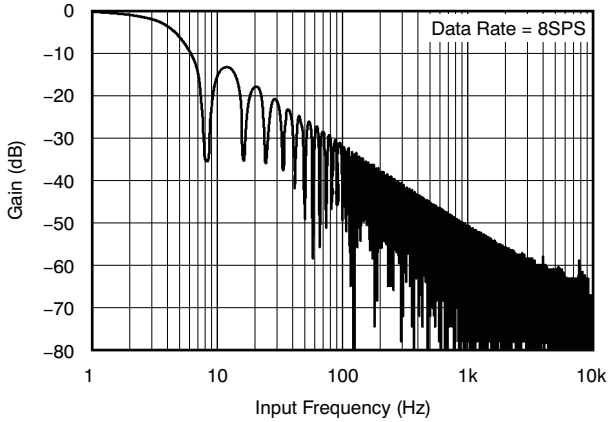

Figure 21. Frequency Response

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7 Detailed Description

7.1 Overview

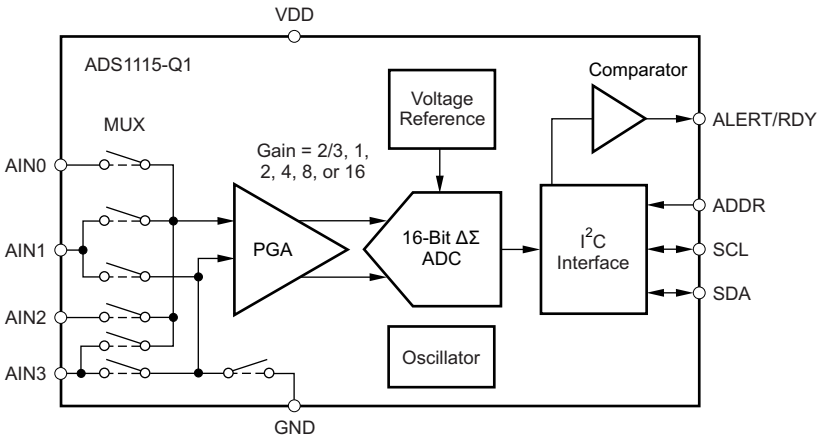
The ADS1115-Q1 device is a small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1115-Q1 device is easy to configure and design into a wide variety of applications, and allows precise measurements to be obtained with very little effort.

The ADS1115-Q1 device consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an I^2C interface. An additional feature available on the ADS1115-Q1 device is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance.

The ADS1115-Q1 ADC core measures a differential signal, V_{IN}, that is the difference between AIN_P and AIN_N. A MUX is available on the ADS1115-Q1 device to route the four input channels to AIN_P and AIN_N. This architecture results in a strong attenuation in any common-mode signals. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1115-Q1 device has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiplexer

The ADS1115-Q1 device contains an input multiplexer, as shown in Figure 22. Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 can be measured differentially to AIN3. The multiplexer is configured by three bits in the Config register (see the *Config Register* section). When the single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

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Feature Description (continued)

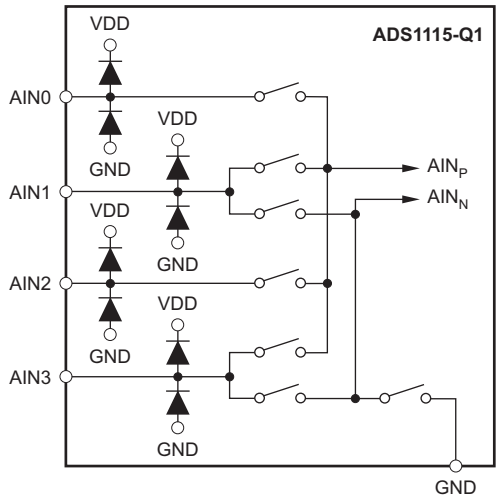

Figure 22. ADS1115-Q1 MUX

When measuring single-ended inputs, the negative range of the output codes are not used. These codes are for measuring negative differential signals such as (AIN_P – AIN_N) < 0. ESD diodes to the VDD and GND pins protect the inputs on this device. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range shown in Equation 1.

$$GND - 0.3\ V < AINx < VDD + 0.3\ V \quad (1)$$

If the voltages on the input pins may violate these conditions, external Schottky clamp diodes, series resistors, or both may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1115-Q1 device can affect conversions taking place on other input pins. If overdrive on unused inputs is possible, again TI recommends to clamp the signal with external Schottky diodes.

7.3.2 Analog Inputs

The ADS1115-Q1 device uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The capacitors used are small, and to external circuitry the average loading appears resistive. This structure is shown in Figure 24. The resistance is set by the capacitor values and the rate at which they are switched. Figure 23 shows the on and off setting of the switches illustrated in Figure 24. During the sampling phase, S_1 switches are closed. This event charges C_{A1} to AIN_P, C_{A2} to AIN_N, and C_B to (AIN_P – AIN_N). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1115-Q1 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}) where $R_{eff} = V_{IN}/I_{AVERAGE}$.

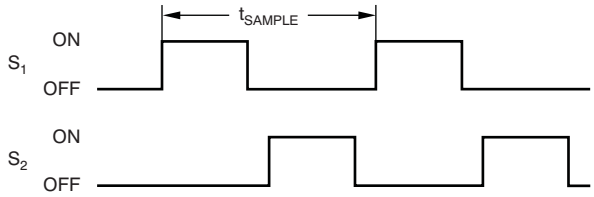

Figure 23. S_1 and S_2 Switch Timing for Figure 24

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Feature Description (continued)

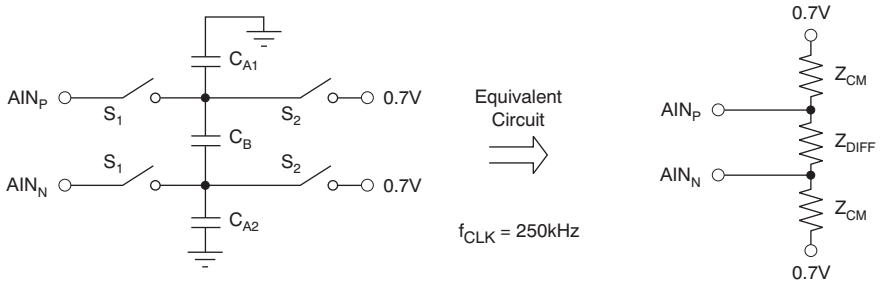

Figure 24. Simplified Analog Input Circuit

The common-mode input impedance is measured by applying a common-mode signal to shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6 MΩ for the default PGA gain setting. In Figure 24, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the PGA gain setting. In Figure 24, the differential input impedance is Z_{DIFF}. Table 1 describes the typical differential input impedance.

Table 1. Differential Input Impedance

FS	DIFFERENTIAL INPUT IMPEDANCE
±6.144 V(1)	22 MΩ
±4.096 V(1)	15 MΩ
±2.048 V	4.9 MΩ
±1.024 V	2.4 MΩ
±0.512 V	710 kΩ
±0.256 V	710 kΩ

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1115-Q1 input impedance can affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 1 for typical input impedance are valid.

7.3.3 Full-Scale Input

A programmable gain amplifier (PGA) is implemented before the ΔΣ core of the ADS1115-Q1 device. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 2 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4 V. In this case (as well as for PGA = 1 and VDD < 4 V), reaching a full-scale output code on the ADC is not possible. Analog input voltages may never exceed the analog input voltage limits given in the *Electrical Characteristics* table.

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Table 2. PGA Gain Full-Scale Range

PGA SETTING	FS (V)
2/3	±6.144(1)
1	±4.096(1)
2	±2.048
4	±1.024
8	±0.512
16	±0.256

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

7.3.4 Data Format

The ADS1115-Q1 device provides 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 25 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ FS $(2^{15} – 1) / 2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0
$–FS/2^{15}$	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

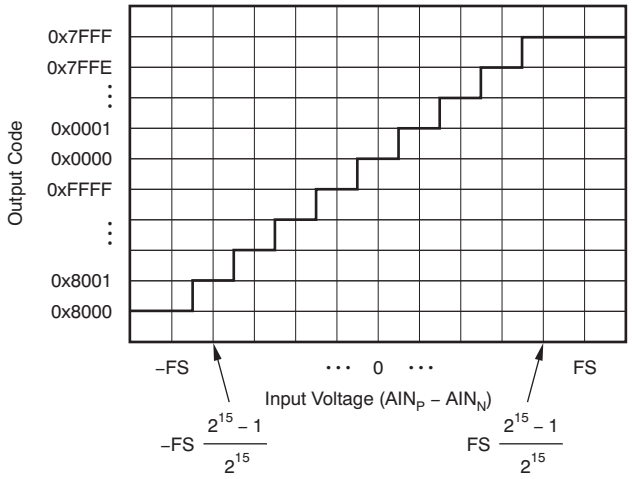

Figure 25. ADS1115-Q1 Code Transition Diagram

7.3.5 Aliasing

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1115-Q1 digital filter provides some attenuation of high-frequency noise, but the digital Sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

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When designing an input filter circuit, consider the interaction between the filter network and the input impedance of the ADS1115-Q1 device.

7.3.6 Reset and Power-up

When the ADS1115-Q1 device powers up, a reset occurs. As part of the reset process, the ADS1115-Q1 device sets all of the bits in the Config register to the respective default settings.

The ADS1115-Q1 device responds to the I^2C general call reset command. When the ADS1115-Q1 device receives a general call reset, an internal reset occurs as if the device had been powered on.

7.3.7 Duty Cycling for Low Power

For many applications, the improved performance at low data rates may not be required. For these applications, the ADS1115-Q1 device supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate. For example, an ADS1115-Q1 device in power-down mode with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires about 1.2 ms, the ADS1115-Q1 device enters power-down mode for the remaining 123.8 ms. In this configuration, the ADS1115-Q1 device consumes about 1/100th the power of the ADS1115-Q1 device operating in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The ADS1115-Q1 device offers lower data rates that do not implement duty cycling and offer improved noise performance if necessary.

7.3.8 Comparator

The ADS1115-Q1 device is equipped with a customizable comparator that can issue an alert on the ALERT/RDY pin. This feature can significantly reduce external circuitry for many applications. The comparator can be implemented as either a traditional comparator or a window comparator via the COMP_MODE bit in the Config register. When implemented as a traditional comparator, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the high threshold register. The comparator then deasserts when the input signal falls below the low threshold register value. In window comparator mode, the ALERT/RDY pin asserts if conversion data exceed the high threshold register or fall below the low threshold register.

In either window or traditional comparator mode, the comparator can be configured to latch when asserted by the COMP_LAT bit in the Config register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can be cleared by issuing an SMBus alert response or by reading the Conversion register (see the *Conversion Register* section). The COMP_POL bit in the Config register configures the ALERT/RDY pin as active high or active low. Operational diagrams for the comparator modes are shown in Figure 26 and Figure 27.

The comparator can be configured to activate the ALERT/RDY pin after a set number of successive readings exceed the threshold. The comparator can be configured to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin by changing the COMP_QUE bits in the Config register. The COMP_QUE bits can also disable the comparator function.

7.3.9 Conversion-Ready Pin

The ALERT/RDY pin can also be configured as a conversion-ready pin. This mode of operation can be realized if the MSB of the high threshold register is set to 1 and the MSB of the low threshold register is set to 0. The COMP_POL bit continues to function and the COMP_QUE bits can disable the pin; however, the COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion-ready pin, ALERT/RDY continues to require a pullup resistor. When in continuous conversion mode, the ADS1115-Q1 device provides a brief (approximately 8 µs) pulse on the ALERT/RDY pin at the end of each conversion. When in single-shot shutdown mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to 0.

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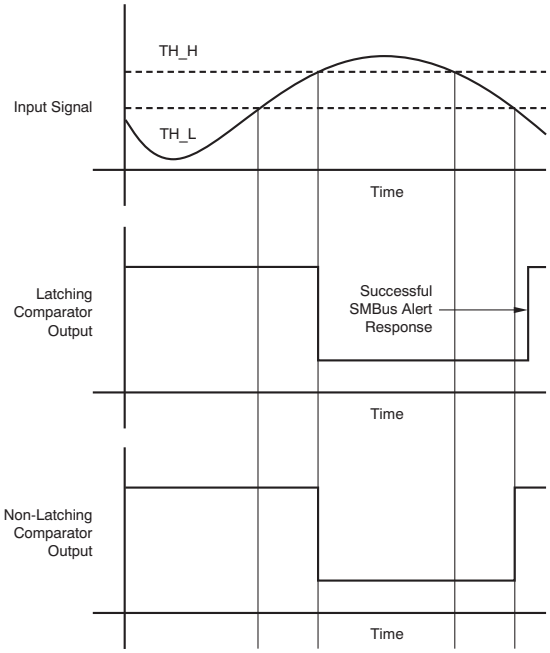

Figure 26. Alert Pin Timing Diagram When Configured as a Traditional Comparator

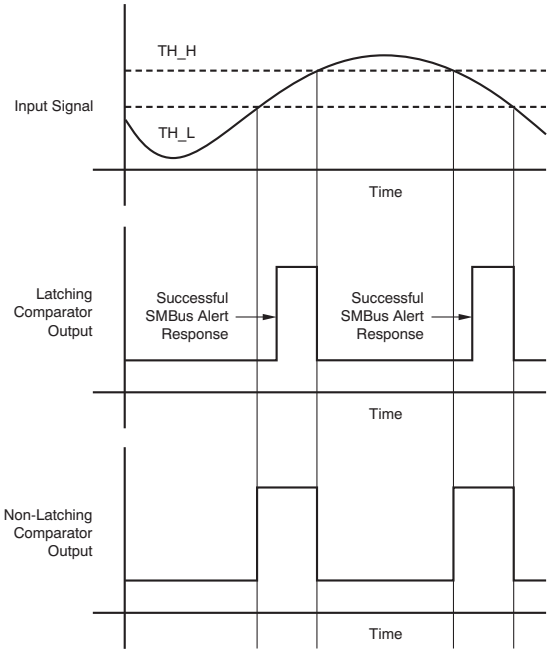

Figure 27. Alert Pin Timing Diagram When Configured as a Window Comparator

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7.3.10 SMBus Alert Response

When configured in latching mode (COMP_LAT = 1 in the Config register), the ALERT/RDY pin can be implemented with an SMBus alert. The pin asserts if the comparator detects a conversion that exceeds an upper or lower threshold. This interrupt is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I^2C address. If conversion data exceed the upper or lower thresholds after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin, as with the SDA pin, is an open-drain pin. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that it does not interfere with other devices on the same bus line.

When the master senses that the ALERT/RDY pin has latched, it issues an SMBus alert command (00011001) to the I^2C bus. Any ADS1115-Q1 data converters on the I^2C bus with the ALERT/RDY pins asserted respond to the command with the slave address. In the event that two or more ADS1115-Q1 data converters present on the bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert decides which device clears its assertion. The device with the lowest I^2C address always wins arbitration. If a device loses arbitration, it does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have had the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a 1 if signals exceed the high threshold and a 0 if signals exceed the low threshold.

7.4 Device Functional Modes

The ADS1115-Q1 device operates in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1115-Q1 device continuously perform conversions. When a conversion is complete, the ADS1115-Q1 device places the result in the Conversion register and immediately begins another conversion. In single-shot mode, the ADS1115-Q1 device waits until the OS bit is set high. When asserted, the bit is set to 0, indicating that a conversion is currently in progress. When the conversion data are ready, the OS bit reasserts and the device powers down. Writing a 1 to the OS bit during a conversion has no effect.

7.5 Programming

7.5.1 I^2C Interface

The ADS1115-Q1 device communicates through an I^2C interface. I^2C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1115-Q1 device can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. The SDA lines carries data and the SCL line provides the clock. All data are transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while the SCL line is low (a low on the SDA line indicates the bit is zero; a high indicates the bit is one). When the SDA line settles, the SCL line is brought high, then low. This pulse on the SCL line clocks the SDA bit into the receiver shift register. If the I^2C bus is held idle for more than 25 ms, the bus times out.

The I^2C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1115-Q1 device never drives the SCL line because it cannot act as a master. On the ADS1115-Q1 device, the SCL line is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication occurs, the bus is active. Only master devices can begin communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

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Programming (continued)

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the *address byte*. Each device on an I^2C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an *acknowledge* bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling the SDA line low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls the SDA line low to acknowledge this to the slave. It then sends a clock pulse to clock the bit (the master always drives the clock line).

A *not-acknowledge* is performed by simply leaving the SDA line high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it can issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master can also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

See the *Timing Requirements* section for a timing diagram showing the ADS1115-Q1 I^2C transaction.

7.5.1.1 I^2C Address Selection

The ADS1115-Q1 device has one address pin, ADDR, that sets the I^2C address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 4. The state of the address pin ADDR is sampled continuously.

Table 4. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN	SLAVE ADDRESS
Ground	1001000
VDD	1001001
SDA	1001010
SCL	1001011

7.5.1.2 I^2C General Call

The ADS1115-Q1 device responds to the I^2C general call address (0000000) if the eighth bit is 0. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the ADS1115-Q1 device resets the internal registers and enters power-down mode.

7.5.1.3 I^2C Speed Modes

The I^2C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100 kHz; fast mode allows a clock frequency of up to 400 kHz; and high-speed mode (also called HS mode) allows a clock frequency of up to 3.4 MHz. The ADS1115-Q1 device is fully compatible with all three modes.

No special action is required to use the ADS1115-Q1 device in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of *00001xxx* following the START condition, where *xxx* are bits unique to the HS-capable master. This byte is called the HS master code.

NOTE

This byte is different from normal address bytes; the eighth bit does not indicate read-write status.

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The ADS1115-Q1 device does not acknowledge this byte; the I^2C specification prohibits acknowledgment of the HS master code. Upon receiving a master code, the ADS1115-Q1 device switches on HS mode filters, and communicates at up to 3.4 MHz. The ADS1115-Q1 device switches out of HS mode with the next STOP condition.

For more information on high-speed mode, refer to the I^2C specification.

7.5.2 Slave Mode Operations

The ADS1115-Q1 device can act as either a slave receiver or slave transmitter. As a slave device, the ADS1115-Q1 device cannot drive the SCL line.

7.5.2.1 Receive Mode

In slave receive mode the first byte transmitted from the master to the slave is the address with the R/$\overline{W}$ bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the register pointer byte. The ADS1115-Q1 device then acknowledges receipt of the register pointer byte. The next two bytes are written to the address given by the register pointer. The ADS1115-Q1 device acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.5.2.2 Transmit Mode

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/$\overline{W}$ bit. This byte places the slave into transmit mode and indicates that the ADS1115-Q1 device is being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register pointer. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master can terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

7.5.3 Writing and Reading the Registers

To access a specific register from the ADS1115-Q1 device, the master must first write an appropriate value to the Pointer register (see the *Pointer Register* section). The Pointer register is written directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. After the Pointer register is written, the slave acknowledges and the master issues a STOP or a repeated START condition.

When reading from the ADS1115-Q1 device, the previous value written to the Pointer register determines the register that is read from. To change which register is read, a new value must be written to the Pointer register. To write a new value to the Pointer register, the master issues a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data need to be transmitted, and a STOP condition can be issued by the master. The master can now issue a START condition and send the slave address byte with the R/$\overline{W}$ bit high to begin the read. Figure 28 details this sequence. If repeated reads from the same register are desired, there is no need to continually send Pointer register bytes, because the ADS1115-Q1 device stores the value of the Pointer register until it is modified by a write operation. However, every write operation requires the Pointer register to be written.

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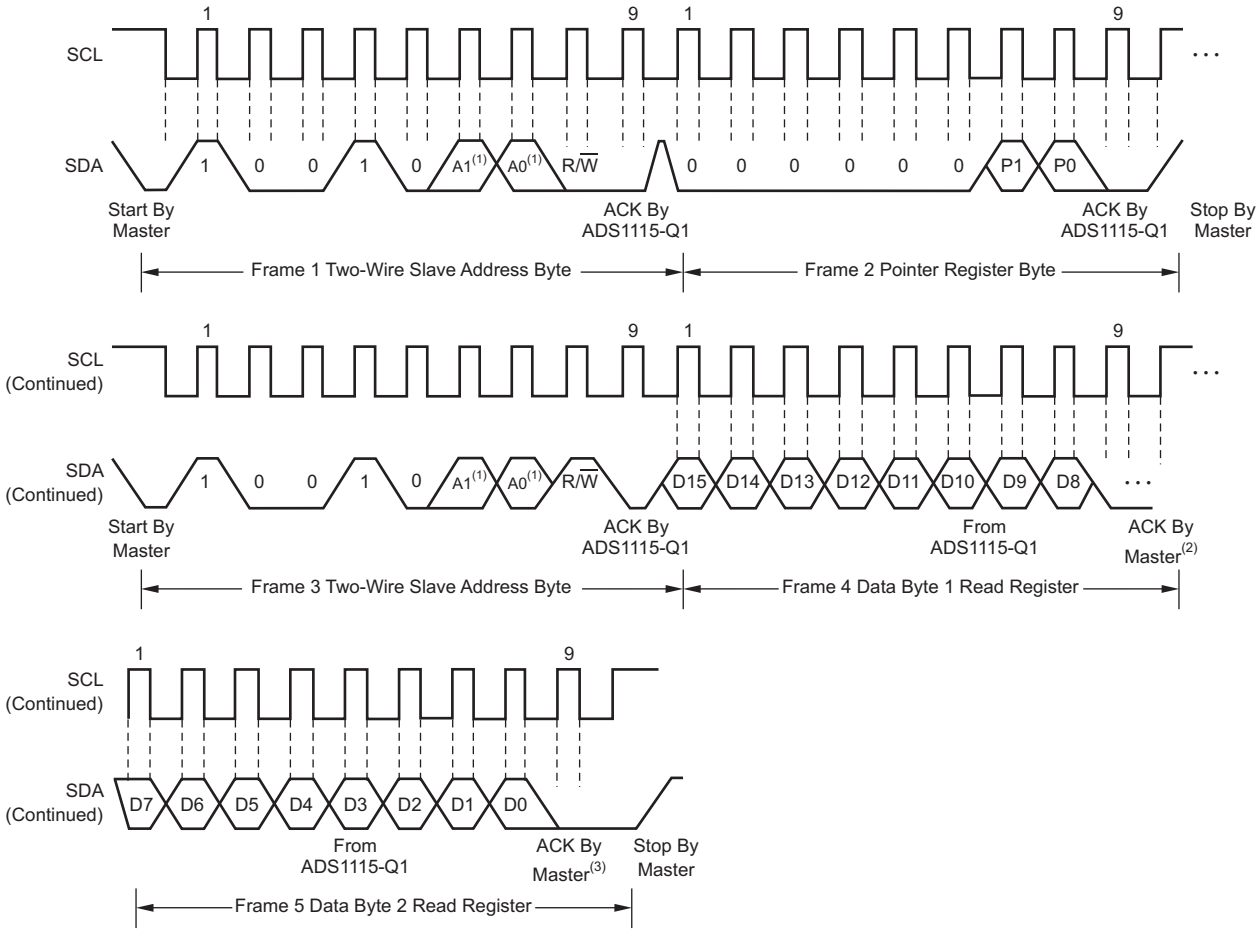

(1) The values of A0 and A1 are determined by the ADDR pin.

(2) The master can leave SDA high to terminate a single-byte read operation.

(3) The master can leave SDA high to terminate a two-byte read operation.

Figure 28. Two-Wire Timing Diagram for Read Word Format

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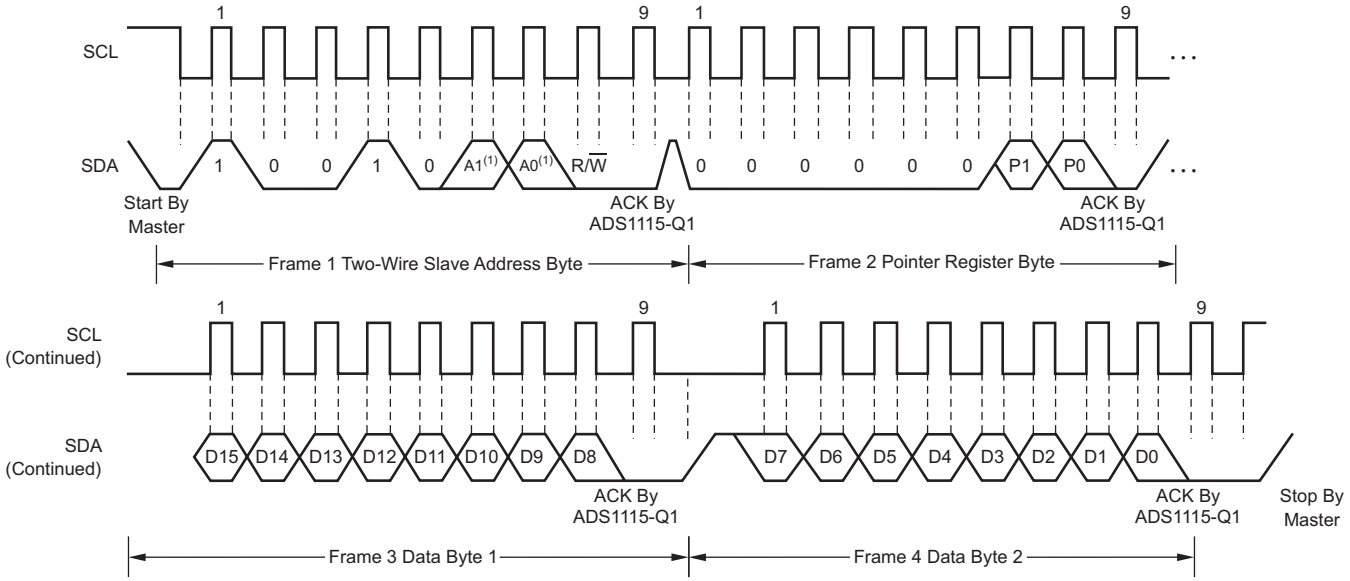
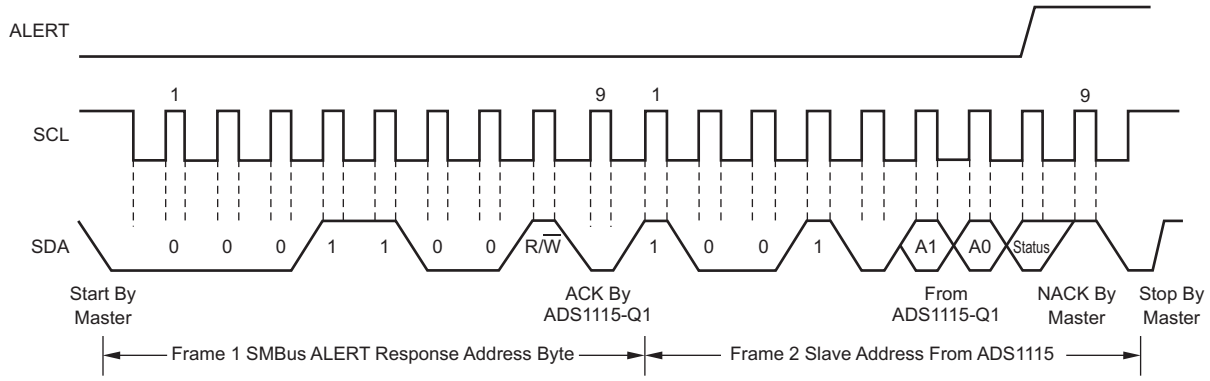


(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 29. Two-Wire Timing Diagram for Write Word Format



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 30. Timing Diagram for SMBus ALERT Response

7.5.4 Quickstart Guide

This section provides a brief example of the ADS1115-Q1 communications. Refer to subsequent sections of this data sheet for more detailed explanations. Hardware for this design includes: one ADS1115-Q1 device configured with an I^2C address of 1001000; a microcontroller with an I^2C interface (TI recommends the MSP430F2002); discrete components such as resistors, capacitors, and serial connectors; and a 2-V to 5-V power supply. Figure 31 shows the basic hardware configuration.

The ADS1115-Q1 device communicates with the master (microcontroller) through an I^2C interface. The master provides a clock signal on the SCL pin and data are transferred through the SDA pin. The ADS1115-Q1 device never drives the SCL pin. For information on programming and debugging the microcontroller being used, see the device-specific data sheet.

The first byte sent by the master should be the ADS1115-Q1 address followed by a bit that instructs the ADS1115-Q1 device to listen for a subsequent byte. The second byte is the register pointer. See the *Register Maps* section for a register map. The third and fourth bytes sent from the master are written to the register indicated in the second byte. Refer to Figure 28 and Figure 29 for read and write operation timing diagrams, respectively. All read and write transactions with the ADS1115-Q1 device must be preceded by a start condition and followed by a stop condition.

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For example, to write to the configuration register to set the ADS1115-Q1 device to continuous conversion mode and then read the conversion result, send the following bytes in this order:

- Write to Config register:
  - First byte: 0b10010000 (first 7-bit I^2C address followed by a low read/write bit)
  - Second byte: 0b00000001 (points to Config register)
  - Third byte: 0b10000100 (MSB of the Config register to be written)
  - Fourth byte: 0b10000011 (LSB of the Config register to be written)
- Write to Pointer register:
  - First byte: 0b10010000 (first 7-bit I^2C address followed by a low read/write bit)
  - Second byte: 0b00000000 (points to Conversion register)
- Read Conversion register:
  - First byte: 0b10010001 (first 7-bit I^2C address followed by a high read/write bit)
  - Second byte: the ADS1115-Q1 response with the MSB of the Conversion register
  - Third byte: the ADS1115-Q1 response with the LSB of the Conversion register

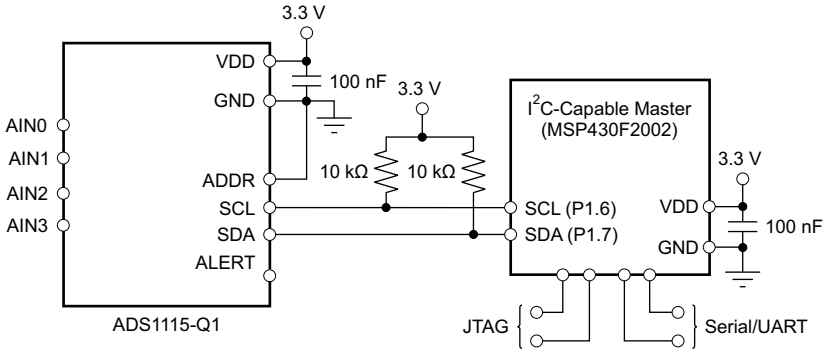

Figure 31. Basic Hardware Configuration

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7.6 Register Maps

The ADS1115-Q1 device has four registers that are accessible through the I^2C port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1115-Q1 operating modes and query the status of the devices. Two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

7.6.1 Pointer Register

The four registers are accessed by writing to the Pointer register byte; see Figure 28. Table 5 and Figure 32 indicate the Pointer register byte map.

Table 5. Register Address

BIT 1	BIT 0	REGISTER
0	0	Conversion register
0	1	Config register
1	0	Lo_thresh register
1	1	Hi_thresh register

Figure 32. Pointer Register Byte (Write-Only)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	Register address	

7.6.2 Conversion Register

The 16-bit register contains the result of the last conversion in binary twos complement format. Following a reset or power-up, the Conversion register is cleared to 0, and remains 0 until the first conversion is complete.

Figure 33 the register format.

Figure 33. Conversion Register (Read-Only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.6.3 Config Register

The 16-bit register can be used to control the ADS1115-Q1 operating mode, input selection, data rate, PGA settings, and comparator modes. Figure 34 shows the register format.

Figure 34. Config Register (Read/Write) [Default = 8583h]

15	14	13	12	11	10	9	8
OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
7	6	5	4	3	2	1	0
DR2	DR1	DR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0

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Table 6. Config Register Field Descriptions

Bit	Description
15	**OS: Operational status/single-shot conversion start** This bit determines the operational status of the device. This bit can only be written when in power-down mode. For a write status: 0 : No effect 1 : Begin a single conversion (when in power-down mode) For a read status: 0 : Device is currently performing a conversion 1 : Device is not currently performing a conversion
14-12	**MUX[2:0]: Input multiplexer configuration** These bits configure the input multiplexer. 000 : AIN_P = AIN0 and AIN_N = AIN1 (default) 001 : AIN_P = AIN0 and AIN_N = AIN3 010 : AIN_P = AIN1 and AIN_N = AIN3 011 : AIN_P = AIN2 and AIN_N = AIN3 100 : AIN_P = AIN0 and AIN_N = GND 101 : AIN_P = AIN1 and AIN_N = GND 110 : AIN_P = AIN2 and AIN_N = GND 111 : AIN_P = AIN3 and AIN_N = GND
11-9	**PGA2[2:0]: Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 : FS = ±6.144 V(1) 001 : FS = ±4.096 V(1) 010 : FS = ±2.048 V (default) 011 : FS = ±1.024 V 100 : FS = ±0.512 V 101 : FS = ±0.256 V 110 : FS = ±0.256 V 111 : FS = ±0.256 V
8	**MODE: Device operating mode** This bit controls the current operational mode of the ADS1115-Q1. 0 : Continuous conversion mode 1 : Power-down single-shot mode (default)
7-5	**DR[2:0]: Data rate** These bits control the data rate setting. 000 : 8 SPS 001 : 16 SPS 010 : 32 SPS 011 : 64 SPS 100 : 128 SPS (default) 101 : 250 SPS 110 : 475 SPS 111 : 860 SPS
4	**COMP_MODE: Comparator mode** This bit controls the comparator mode of operation. It changes whether the comparator is implemented as a traditional comparator (COMP_MODE = 0) or as a window comparator (COMP_MODE = 1). 0 : Traditional comparator with hysteresis (default) 1 : Window comparator
3	**COMP_POL: Comparator polarity** This bit controls the polarity of the ALERT/RDY pin. When COMP_POL = 0 the comparator output is active low. When COMP_POL = 1 the ALERT/RDY pin is active high. 0 : Active low (default) 1 : Active high
2	**COMP_LAT: Latching comparator** This bit controls whether the ALERT/RDY pin latches once asserted or clears once conversions are within the margin of the upper and lower threshold values. When COMP_LAT = 0, the ALERT/RDY pin does not latch when asserted. When COMP_LAT = 1, the asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master, the device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line. 0 : Non-latching comparator (default) 1 : Latching comparator
1-0	**COMP_QUE[1:0]: Comparator queue and disable** These bits perform two functions. When set to 11, they disable the comparator function and put the ALERT/RDY pin into a high state. When set to any other value, they control the number of successive conversions exceeding the upper or lower thresholds required before asserting the ALERT/RDY pin. 00 : Assert after one conversion 01 : Assert after two conversions 10 : Assert after four conversions 11 : Disable comparator (default)

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

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7.6.4 Lo_thresh and Hi_thresh Registers

The upper and lower threshold values used by the comparator are stored in two 16-bit registers. These registers store values in the same format that the output register displays values; that is, they are stored in 2s complement format. Because it is implemented as a digital comparator, special attention should be taken to readjust values whenever PGA settings are changed.

A secondary conversion ready function of the comparator output pin can be realized by setting the Hi_thresh register MSB to 1 and the Lo_thresh register MSB to 0. However, in all other cases, the Hi_thresh register must be larger than the Lo_thresh register. Figure 35 and Figure 36 show the threshold register formats. When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode and pulses when in continuous conversion mode.

Figure 35. Lo_thresh Register (Read/Writer) [Default = 8000h]

15	14	13	12	11	10	9	8
Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
7	6	5	4	3	2	1	0
Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0

Figure 36. Hi_thresh Register (Read/Write) [Default = 7FFFh]

15	14	13	12	11	10	9	8
Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
7	6	5	4	3	2	1	0
Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections give example circuits and suggestions for using the ADS1115-Q1 device in various situations.

8.1.1 Basic Connections

For many applications, connecting the ADS1115-Q1 device is simple. Figure 37 shows a basic connection diagram for the ADS1115-Q1 device.

The fully differential voltage input of the ADS1115-Q1 device is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1115-Q1 device can read bipolar differential signals, they cannot accept negative voltages on either input. It may be helpful to think of the ADS1115-Q1 positive voltage input as *noninverting*, and of the negative input as *inverting.*

When the ADS1115-Q1 device converts data, it draws current in short spikes. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1115-Q1 device interfaces directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, can operate with the ADS1115-Q1 device. The ADS1115-Q1 device does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this function unless other clock-stretching devices are on the same I^2C bus.

Pullup resistors are required on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

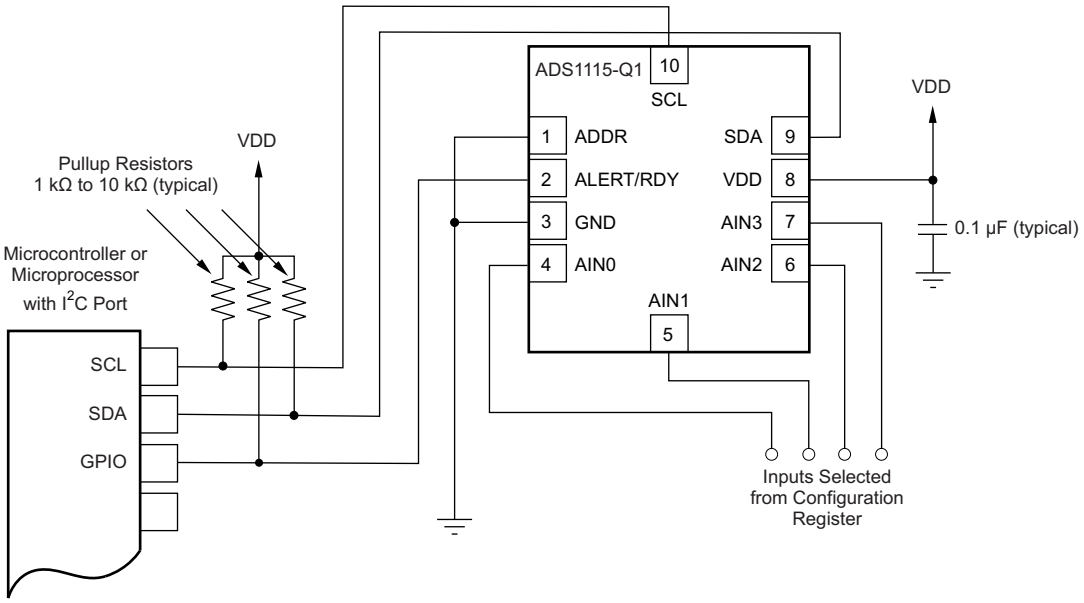

Figure 37. Typical Connections of the ADS1115-Q1

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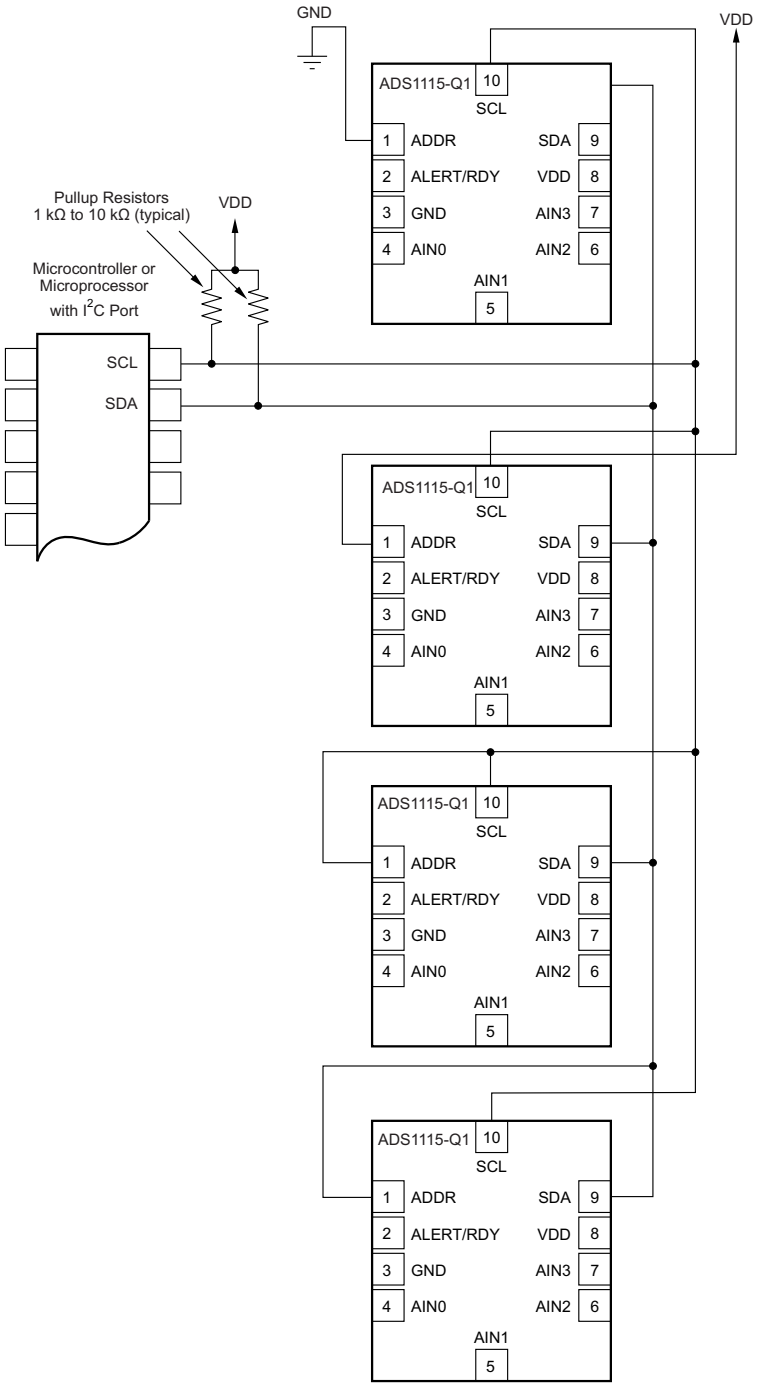
8.1.1.1 Connecting Multiple Devices

Connecting multiple ADS1115-Q1 devices to a single bus is simple. Using the address pin, the ADS1115-Q1 device can be set to one of four different I^2C addresses. Figure 38 shows an example using three ADS1115-Q1 devices. Up to four ADS1115-Q1 devices (using different address pin configurations) can be connected to a single bus.

Only one set of pullup resistors is require per bus. The pullup resistor values can be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.



The ADS1115-Q1 power and input connections are omitted for clarity. The ADDR pin selects the I^2C address.

Figure 38. Connecting Multiple ADS1115-Q1 Devices

8.1.1.2 Using GPIO Ports for Communication

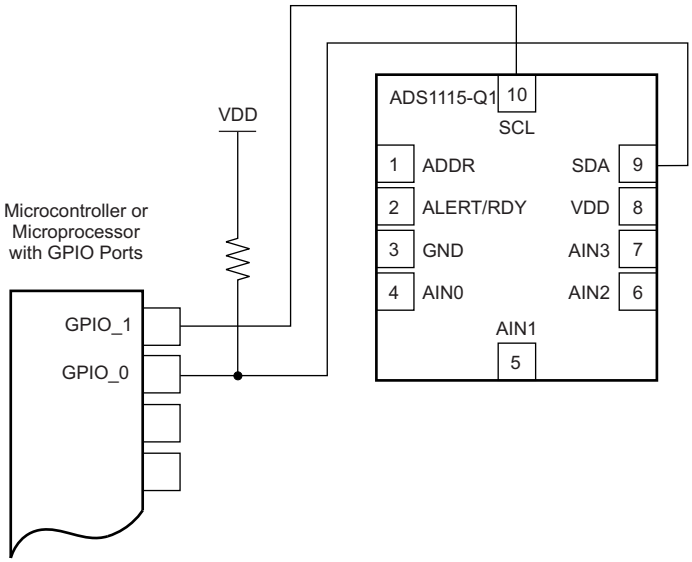
Most microcontrollers have programmable input-output (I/O) pins that can be set in software to act as inputs or outputs. If an I^2C controller is not available, the ADS1115-Q1 device can be connected to GPIO pins and the I^2C bus protocol simulated, or *bit-banged*, in software. Figure 39 shows an example of this configuration for a single ADS1115-Q1 device.

Bit-banging the I^2C with GPIO pins occurs by setting the GPIO line to 0 and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output 0; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this configuration reads as a 0 in the port input register.

Note that no pullup resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to 1 or 0 as appropriate. This action is possible because the ADS1115-Q1 never drives the clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption as a result of the absence of a resistive pullup.

If there are any devices on the bus that may drive the clock lines low, this method should not be used; the SCL line should be high-Z or 0 and a pullup resistor provided as usual.

Some microcontrollers have selectable strong pullup circuits built into the GPIO ports. In some cases, these circuits can be switched on and used in place of an external pullup resistor. Weak pullups are also provided on some microcontrollers, but usually these are too weak for I^2C communication. If there is any doubt about the matter, test the circuit before committing it to production.



ADS1115-Q1 power and input connections omitted for clarity.

Figure 39. Using GPIO with a Single ADS1115-Q1

8.1.1.3 Single-Ended Inputs

Although the ADS1115-Q1 device has two differential inputs, the device can easily measure four single-ended signals. Figure 40 shows a single-ended connection scheme. The ADS1115-Q1 device is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0 V to the supply voltage. The ADS1115-Q1 device loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1115-Q1 device can only accept positive voltages.

The ADS1115-Q1 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 40 covers only half the ADS1115-Q1 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.

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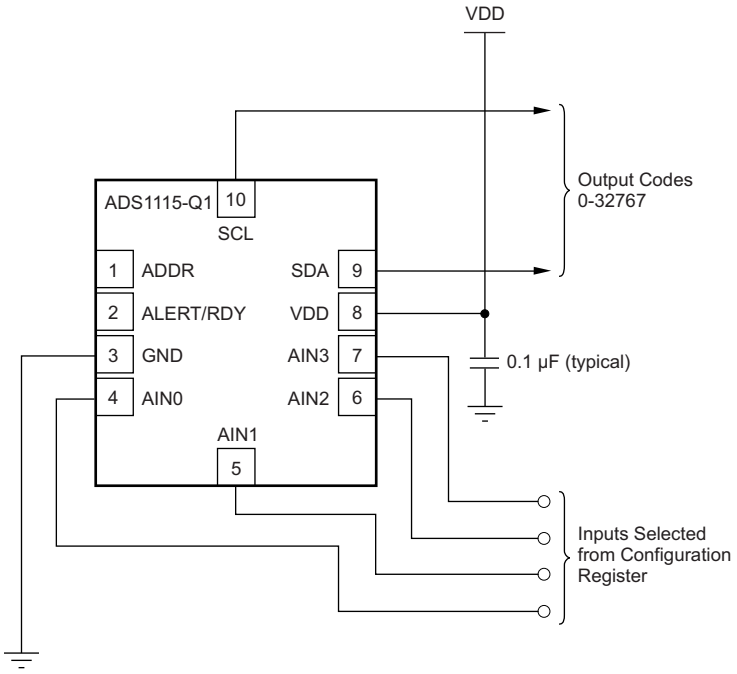

Digital and address pin connections omitted for clarity.

Figure 40. Measuring Single-Ended Inputs

8.2 Typical Applications

8.2.1 ADS1115-Q1 With Current Shunt Monitor

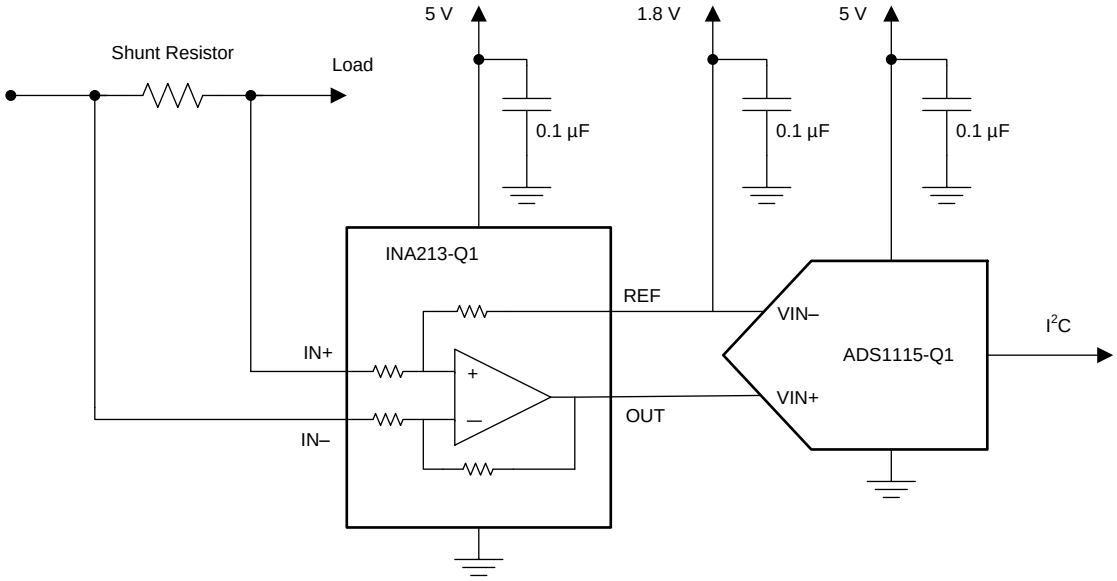

Figure 41. ADS1115-Q1 With Current Shunt Monitor

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, the ADS1115-Q1 device is paired with a current shunt monitor. Bi-directional current monitoring is required when there is both charging and discharging. The requirements for this example are as follows:

- Voltage across current shunt varies –15 mV to 15 mV
- 5-V supply
- 1.8-V rail available as reference

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Part Selection

The INA213-Q1 device was selected because of the low offset and zero drift of the device. The ADS1115-Q1 device has a low noise floor, so it can support more of the gain. For this reason, the lowest gain option was selected from the INA21x-Q1 family. The INA213-Q1 device has a gain of 50.

8.2.1.2.2 Gain Settings

First, determine the full-scale (fs) differential range into the ADS1115-Q1 device.

$$V_{fs} = VIN_{diff} \times G_{INA213} \quad (2)$$

$$V_{fs} = \pm 15mV \times 50 \quad (3)$$

$$V_{fs} = \pm 0.75V \quad (4)$$

By looking at Table 2, the PGA setting of 4 is the closest gain setting that will satisfy the full-scale range requirements.

8.2.1.2.3 Circuit Implementation

Because the ADS1115-Q1 device has a differential input, connect the reference voltage of the INA213-Q1 device to the negative input terminal of the ADS1115-Q1 device. Because bi-directional current sensing is required in this application, VREF must be chosen so that:

$$VREF > \frac{V_{fs}}{2} \quad (5)$$

$$VREF < V_{supply} - \frac{V_{fs}}{2} \quad (6)$$

- where V_{fs} = 1.5 V

A 1.8-V reference is used for this example. Because the ADS1115-Q1 device is a differential input ADC, a resistive divider can be used to generate the reference voltage because impedance effects on the INA213-Q1 device is canceled out by the ADS1115-Q1 device.

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Typical Applications (continued)

8.2.1.3 Application Curve

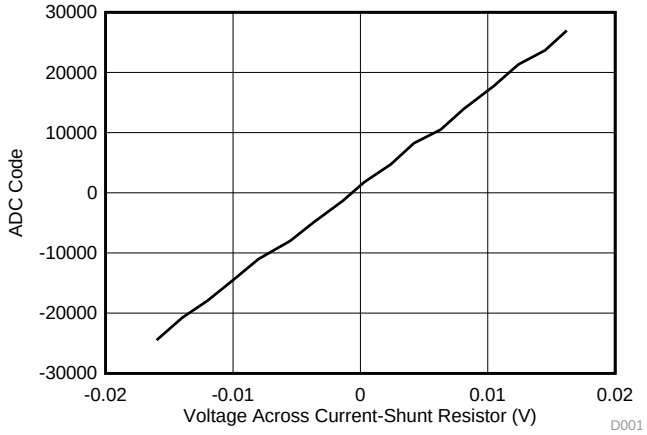
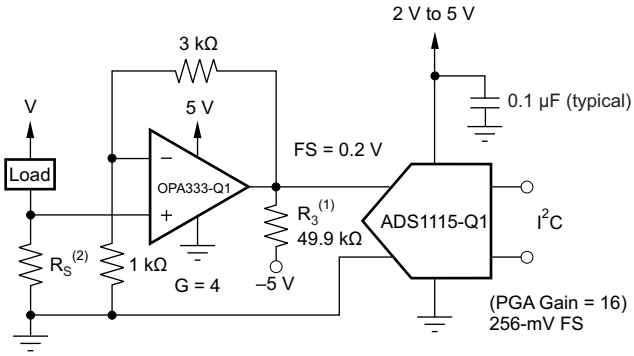


Figure 42. ADC Code vs Voltage Across Current-Shunt Resistor in Bi-Directional Current Sensing Application

8.2.2 Low-Side Current Monitor



(1) Pulldown resistor to allow accurate swing to 0V.

(2) R_S is sized for a 50-mV drop at full-scale current.

Figure 43. Low-Side Current Measurement

8.2.2.1 Design Requirements

Figure 43 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an OPA333-Q1 low-drift operational amplifier, and the result is read by the ADS1115-Q1 device. The maximum voltage across the current shunt is 50 mV. This design uses a 5-V power supply.

8.2.2.2 Detailed Design Procedure

Texas Instruments recommends operating the ADS1115-Q1 device with a gain of 8. The gain of the OPA333-Q1 device can then be set lower. For a gain of 16, the operational amplifier should be set up to give a maximum output voltage no greater than 0.256 V. If the shunt resistor is sized to provide a maximum voltage drop of 50 mV at full-scale current, the full-scale input to the ADS1115-Q1 device is 0.2 V.

The ADS1115-Q1 device is fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1115-Q1 device can be permanently damaged by analog input voltages that remain more than approximately 300 mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1115-Q1 analog inputs can withstand momentary currents as large as 100 mA.

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Typical Applications (continued)

If the ADS1115-Q1 device is driven by an operational amplifier with high-voltage supplies, such as ±12 V, protection should be provided, even if the operational amplifier is configured so that it does not output out-of-range voltages. Many operational amplifiers drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1115-Q1 device. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an operational amplifier or other front-end circuitry is used with an ADS1115-Q1 device, performance characteristics must be taken into account when designing the application.

9 Power Supply Recommendations

The device requires only one power supply, VDD, which can have an input voltage between 2 V and 5.5 V. The value of VDD affects the input voltage range and the digital logic high and low levels.

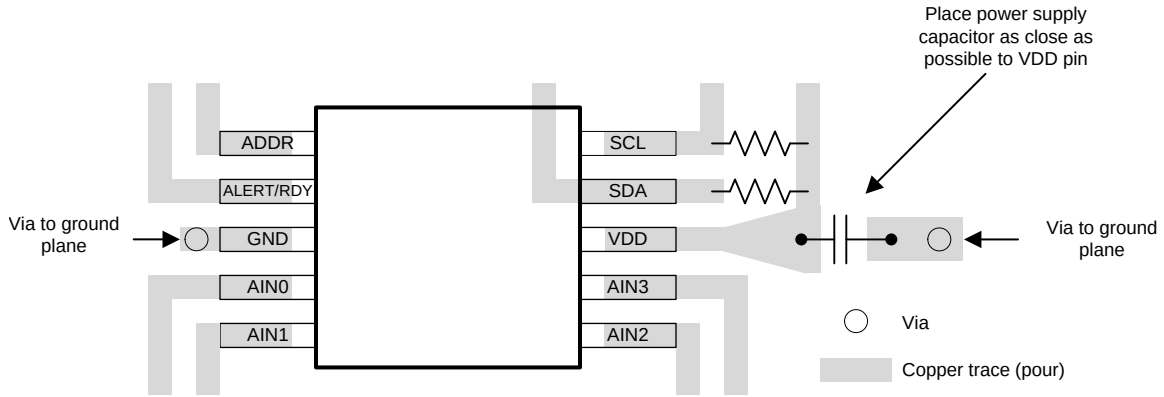
A decoupling capacitor should be placed close to the VDD pin. A value of at least 0.1 µF is recommended.

10 Layout

10.1 Layout Guidelines

An optimum layout for the ADS1115-Q1 device helps to reduce noise and improve performance. The decoupling capacitor on the VDD pin should be placed as close to the VDD pin as possible. Also, the analog input pins (AIN0, AIN1, AIN2, and AIN3) should be routed carefully to reduce noise.

10.2 Layout Example



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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *INA21x-Q1 Automotive-Grade Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*, SBOS475
- *OPA333-Q1 1.8-V Micropower CMOS Operational Amplifier Zero-Drift Series* data sheet (SBOS522)
- *MSP430F20xx Mixed Signal Controllers* data sheet (SLAS491)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1115QDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BCOQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS1115-Q1 :

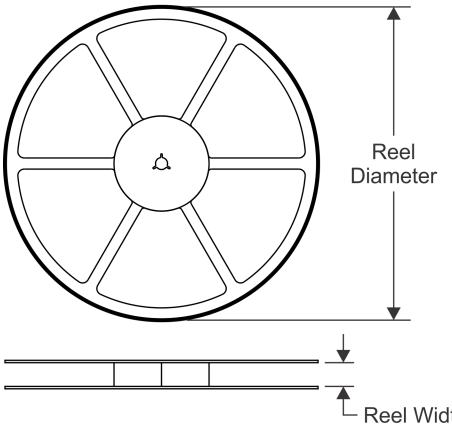
- Catalog: ADS1115

NOTE: Qualified Version Definitions:

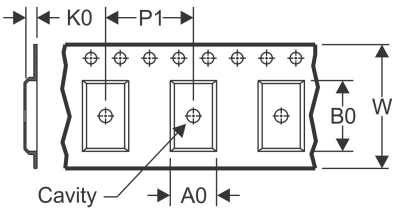
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

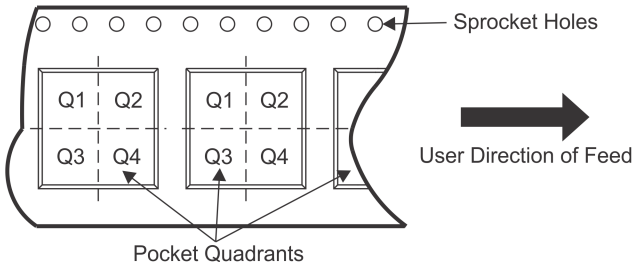


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

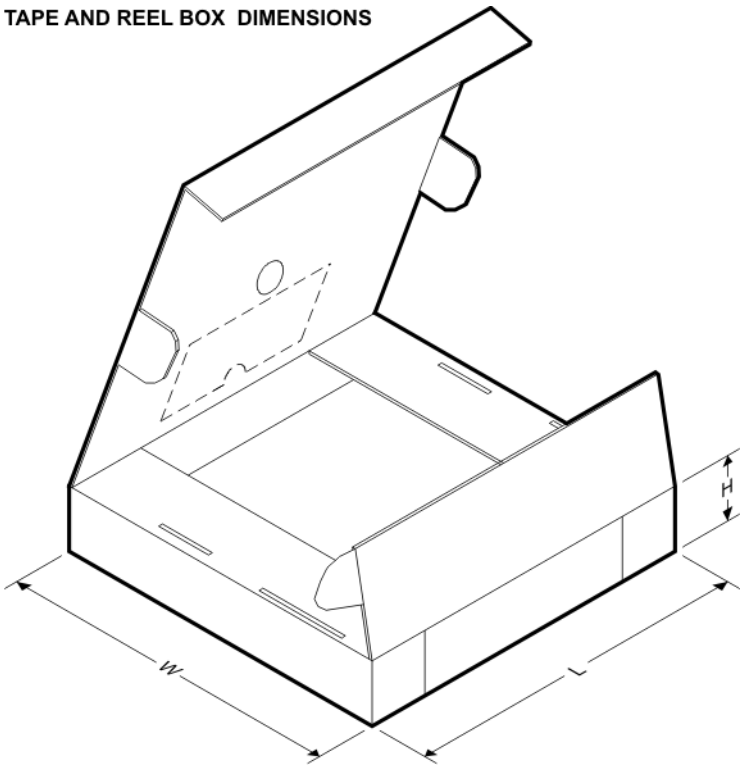
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1115QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

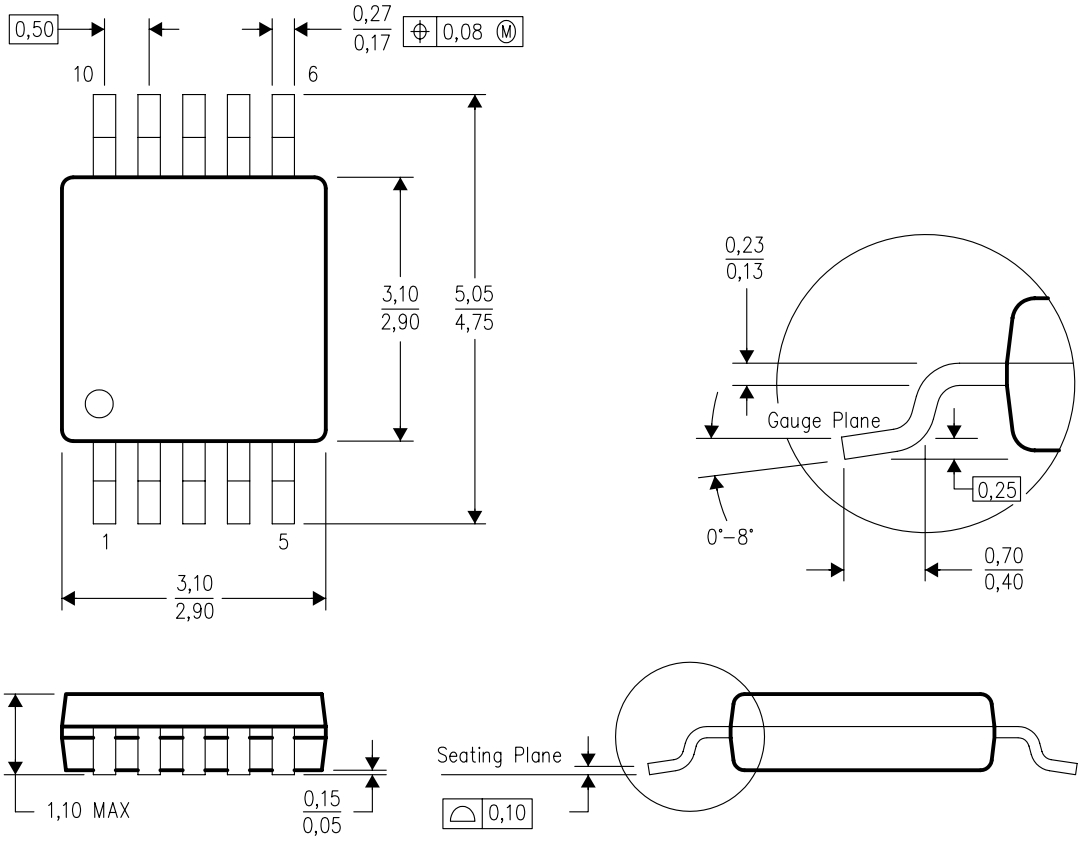
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1115QDGSRQ1	VSSOP	DGS	10	2500	370.0	355.0	55.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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