

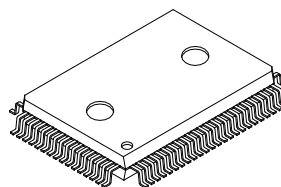
## CMOS 8-bit Single Chip Microcomputer

### Description

The CXP82316/82320/82324 microcomputer is composed of a CPU, ROM and RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, fluorescent display controller/driver, remote control receiver.

This device also includes a power-on reset function and sleep/stop functions which can be used to achieve low power consumption.

80 pin QFP (Plastic)



### Features

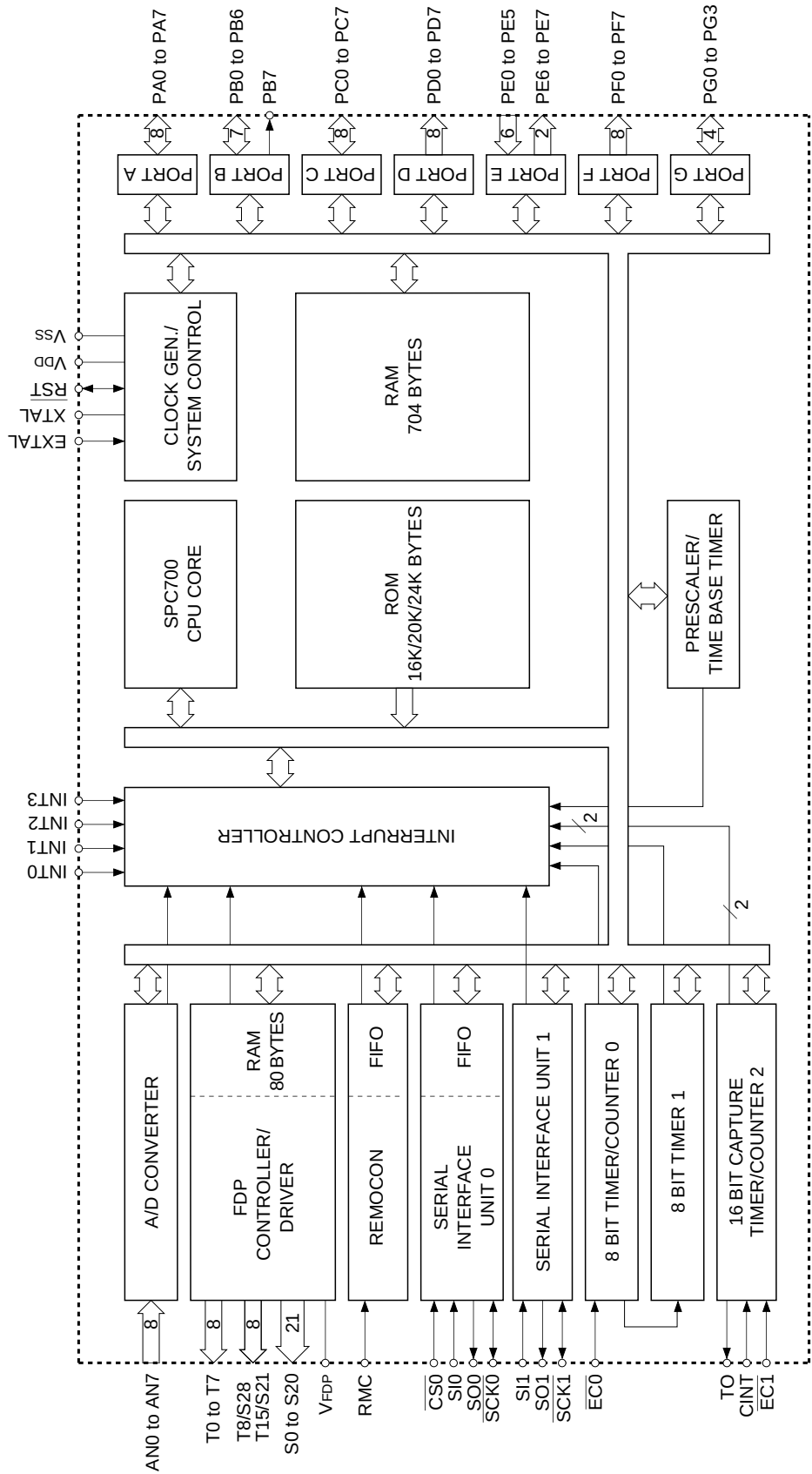
- Instruction set which supports a wide array of data types
  - 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle      400ns for 10MHz operation
- On-chip ROM      16K bytes (CXP82316)  
                          20K bytes (CXP82320)  
                          24K bytes (CXP82324)
- On-chip RAM      704 bytes (Including fluorescent display data area)
- Peripheral functions:
  - A/D converter      8-bit, 8-channel, successive approximation system  
                                  (conversion rate 32μs/10MHz)
  - Serial interface      On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer) 1 channel  
                                  8-bit clock synchronized 1 channel
  - Timers      8-bit timer  
                          8-bit timer/counter  
                          19-bit time-base timer  
                          16-bit capture timer/counter
  - Fluorescent display controller/driver      Maximum of 336 segment display available  
                                  1 to 16 digits dynamic display  
                                  Dimmer function  
                                  High voltage tolerant output (40V)  
                                  On-chip pull-down resistor (Mask option)
  - Remote control receiver circuit      On-chip noise elimination circuit  
                                  On-chip 6 stage FIFO 8-bit pulse measurement counter
- Interrupts      14 factors, 15 vectors multi-interruption possible
- Standby mode      Sleep/stop
- Package      80-pin plastic QFP
- Piggyback/evaluator      CXP82300 80-pin ceramic QFP

### Structure

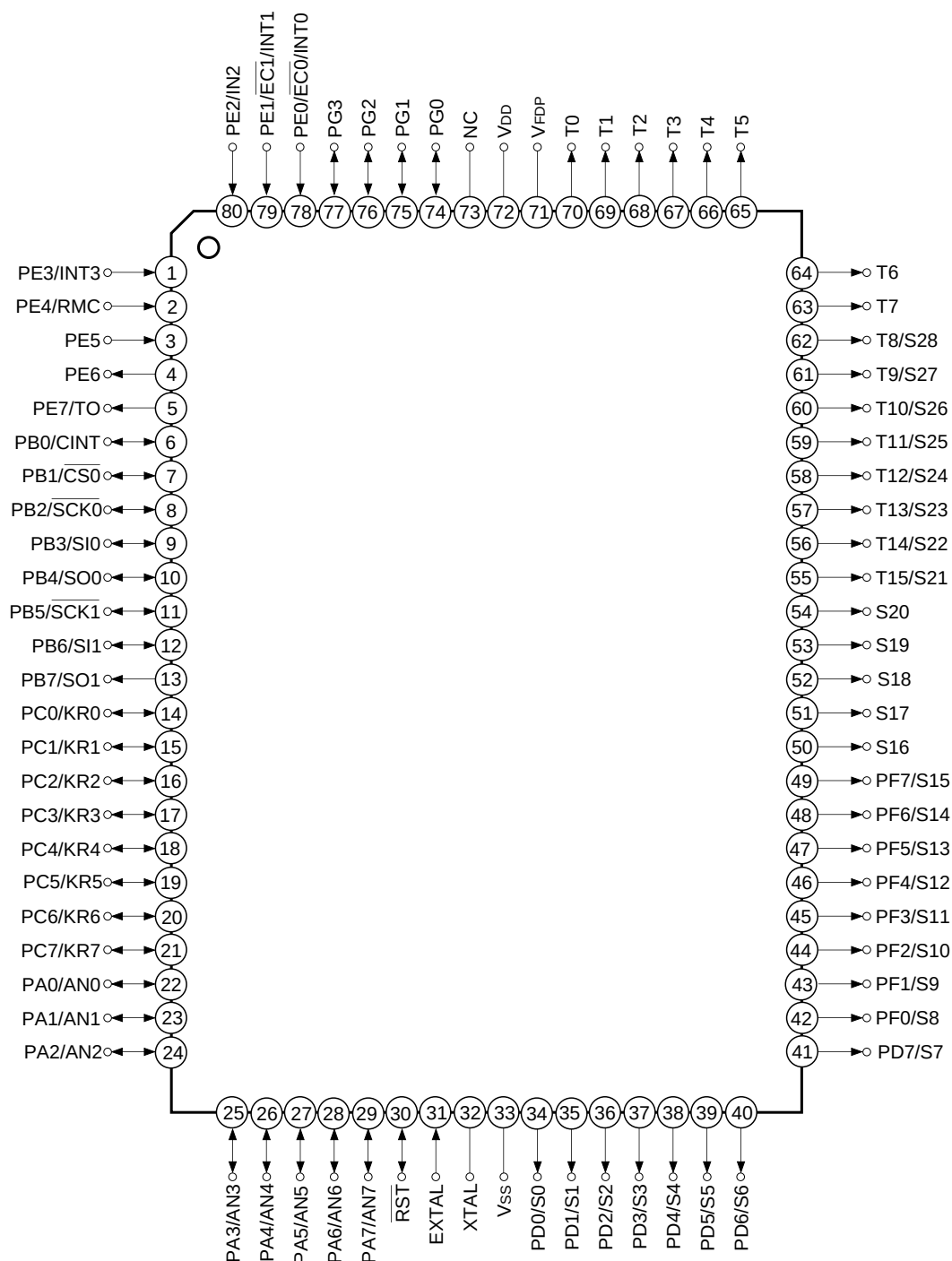
Silicon gate CMOS IC

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Block Diagram



## Pin Assignment (Top View)



**Note)** NC (Pin 73) is always connected to V<sub>DD</sub>.

# Pin Description

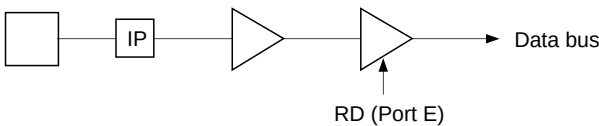
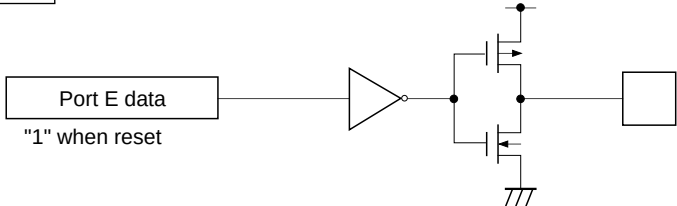
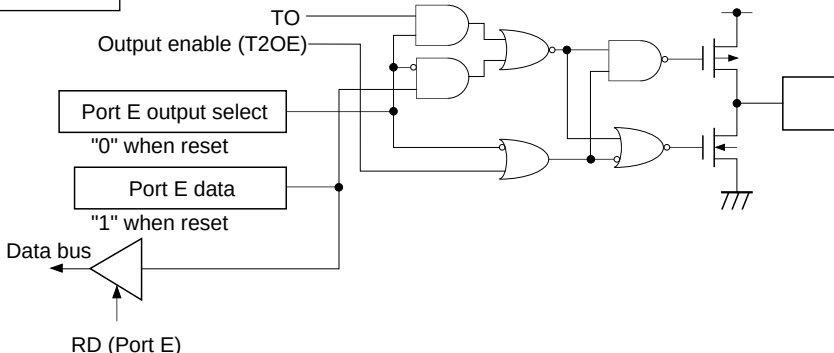
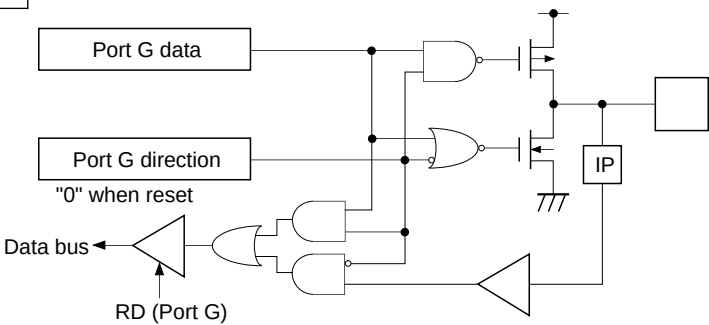
| Symbol                            | I/O               | Description                                                                                                               |                                                                                                  |                                                                          |
|-----------------------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| PA0/AN0<br>to<br>PA7/AN7          | I/O/Analog input  | (Port A)<br>8-bit port; single bit<br>addressable.<br>(8 pins)                                                            | Analog inputs to A/D converter.<br>(8 pins)                                                      |                                                                          |
| PB0/CINT                          | I/O/Input         | (Port B)<br>Single bit addressable from<br>amongst lower 7 bits;<br>highest bit (PB7)<br>dedicated to output.<br>(8 pins) | External capture input to 16-bit timer/counter                                                   |                                                                          |
| PB1/ $\overline{\text{CS}}0$      | I/O/Input         |                                                                                                                           | Chip select input for serial interface (CH0).                                                    |                                                                          |
| PB2/ $\overline{\text{SCK}}0$     | I/O/I/O           |                                                                                                                           | Serial clock (CH0) input/output.                                                                 |                                                                          |
| PB3/SI0                           | I/O/Input         |                                                                                                                           | Serial data (CH0) input.                                                                         |                                                                          |
| PB4/SO0                           | I/O/Output        |                                                                                                                           | Serial data (CH0) output.                                                                        |                                                                          |
| PB5/ $\overline{\text{SCK}}1$     | I/O/I/O           |                                                                                                                           | Serial clock (CH1) input/output.                                                                 |                                                                          |
| PB6/SI1                           | I/O/Input         |                                                                                                                           | Serial data (CH1) input.                                                                         |                                                                          |
| PB7/SO1                           | Output/Output     |                                                                                                                           | Serial data (CH1) output.                                                                        |                                                                          |
| PC0/KR0<br>to<br>PC7/KR7          | I/O/Input         |                                                                                                                           | (Port C)<br>8-bit port; single bit<br>addressable. Can provide<br>12mA sink current.<br>(8 pins) | Key return input for FDP segment signal.<br>which performs key scanning. |
| PE0/INT0/ $\overline{\text{EC}}0$ | Input/Input/Input | (Port E)<br>8-bit port with lower 6 bits<br>dedicated to input and<br>upper 2 bits dedicated to<br>output.<br>(8 pins)    | Input for external<br>interrupt requests.<br>(4 pins)                                            | External event input<br>to timer/counter.<br>(2 pins)                    |
| PE1/INT1/ $\overline{\text{EC}}1$ | Input/Input/Input |                                                                                                                           |                                                                                                  |                                                                          |
| PE2/INT2                          | Input/Input       |                                                                                                                           | Input for remote control receiver circuit.                                                       |                                                                          |
| PE3/INT3                          | Input/Input       |                                                                                                                           |                                                                                                  |                                                                          |
| PE4/RMC                           | Input/Input       |                                                                                                                           |                                                                                                  |                                                                          |
| PE5                               | Input             |                                                                                                                           |                                                                                                  |                                                                          |
| PE6                               | Output            |                                                                                                                           |                                                                                                  |                                                                          |
| PE7/TO                            | Output/Output     | Output pin for 16-bit timer/counter<br>rectangular waveform.                                                              |                                                                                                  |                                                                          |
| PG0 to PG3                        | I/O               | (Port G)<br>4-bit input/output port; single bit addressable.<br>(4 pins)                                                  |                                                                                                  |                                                                          |
| PF0/S8<br>to<br>PF7/S15           | Output/Output     | (Port F)<br>8-bit dedicated output port.<br>(8 pins)                                                                      | Segment signal<br>output for FDP.                                                                |                                                                          |
| S16 to S20                        | Output            | Segment signal output for FDP.                                                                                            |                                                                                                  |                                                                          |
| T8/S28<br>to<br>T15/S21           | Output/Output     | Dual purpose output for FDP timing and segment signals.                                                                   |                                                                                                  |                                                                          |
| T0 to T7                          | Output            | Timing signal output for FDP.                                                                                             |                                                                                                  |                                                                          |
| PD0/S0<br>to<br>PD7/S7            | Output/Output     | (Port D)<br>8-bit dedicated output port.<br>(8 pins)                                                                      | Segment signal output for FDP.                                                                   |                                                                          |

| Symbol                  | I/O    | Description                                                                                                                                                                                   |
|-------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>FDP</sub>        |        | Provides voltage for FDP when on-chip resistor is selected under mask option.                                                                                                                 |
| EXTAL                   | Input  | Connection for system clock oscillation crystal. When using an external clock, input normal signal to EXTAL and reverse phase signal to the XTAL pin.                                         |
| XTAL                    | Output |                                                                                                                                                                                               |
| $\overline{\text{RST}}$ | I/O    | System reset, active "L". The $\overline{\text{RST}}$ pin is an input/output pin which outputs a "L" level from the on-chip power on reset circuit when the power is turned on. (Mask option) |
| NC                      |        | NC pin is always connected to V <sub>DD</sub> .                                                                                                                                               |
| V <sub>DD</sub>         |        | Positive power supply pin.                                                                                                                                                                    |
| V <sub>SS</sub>         |        | GND                                                                                                                                                                                           |

Input/Output Circuit Formats for Pins

| Pin                                                                       | Circuit format    | When reset |
|---------------------------------------------------------------------------|-------------------|------------|
| <div>PA0/AN0<br/>to<br/>PA7/AN7</div> <div>8 pins</div>                   | <div>Port A</div> | Hi-Z       |
| <div>PB0/CINT<br/>PB1/CS0<br/>PB3/SI0<br/>PB6/SI1</div> <div>4 pins</div> | <div>Port B</div> | Hi-Z       |
| <div>PB2/SCK0<br/>PB5/SCK1</div> <div>2 pins</div>                        | <div>Port B</div> | Hi-Z       |

| Pin                                                                                                                       | Circuit format                                                  | When reset |
|---------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|------------|
| PB4/SO0<br><br>1 pin                                                                                                      | <div>Port B</div>                                               | Hi-Z       |
| PB7/SO1<br><br>1 pin                                                                                                      | <div>Port B</div> <p>*Pull-up transistor</p>                    | High level |
| PC0/KR0 to PC7/KR7<br><br>8 pins                                                                                          | <div>Port C</div> <p>*Capable of driving 12mA large current</p> | Hi-Z       |
| PE0/ $\overline{\text{EC0}}$ /INT0<br>PE1/ $\overline{\text{EC1}}$ /INT1<br>PE2/INT2<br>PE3/INT3<br>PE4/RMC<br><br>5 pins | <div>Port E</div>                                               | Hi-Z       |

| Pin                                     | Circuit format                                                                                                    | When reset |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------|
| <div>PE5</div> <div>1 pin</div>         | <div>Port E</div> <div></div>   | Hi-Z       |
| <div>PE6</div> <div>1 pin</div>         | <div>Port E</div> <div></div>   | High level |
| <div>PE7/TO</div> <div>1 pin</div>      | <div>Port E</div> <div></div>  | High level |
| <div>PG0 to PG3</div> <div>4 pins</div> | <div>Port G</div> <div></div> | Hi-Z       |

| Pin                                                    | Circuit format                                                                                                                                                                                                                                                                                                                   | When reset                                        |
|--------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| PD0/S0 to PD7/S7<br>PF0/S8 to PF7/S15<br>16 pins       | <p>Port D</p> <p>Port F</p> <p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>Port D data or Port F data</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port D or Port F)</p> <p>*High voltage tolerant transistor</p> <p>Pull-down resistor</p> <p>Mask option</p> <p>V<sub>FDP</sub></p> | Hi-Z or Low level (when PD resistor is connected) |
| S16 to S20<br>T15/S21 to T8/S28<br>T0 to T7<br>21 pins | <p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>*High voltage tolerance transistor</p> <p>Pull-down resistor</p> <p>Mask option</p> <p>V<sub>FDP</sub></p>                                                                                                                                 | Hi-Z or Low level (when PD resistor is connected) |
| EXTAL<br>XTAL<br>2 pins                                | <p>EXTAL</p> <p>XTAL</p> <p>IP</p> <p>IP</p> <p>*Diagram shows circuit construction for oscillation.</p> <p>*During stop feedback resistor is disconnected.</p>                                                                                                                                                                  | Oscillation                                       |
| $\overline{\text{RST}}$<br>1 pin                       | <p>Pull-up resistor</p> <p>Mask option</p> <p>From power on reset circuit (Mask option)</p> <p>Schmitt input</p>                                                                                                                                                                                                                 | Low level                                         |

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

| Item                            | Symbol            | Rating                                        | Unit | Remarks                                                                                   |
|---------------------------------|-------------------|-----------------------------------------------|------|-------------------------------------------------------------------------------------------|
| Supply voltage                  | V <sub>DD</sub>   | −0.3 to +7.0                                  | V    |                                                                                           |
| Input voltage                   | V <sub>IN</sub>   | −0.3 to +7.0* <sup>1</sup>                    | V    |                                                                                           |
| Output voltage                  | V <sub>OUT</sub>  | −0.3 to +7.0* <sup>1</sup>                    | V    |                                                                                           |
| Display output voltage          | V <sub>OD</sub>   | V <sub>DD</sub> − 40 to V <sub>DD</sub> + 0.3 | V    | As P channel transistor is open drain, V <sub>DD</sub> voltage is determined as standard. |
| High level output current       | I <sub>OH</sub>   | −5                                            | mA   | Other than display output pins* <sup>2</sup> : per pin                                    |
|                                 | I <sub>ODH1</sub> | −15                                           | mA   | Display outputs S0 to S20: per pin                                                        |
|                                 | I <sub>ODH2</sub> | −35                                           | mA   | Display outputs T0 to T7, T8/S28 to T15/S21: per pin                                      |
| High level total output current | ΣI <sub>OH</sub>  | −40                                           | mA   | Total of other than display output pins                                                   |
|                                 | ΣI <sub>ODH</sub> | −100                                          | mA   | Total of display output pins                                                              |
| Low level output current        | I <sub>OL</sub>   | 15                                            | mA   | Port 1 pin                                                                                |
|                                 | I <sub>OLC</sub>  | 20                                            | mA   | Large current port pin * <sup>3</sup>                                                     |
| Low level total output current  | ΣI <sub>OL</sub>  | 100                                           | mA   | Entire pin total                                                                          |
| Operating temperature           | T <sub>opr</sub>  | −20 to +75                                    | °C   |                                                                                           |
| Storage temperature             | T <sub>stg</sub>  | −55 to +150                                   | °C   |                                                                                           |
| Allowable power dissipation     | P <sub>D</sub>    | 600                                           | mW   |                                                                                           |

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> cannot exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> Rating for output current of general input/output port.

\*<sup>3</sup> The large current drive transistor is an N-channel transistor of Port C.

**Note)** If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

| Item                     | Symbol            | Min.                  | Max.                  | Unit | Remarks                                                            |
|--------------------------|-------------------|-----------------------|-----------------------|------|--------------------------------------------------------------------|
| Supply voltage           | V <sub>DD</sub>   | 4.5                   | 5.5                   | V    | High-speed mode (1/2, 1/4 clock) guaranteed range during operation |
|                          |                   | 3.5                   | 5.5                   |      | Low-speed mode (1/16 clock) guaranteed range during operation      |
|                          |                   | 2.5                   | 5.5                   |      | Guaranteed data hold operation range during stop                   |
| High level input voltage | V <sub>IH</sub>   | 0.7V <sub>DD</sub>    | V <sub>DD</sub>       | V    | *1                                                                 |
|                          | V <sub>IHS</sub>  | 0.8V <sub>DD</sub>    | V <sub>DD</sub>       | V    | Hysteresis input*2                                                 |
|                          | V <sub>IHEX</sub> | V <sub>DD</sub> - 0.4 | V <sub>DD</sub> + 0.3 | V    | EXTAL pin*3                                                        |
| Low level input voltage  | V <sub>IL</sub>   | 0                     | 0.3V <sub>DD</sub>    | V    | *1                                                                 |
|                          | V <sub>ILS</sub>  | 0                     | 0.2V <sub>DD</sub>    | V    | Hysteresis input                                                   |
|                          | V <sub>ILEX</sub> | -0.3                  | 0.4                   | V    | EXTAL pin*3                                                        |
| Operating temperature    | T <sub>opr</sub>  | -20                   | +75                   | °C   |                                                                    |

\*1 All regular input ports (PA, PB3, PB4, PB6, PC, PE5, PG).

\*2 For pins  $\overline{\text{RST}}$ , CINT,  $\overline{\text{CS0}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SCK1}}$ ,  $\overline{\text{EC0/INT0}}$ ,  $\overline{\text{EC1/INT1}}$ , INT2, INT3, RMC.

\*3 Rating only for external clock input.

# Electrical Characteristics

## DC Characteristics

(Ta = -20 to +75°C, Vss = 0V)

| Item                                                  | Symbol            | Pins                                                                                                         | Conditions                                                                                                    | Min. | Typ. | Max. | Unit |
|-------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|------|------|------|------|
| High level output voltage                             | V <sub>OH</sub>   | PA, PB, PC, PE6, PE7, PG, $\overline{\text{RST}}$ *1 (for V <sub>OL</sub> only)                              | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = −0.5mA                                                              | 4.0  |      |      | V    |
|                                                       |                   |                                                                                                              | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = −1.2mA                                                              | 3.5  |      |      | V    |
| Low level output voltage                              | V <sub>OL</sub>   |                                                                                                              | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA                                                               |      |      | 0.4  | V    |
|                                                       |                   |                                                                                                              | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA                                                               |      |      | 0.6  | V    |
|                                                       |                   | PC                                                                                                           | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA                                                              |      |      | 1.5  | V    |
| Input current                                         | I <sub>IHE</sub>  | EXTAL                                                                                                        | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V                                                                | 0.5  |      | 40   | μA   |
|                                                       | I <sub>IIE</sub>  |                                                                                                              | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                                | −0.5 |      | −40  | μA   |
|                                                       | I <sub>ILR</sub>  | $\overline{\text{RST}}$ *2                                                                                   | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                                | −1.5 |      | −400 | μA   |
| Display output current                                | I <sub>OH</sub>   | S0 to S20                                                                                                    | V <sub>DD</sub> = 4.5V<br>V <sub>OH</sub> = V <sub>DD</sub> − 2.5V                                            | −8   |      |      | mA   |
|                                                       |                   | S21/T15 to S28/T8<br>T0 to T7                                                                                |                                                                                                               | −20  |      |      | mA   |
| Open drain output leakage current (P-CH Tr off state) | I <sub>IOL</sub>  | S0 to S20<br>S21/T15 to S28/T8<br>T0 to T7                                                                   | V <sub>DD</sub> = 5.5V<br>V <sub>OL</sub> = V <sub>DD</sub> − 35V<br>V <sub>FDP</sub> = V <sub>DD</sub> − 35V |      |      | −20  | μA   |
| Pull-down resistor*3                                  | R <sub>L</sub>    | S0 to S20<br>S21/T15 to S28/T8<br>T0 to T7                                                                   | V <sub>DD</sub> = 5V<br>V <sub>OD</sub> − V <sub>FDP</sub> = 30V                                              | 60   | 100  | 270  | kΩ   |
| Input/output leak current                             | I <sub>Iz</sub>   | PA to PC, PE, PG, $\overline{\text{RST}}$ *2                                                                 | V <sub>DD</sub> = 5.5V<br>V <sub>I</sub> = 0, 5.5V                                                            |      |      | ±10  | μA   |
| Supply current*4                                      | I <sub>DD1</sub>  | V <sub>DD</sub>                                                                                              | V <sub>DD</sub> = 5.5V<br>High-speed mode (1/2 clock) operation                                               |      | 25   | 40   | mA   |
|                                                       |                   |                                                                                                              | 10MHz crystal oscillator (C <sub>1</sub> = C <sub>2</sub> = 15pF)                                             |      |      |      |      |
|                                                       | I <sub>DDSL</sub> |                                                                                                              | Sleep mode                                                                                                    |      | 3    | 8    | mA   |
|                                                       | I <sub>DDST</sub> |                                                                                                              | Stop mode                                                                                                     |      |      | 10   | μA   |
| Input capacitance                                     | C <sub>IN</sub>   | For pins other than S0 to S28, T0 to T7, PB7, PE6, PE7, V <sub>DD</sub> , V <sub>SS</sub> , V <sub>FDP</sub> | 1MHz clock<br>0V other than measured                                                                          |      | 10   | 20   | pF   |

\*1 RST pin is rated only when the power-on reset circuit is selected under the mask option.

\*2 RST pin is rated for input current when the pull-up resistor is selected; otherwise it is rated for leak current.

\*3 Applies when the on-chip pull-down resistor is selected under the mask option.

\*4 All output pins are left open.

## AC Characteristics

## (1) Clock timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

| Item                                             | Symbol                               | Pins                                                 | Conditions                              | Min.                   | Max. | Unit |
|--------------------------------------------------|--------------------------------------|------------------------------------------------------|-----------------------------------------|------------------------|------|------|
| System clock frequency                           | f <sub>C</sub>                       | XTAL<br>EXTAL                                        | Fig. 1, Fig. 2                          | 1                      | 10   | MHz  |
| System clock input pulse width                   | t <sub>XL</sub> ,<br>t <sub>XH</sub> | EXTAL                                                | Fig. 1, Fig. 2<br>External clock driver | 45                     |      | ns   |
| System clock input rising and falling times      | t <sub>CR</sub> ,<br>t <sub>CF</sub> | EXTAL                                                | Fig. 1, Fig. 2<br>External clock driver |                        | 200  | ns   |
| Event count input clock pulse width              | t <sub>EH</sub> ,<br>t <sub>EL</sub> | $\overline{\text{EC0}}$ ,<br>$\overline{\text{EC1}}$ | Fig. 3                                  | t <sub>sys</sub> + 50* |      | ns   |
| Event count input clock rising and falling times | t <sub>ER</sub> ,<br>t <sub>EF</sub> | $\overline{\text{EC0}}$ ,<br>$\overline{\text{EC1}}$ | Fig. 3                                  |                        | 20   | ms   |

\* t<sub>sys</sub> is determined by the upper two bits of the clock control register (Address: 00FE<sub>H</sub>; CPU clock selected) resulting in one of the 3 following values:

t<sub>sys</sub> [ns] = 2000/f<sub>C</sub> (Upper 2 bits = "00"), 4000/f<sub>C</sub> (Upper 2 bits = "01"), 16000/f<sub>C</sub> (Upper 2 bits = "11")

Fig. 1. Clock timing

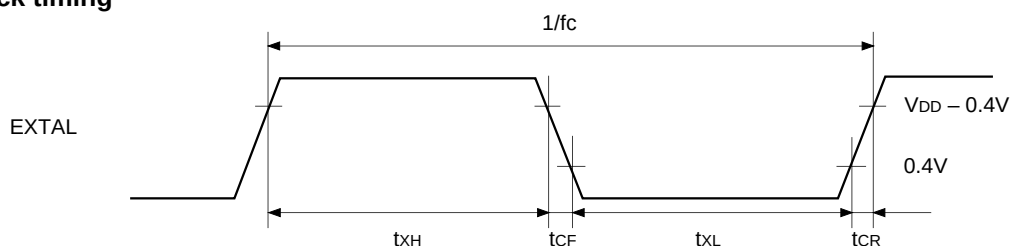


Fig. 2. Clock applying condition

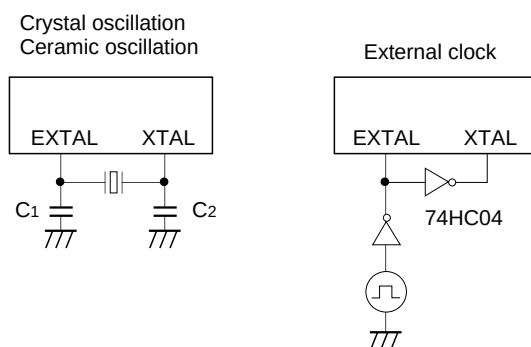
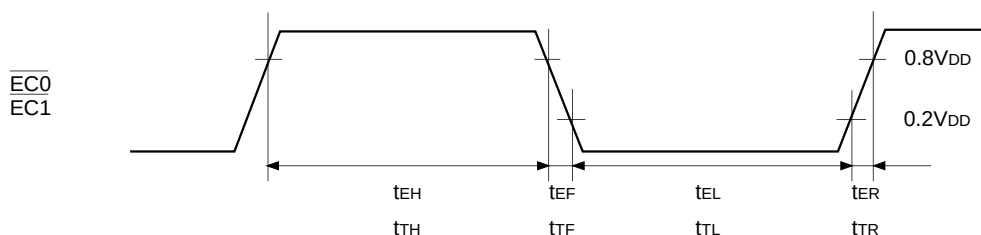


Fig. 3. Event count clock timing



## (2) Serial transfer (CH0)

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

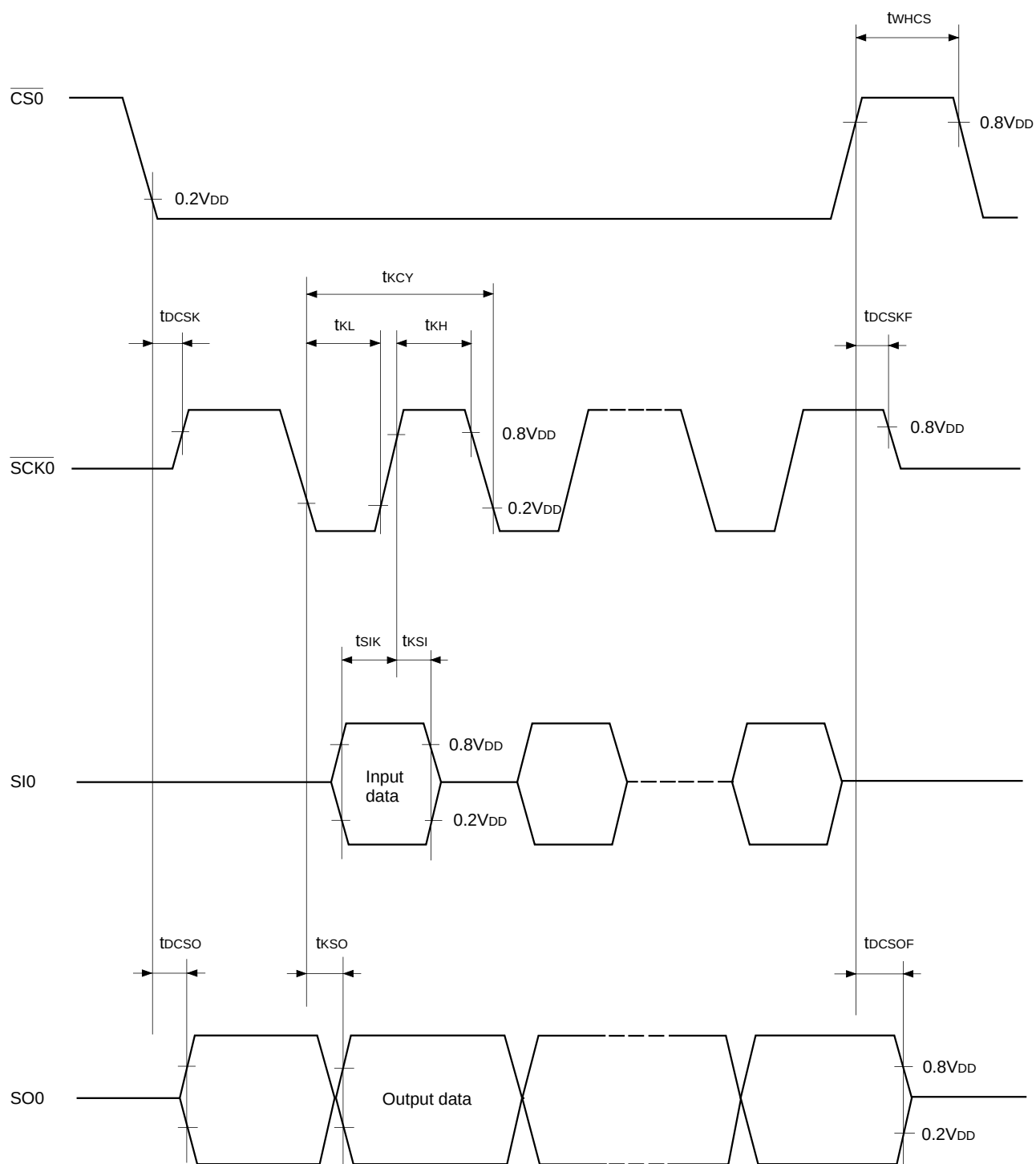
| Item                                                                                    | Symbol                             | Pin                      | Condition                                                              | Min.                    | Max.                   | Unit |
|-----------------------------------------------------------------------------------------|------------------------------------|--------------------------|------------------------------------------------------------------------|-------------------------|------------------------|------|
| $\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$<br>delay time     | $t_{\text{DCSK}}$                  | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK0}}$ = output mode) |                         | $t_{\text{sys}} + 200$ | ns   |
| $\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$<br>float delay time | $t_{\text{DCSKF}}$                 | $\overline{\text{SCK0}}$ | Chip select transfer mode<br>( $\overline{\text{SCK0}}$ = output mode) |                         | $t_{\text{sys}} + 200$ | ns   |
| $\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$<br>delay time                 | $t_{\text{DCSO}}$                  | SO0                      | Chip select transfer mode                                              |                         | $t_{\text{sys}} + 200$ | ns   |
| $\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$<br>float delay time             | $t_{\text{DCSOF}}$                 | SO0                      | Chip select transfer mode                                              |                         | $t_{\text{sys}} + 200$ | ns   |
| $\overline{\text{CS0}}$ high level width                                                | $t_{\text{WHCS}}$                  | $\overline{\text{CS0}}$  | Chip select transfer mode                                              | $t_{\text{sys}} + 200$  |                        | ns   |
| $\overline{\text{SCK0}}$ cycle time                                                     | $t_{\text{KCY}}$                   | $\overline{\text{SCK0}}$ | Input mode                                                             | $2t_{\text{sys}} + 200$ |                        | ns   |
|                                                                                         |                                    |                          | Output mode                                                            | $16000/f_c$             |                        | ns   |
| $\overline{\text{SCK0}}$<br>high and low level width                                    | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK0}}$ | Input mode                                                             | $t_{\text{sys}} + 100$  |                        | ns   |
|                                                                                         |                                    |                          | Output mode                                                            | $8000/f_c - 50$         |                        | ns   |
| SI0 input setup time<br>(against $\overline{\text{SCK0}} \uparrow$ )                    | $t_{\text{SIK}}$                   | SI0                      | $\overline{\text{SCK0}}$ input mode                                    | 100                     |                        | ns   |
|                                                                                         |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   | 200                     |                        | ns   |
| SI0 input hold time<br>(against $\overline{\text{SCK0}} \uparrow$ )                     | $t_{\text{KSI}}$                   | SI0                      | $\overline{\text{SCK0}}$ input mode                                    | $t_{\text{sys}} + 200$  |                        | ns   |
|                                                                                         |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   | 100                     |                        | ns   |
| $\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$<br>delay time                | $t_{\text{KSO}}$                   | SO0                      | $\overline{\text{SCK0}}$ input mode                                    |                         | $t_{\text{sys}} + 200$ | ns   |
|                                                                                         |                                    |                          | $\overline{\text{SCK0}}$ output mode                                   |                         | 100                    | ns   |

**Note 1)**  $t_{\text{sys}}$  is determined by the upper two bits of the clock control register (Address: 00FE<sub>H</sub>; CPU clock selected) resulting in one of the 3 following values:

$t_{\text{sys}}$  [ns] =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

**Note 2)** The load of  $\overline{\text{SCK0}}$  output mode and SO0 output delay time is 50pF + 1TTL.

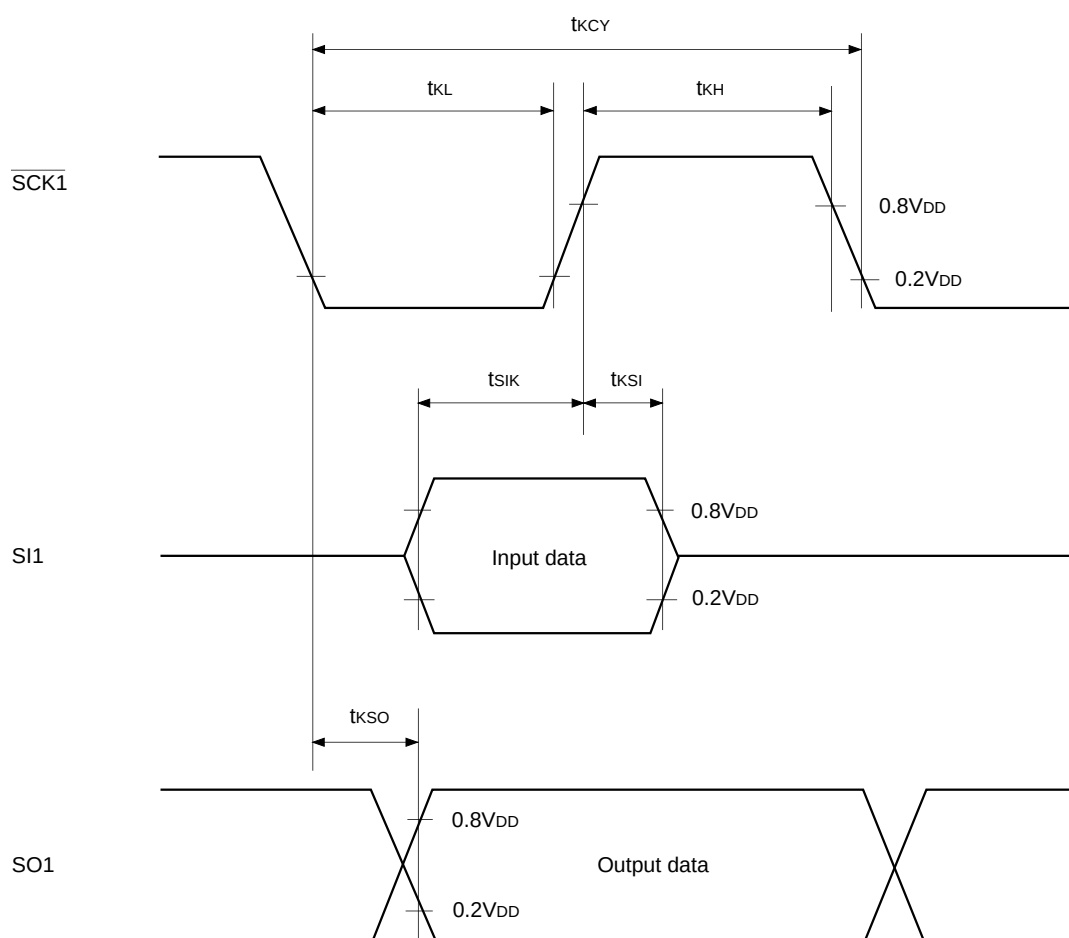
Fig. 4. Serial transfer CH0 timing



## Serial transfer (CH1)

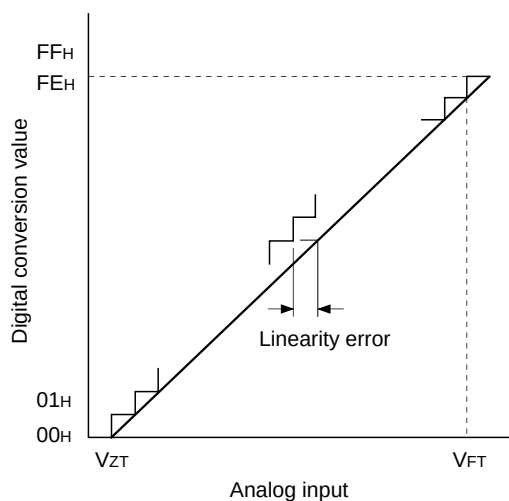
(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

| Item                                                      | Symbol                             | Pin                      | Condition                            | Min.         | Max. | Unit |
|-----------------------------------------------------------|------------------------------------|--------------------------|--------------------------------------|--------------|------|------|
| $\overline{\text{SCK1}}$ cycle time                       | $t_{\text{KCY}}$                   | $\overline{\text{SCK1}}$ | Input mode                           | 1000         |      | ns   |
|                                                           |                                    |                          | Output mode                          | 16000/fc     |      | ns   |
| $\overline{\text{SCK1}}$ high and low level width         | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK1}}$ | Input mode                           | 400          |      | ns   |
|                                                           |                                    |                          | Output mode                          | 8000/fc - 50 |      | ns   |
| SI1 input setup time (against $\overline{\text{SCK1}}$ ↑) | $t_{\text{SIK}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 100          |      | ns   |
|                                                           |                                    |                          | $\overline{\text{SCK1}}$ output mode | 200          |      | ns   |
| SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)  | $t_{\text{KSI}}$                   | SI1                      | $\overline{\text{SCK1}}$ input mode  | 200          |      | ns   |
|                                                           |                                    |                          | $\overline{\text{SCK1}}$ output mode | 100          |      | ns   |
| $\overline{\text{SCK1}}$ ↓ → SO1 delay time               | $t_{\text{KSO}}$                   | SO1                      | $\overline{\text{SCK1}}$ input mode  |              | 200  | ns   |
|                                                           |                                    |                          | $\overline{\text{SCK1}}$ output mode |              | 100  | ns   |

**Note)** The load of  $\overline{\text{SCK1}}$  output mode and SO1 output delay time is 50pF + 1TTL.**Fig. 5. Serial transfer CH1 timing**

**(3) A/D converter characteristics**(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

| Item                          | Symbol             | Pin        | Condition                                                                                   | Min.                    | Typ. | Max.            | Unit |
|-------------------------------|--------------------|------------|---------------------------------------------------------------------------------------------|-------------------------|------|-----------------|------|
| Resolution                    |                    |            |                                                                                             |                         |      | 8               | Bits |
| Linearity error               |                    |            | A/D converter operation only<br>Ta = 25°C<br>V <sub>DD</sub> = 5.0V<br>V <sub>SS</sub> = 0V |                         |      | ±3              | LSB  |
| Zero transition voltage       | V <sub>ZT</sub> *1 |            |                                                                                             | -10                     | 70   | 150             | mV   |
| Full-scale transition voltage | V <sub>FT</sub> *2 |            |                                                                                             | 4930                    | 5050 | 5120            | mV   |
| Conversion time               | t <sub>CONV</sub>  |            |                                                                                             | 160/f <sub>ADC</sub> *3 |      |                 | μs   |
| Sampling time                 | t <sub>SAMP</sub>  |            |                                                                                             | 12/f <sub>ADC</sub> *3  |      |                 | μs   |
| Analog input voltage          | V <sub>IAN</sub>   | AN0 to AN7 |                                                                                             | 0                       |      | V <sub>DD</sub> | V    |

**Fig. 6. Definition of A/D converter terms**\*1 V<sub>ZT</sub> : Digital Value converted between 00H to 01H.\*2 V<sub>FT</sub> : Digital Value converted between FEH to FFH.\*3 f<sub>ADC</sub> : ADC operation clock selection (MSC: Bit 0 of address 01FFH) and assumes following values:f<sub>ADC</sub> = f<sub>c</sub>/2 when PS2 is selected.f<sub>ADC</sub> = f<sub>c</sub> when PS1 is selected.

(4) Interrupts, reset inputs (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

| Item                                         | Symbol                             | Pin                          | Condition | Min. | Max. | Unit |
|----------------------------------------------|------------------------------------|------------------------------|-----------|------|------|------|
| External interrupt high and low level widths | t <sub>IH</sub><br>t <sub>IL</sub> | INT0<br>INT1<br>INT2<br>INT3 |           | 1    |      | μs   |
| Reset input low level width                  | t <sub>RSL</sub>                   | $\overline{\text{RST}}$      |           | 8/fc |      | μs   |

Fig. 7. Interrupt input timing

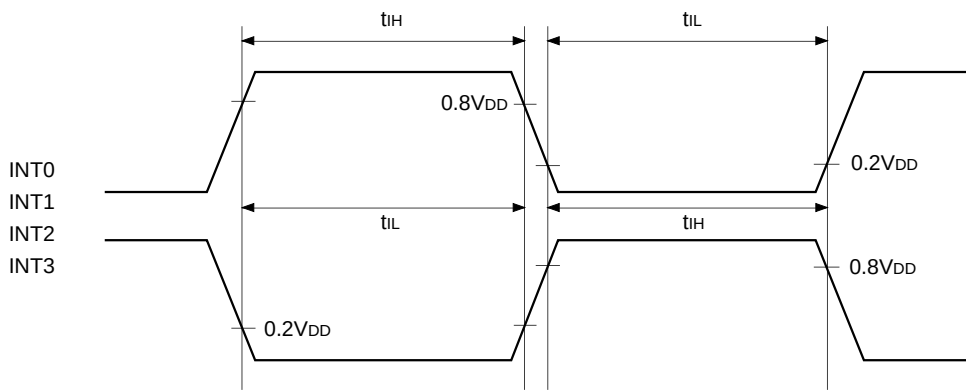
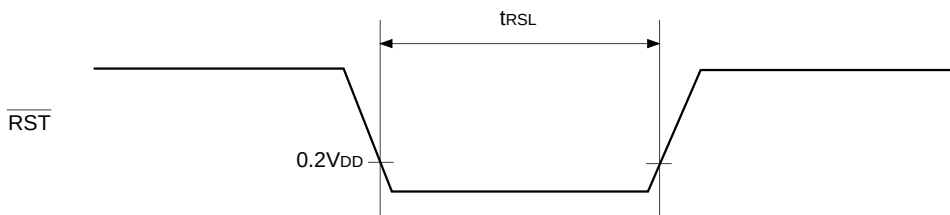


Fig. 8.  $\overline{\text{RST}}$  input timing



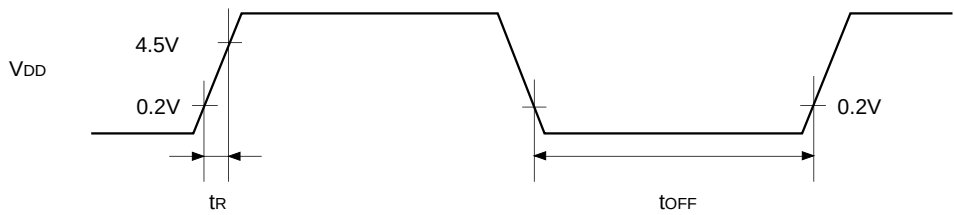
(5) Power-on reset

Power-on reset\* (Ta = -20 to +75°C, VDD = 4.5 to 5.0V, VSS = 0V)

| Item                      | Symbol           | Pin | Condition                 | Min. | Max. | Unit |
|---------------------------|------------------|-----|---------------------------|------|------|------|
| Power supply rising time  | t <sub>R</sub>   | VDD | Power-on reset            | 0.05 | 50   | ms   |
| Power supply cut-off time | t <sub>OFF</sub> |     | Repetitive power-on reset | 1    |      | ms   |

\* Specifies only when power-on reset function is selected.

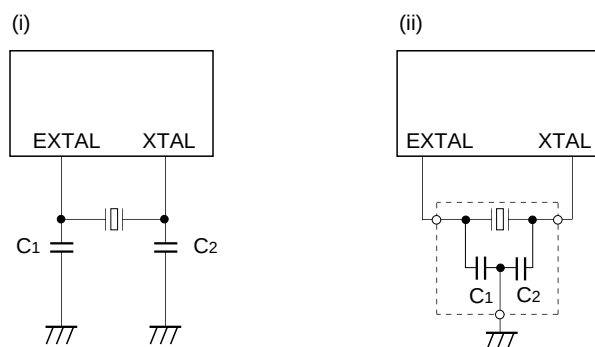
Fig. 9. Power-on reset



The power supply should be rise smoothly

## Supplement

Fig. 10. Recommended Oscillation Circuit

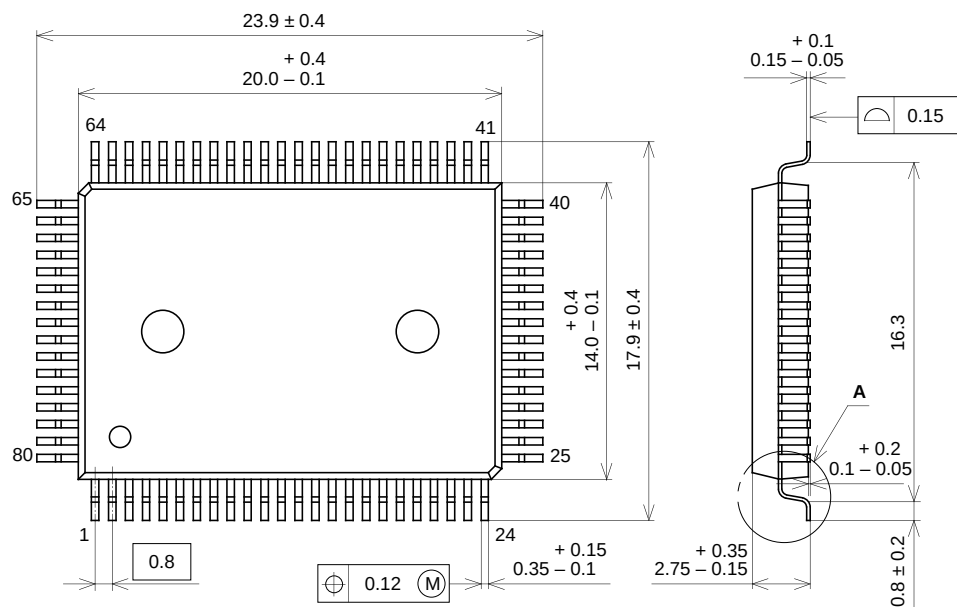
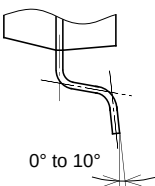


| Manufacturer         | Model        | fc (MHz) | C1 (pF) | C2 (pF) | Circuit Example |
|----------------------|--------------|----------|---------|---------|-----------------|
| MURATA MFG CO., LTD  | CSA4.19MG    | 4.19     | 30      | 30      | (i)             |
|                      | CSA8.00MG    | 8.00     |         |         |                 |
|                      | CSA10.0MT    | 10.00    |         |         |                 |
|                      | CST4.19MGW*  | 4.19     |         |         | (ii)            |
|                      | CST8.00MTW*  | 8.00     |         |         |                 |
|                      | CST10.00MTW* | 10.00    |         |         |                 |
| FUJI SANGYO CO., LTD | HC-49/U03    | 4.19     | 15      | 15      | (i)             |
|                      |              | 8.00     |         |         |                 |
|                      |              | 10.00    |         |         |                 |
| KINSEKI LTD.         | HC-49/U (-S) | 4.19     | 27      | 27      |                 |
|                      |              | 8.00     |         |         |                 |
|                      |              | 10.00    |         |         |                 |

\* Indicates types with on-chip grounding capacitors (C1 and C2).

Package Outline      Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

|            |               |                  |                 |
|------------|---------------|------------------|-----------------|
| SONY CODE  | QFP-80P-L01   | PACKAGE MATERIAL | EPOXY RESIN     |
| EIAJ CODE  | QFP080-P-1420 | LEAD TREATMENT   | SOLDER PLATING  |
| JEDEC CODE |               | LEAD MATERIAL    | 42/COPPER ALLOY |
|            |               | PACKAGE MASS     | 1.6g            |