Wideband, Low Noise Amplifier, Single Positive Supply, 0.01 GHz to 26.5 GHz

Data Sheet **ADL9005**

FEATURES

Single positive supply
Low noise figure: 2.5 dB typical from 0.01 GHz to 14 GHz
High gain: 17.5 dB typical from 0.01 GHz to 14 GHz
OP1dB: 13.5 dBm typical from 0.01 GHz to 20 GHz
High OIP3: 26 dBm typical from 0.01 GHz to 14 GHz
RoHS-compliant, 4 mm × 4 mm, 24-lead LFCSP

APPLICATIONS

Test instrumentation
Military
Communications

FUNCTIONAL BLOCK DIAGRAM

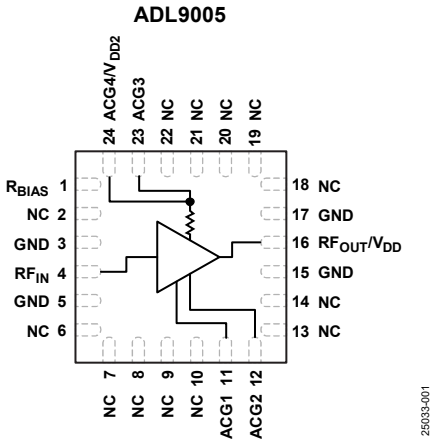


Figure 1.

GENERAL DESCRIPTION

The ADL9005 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), wideband, LNA that operates from 0.01 to 26.5 GHz. The ADL9005 provides a typical gain of 17.5 dB from 0.01 GHz to 14 GHz with a positive gain slope from 14 GHz to 20 GHz, a 13.5 dBm typical output power at 1 dB compression (OP1dB) from 0.01 GHz to 20 GHz, a 2.5 dB typical noise figure from 0.01 GHz to 14 GHz, and a typical output third-order intercept (OIP3) of 26 dBm from 0.01 GHz to 14 GHz, requiring only 80 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) of up to 16 dBm enables the LNA to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, inphase/quadrature (I/Q) or image rejection mixers. The ADL9005 also features inputs and outputs (I/Os) that are internally matched to 50 Ω, making it ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

The ADL9005 is housed in a RoHS-compliant, 4 mm × 4 mm, LFCSP.

Multifunction pin names may be referenced by their relevant function only.

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REVISION HISTORY

2/2021—Revision 0: Initial Version

SPECIFICATIONS

0.01 GHz TO 14 GHz

Drain voltage (V_{DD}) = 5 V, bias voltage (V_{BIAS}) = 5 V, total current (I_{DQ}) = 80 mA, R_{BIAS} = 300 Ω, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.01		14	GHz	
GAIN	15.5	17.5		dB	
Gain Variation Over Temperature		0.0077		dB/°C	
RETURN LOSS					
Input		15		dB	
Output		14		dB	
OUTPUT					
OP1dB	11.5	13.5		dBm	
P_{SAT}		16		dBm	
OIP3		26		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
NOISE FIGURE		2.5		dB	

14 GHz TO 20 GHz

V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	14		20	GHz	
GAIN	16.5	18.5		dB	
Gain Variation Over Temperature		0.0127		dB/°C	
RETURN LOSS					
Input		15		dB	
Output		14		dB	
OUTPUT					
OP1dB	11	13.5		dBm	
P_{SAT}		15		dBm	
OIP3		25		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
NOISE FIGURE		3		dB	

20 GHz TO 26.5 GHz

V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω, and T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	20		26.5	GHz	
GAIN	17	19		dB	
Gain Variation Over Temperature		0.0214		dB/°C	
RETURN LOSS					
Input		15		dB	
Output		14		dB	
OUTPUT					
OP1dB	8.5	11.5		dBm	
P_{SAT}		14		dBm	
OIP3		22		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
NOISE FIGURE		4		dB	

DC SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit
V_{DD}	3	5	6	V
CURRENT				
I_{DQ}		80		mA
Amplifier (I_{DQ_AMP})		73.6		mA
R_{BIAS} (I_{DQ_BIAS})		6.4		mA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{DD}	7 V
RF_{IN} Power	22 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 12.5 mW/°C Above 85°C)	1.125 W
Temperature	
Peak Reflow, Moisture Sensitivity Level (MSL)[1]	260°C
Junction to Maintain 1,000,000 Hour Meant Time to Failure (MTTF)	175°C
Nominal Junction (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 80 mA)	117°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C

[1] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package	θ_{JC}	Unit
CP-24-15	80	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL9005

Table 7. ADL9005, 24-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

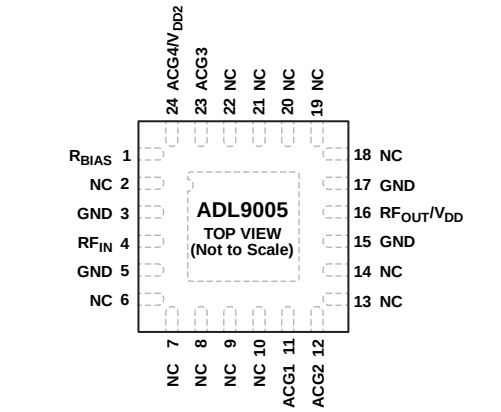


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{BIAS}	Current Mirror Bias Resistor Pin. Use the R_{BIAS} pin to set the I_{DQ} by connecting an external bias resistor as defined in Table 9. Refer to Figure 74 for the bias resistor connection. See Figure 3 for the interface schematic.
2, 6 to 10, 13, 14, 18 to 22	NC	No Internal Connection. Note the data shown herein was measured with these pins externally connected to the RF and dc ground.
3, 5, 15, 17	GND	Ground. The GND pins must be connected to RF and dc ground. See Figure 4 for the interface schematic.
4	RF_{IN}	RF Input. The RF_{IN} pin is dc-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
11	ACG1	AC Grounding 1. A capacitor is required on the ACG1 pin to provide low frequency decoupling. Refer to Figure 74 for the capacitor value. See Figure 5 for the interface schematic.
12	ACG2	AC Grounding 2. A capacitor is required on the ACG2 pin to provide low frequency decoupling. Refer to Figure 74 for the capacitor value. See Figure 5 for the interface schematic.
16	RF_{OUT}/V_{DD}	RF Output (RF_{OUT})/Drain Voltage for Amplifier (V_{DD}). The RF_{OUT}/V_{DD} pin is dc-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
23	ACG3	AC Grounding 3. A capacitor is required on the ACG3 pin to provide low frequency decoupling. Refer to Figure 74 for the capacitor value. See Figure 6 for the interface schematic.
24	$ACG4/V_{DD2}$	AC Grounding 4 (ACG4). A capacitor is required on the ACG4 pin to provide low frequency decoupling. Refer to Figure 74 for the capacitor value. See Figure 6 for the interface schematic. Optional Drain Voltage for the Amplifier that Requires a Higher Voltage (V_{DD2}). Do not use the V_{DD2} pin simultaneously with RF_{OUT}/V_{DD}. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

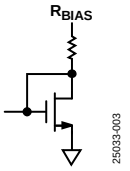


Figure 3. R_{BIAS} Interface Schematic



Figure 4. GND Interface Schematic

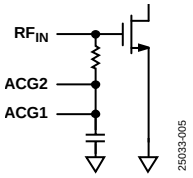


Figure 5. RF_{IN}, ACG1, and ACG2 Interface Schematic

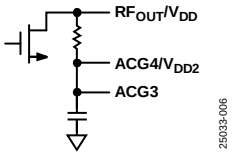


Figure 6. RF_{OUT}/V_{DD}, ACG3, and $ACG4/V_{DD2}$ Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

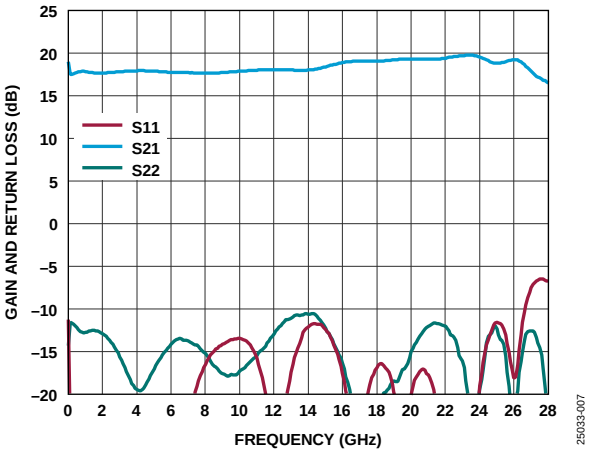


Figure 7. Gain and Return Loss vs. Frequency, 0.01 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω (S22 Is the Output Return Loss, S11 Is the Input Return Loss, and S21 Is the Gain)

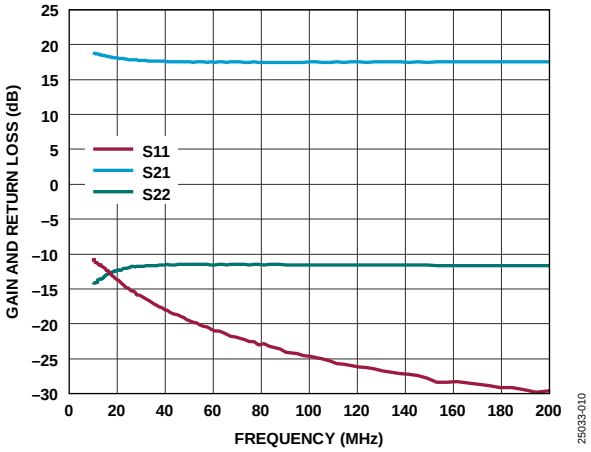


Figure 10. Gain and Return Loss vs. Frequency, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

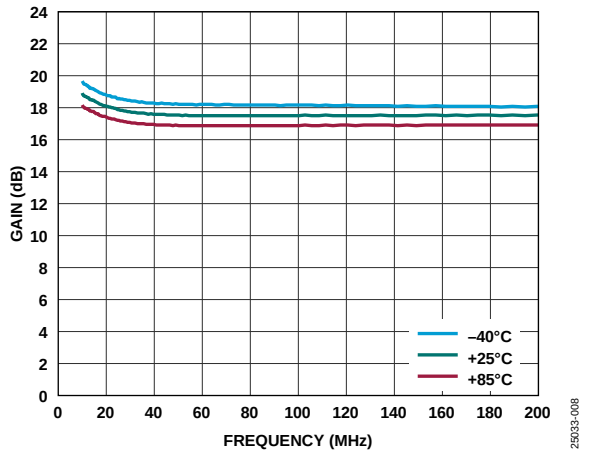


Figure 8. Gain vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

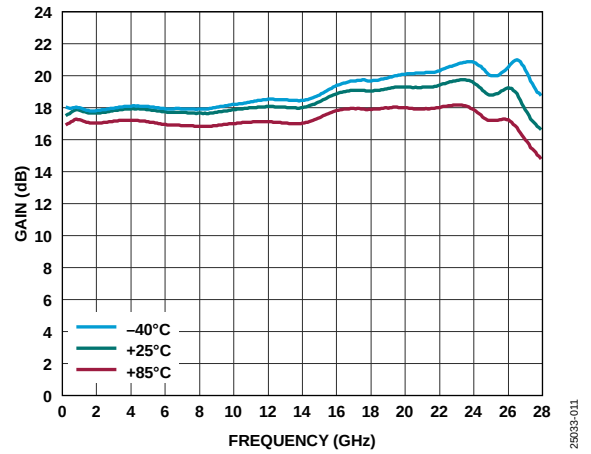


Figure 11. Gain vs. Frequency for Various Temperatures, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

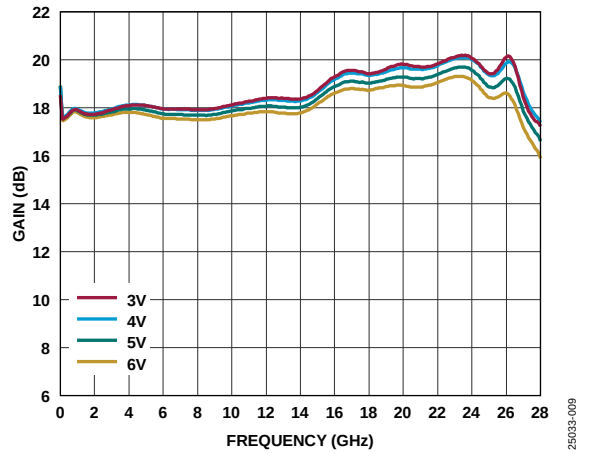


Figure 9. Gain vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 28 GHz

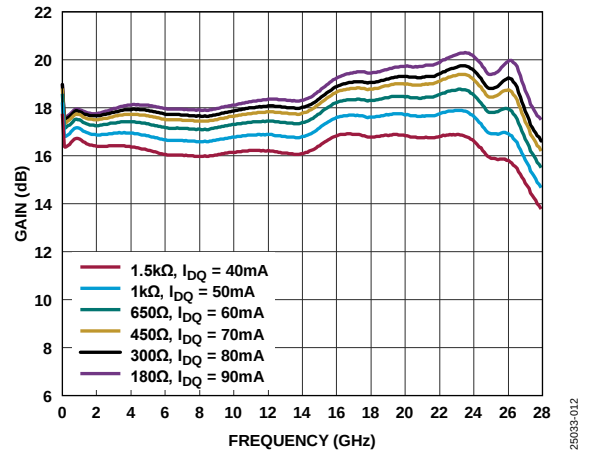


Figure 12. Gain vs. Frequency for Various Bias Resistor Values and I_{DQ}, 10 MHz to 28 GHz, V_{DD} = 5 V

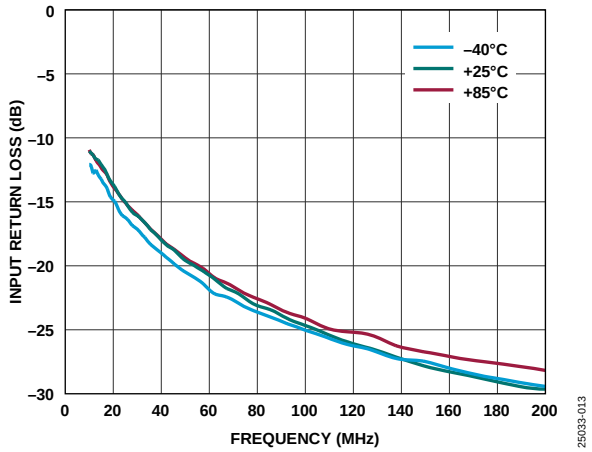


Figure 13. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

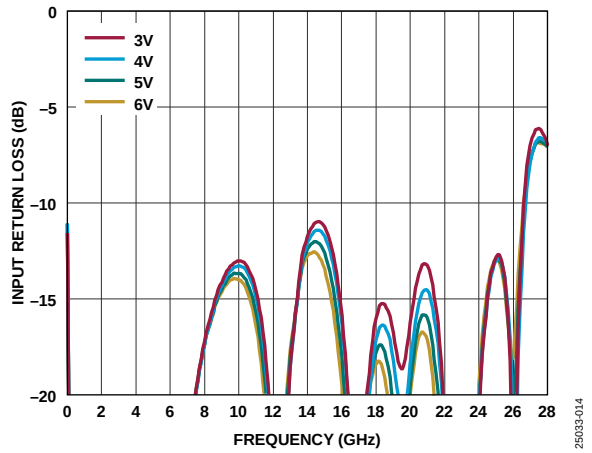


Figure 14. Input Return Loss vs Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 28 GHz

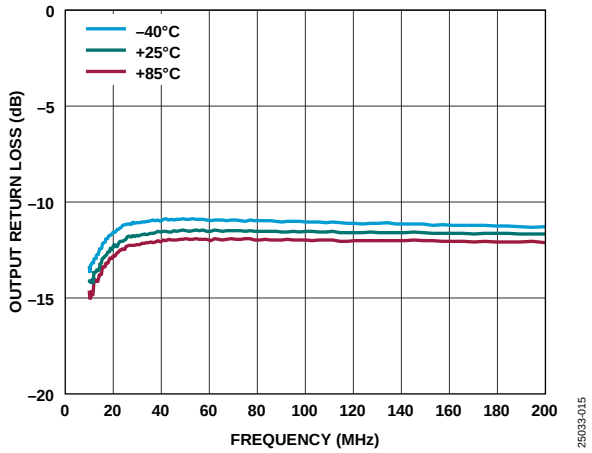


Figure 15. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

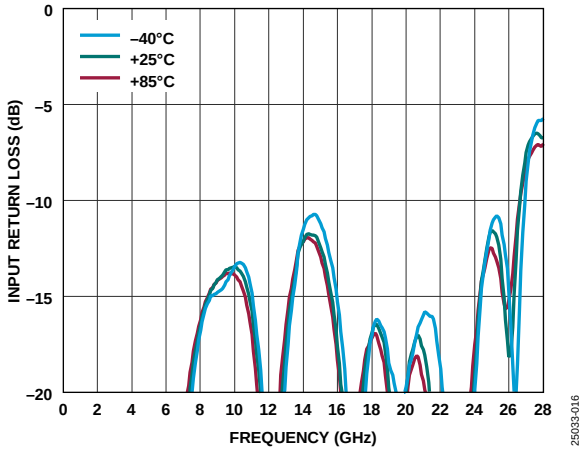


Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

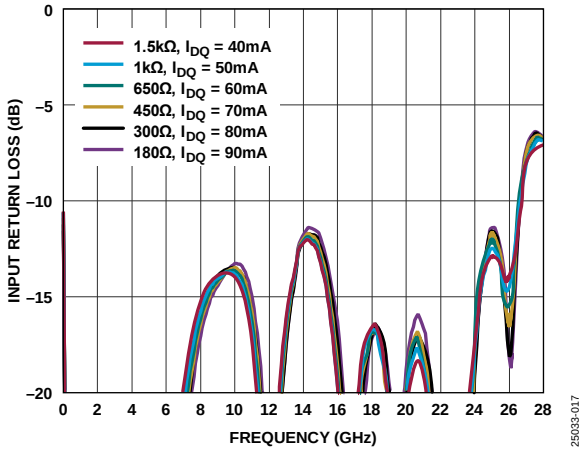


Figure 17. Input Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 28 GHz, V_{DD} = 5 V

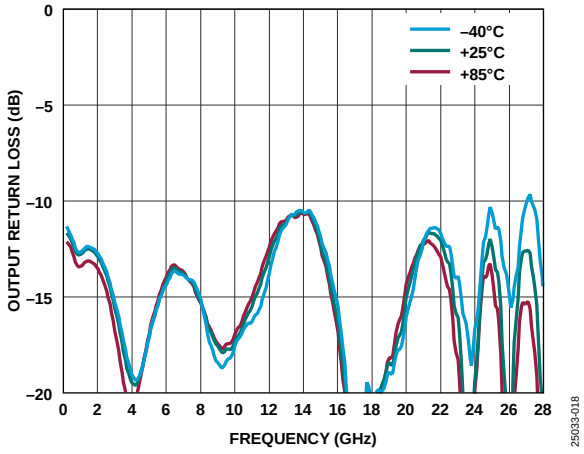


Figure 18. Output Return Loss vs. Frequency for Various Temperatures, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

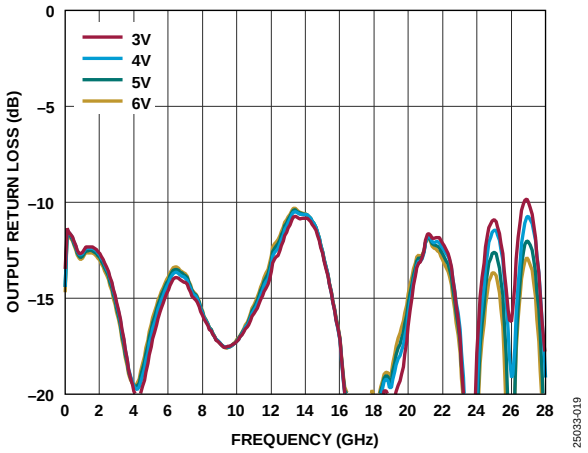


Figure 19. Output Return Loss vs. Frequency at Various V_{DD}, I_{DQ} = 80mA, 0.01 GHz to 28 GHz

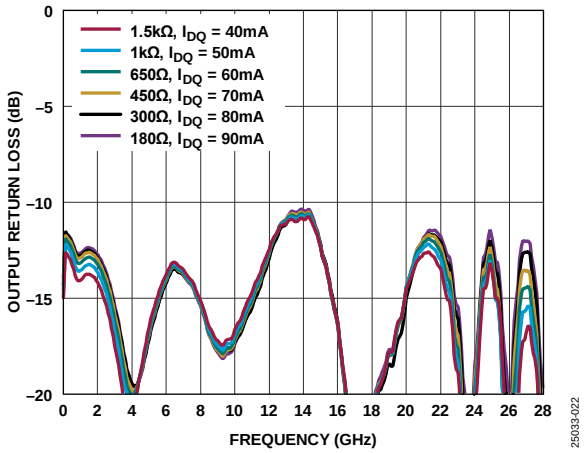


Figure 22. Output Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 28 GHz, V_{DD} = 5 V

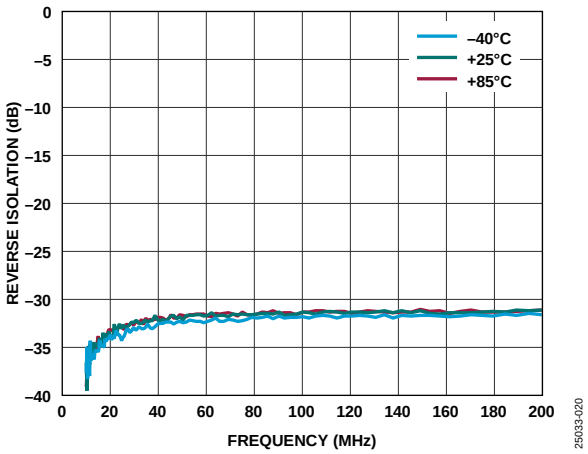


Figure 20. Reverse Isolation (S12) vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

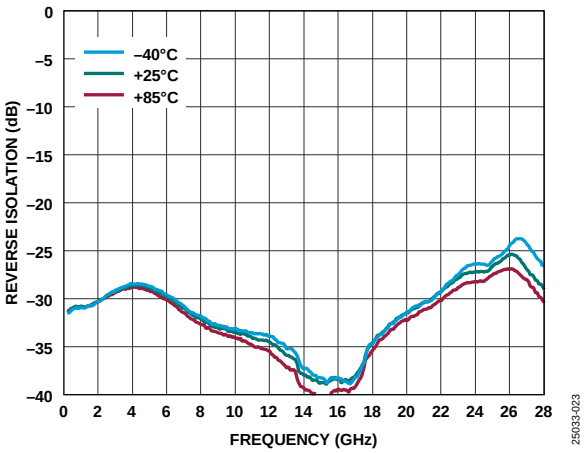


Figure 23. Reverse Isolation vs. Frequency for Various Temperatures, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

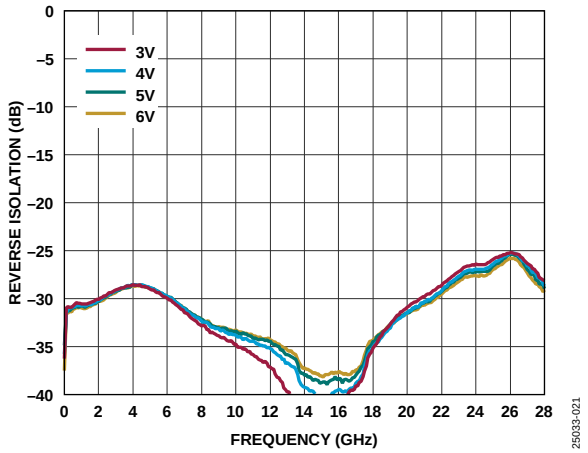


Figure 21. Reverse Isolation vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 28 GHz

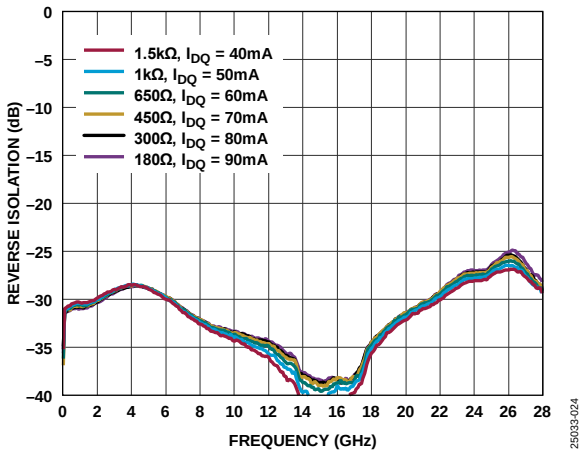


Figure 24. Reverse Isolation vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 28 GHz, V_{DD} = 5 V

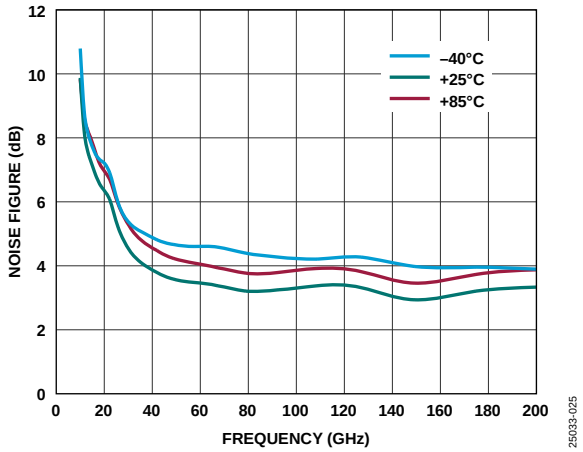


Figure 25. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

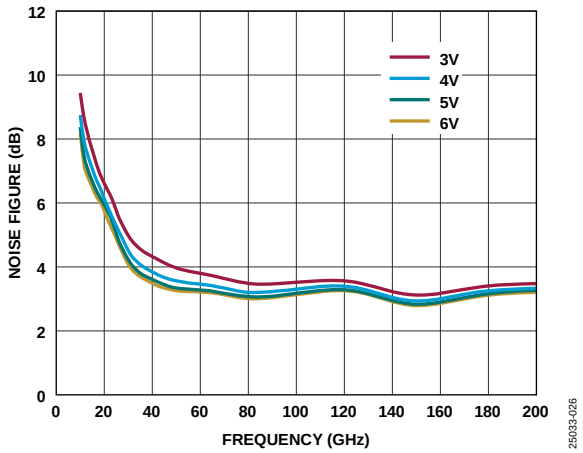


Figure 26. Noise Figure vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 10 MHz to 200 MHz

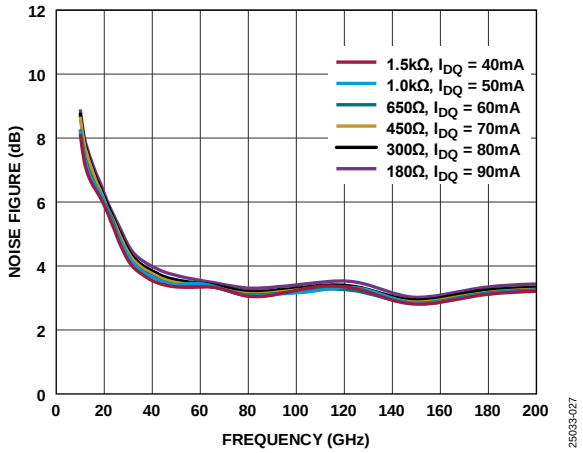


Figure 27. Noise Figure vs. Frequency for Various Bias Resistor Values and I_{DQ}, 10 MHz to 200 MHz, V_{DD} = 5 V, V_{BIAS} = 5 V

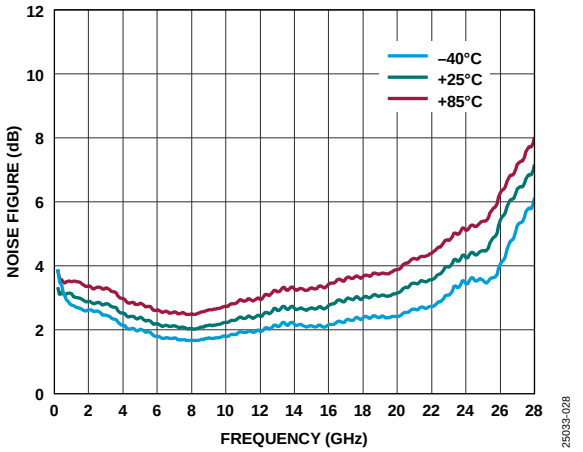


Figure 28. Noise Figure vs. Frequency for Various Temperatures, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

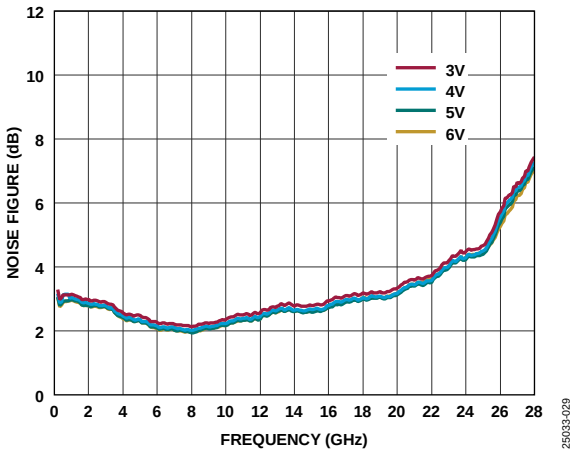


Figure 29. Noise Figure vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.2 GHz to 28 GHz

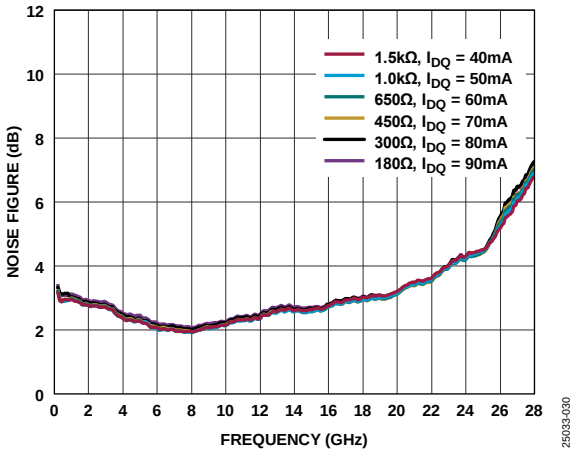


Figure 30. Noise Figure vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.2 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

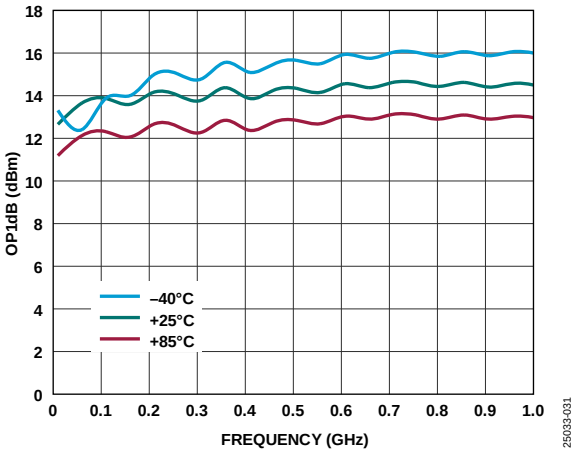


Figure 31. OP1dB vs. Frequency for Various Temperatures, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

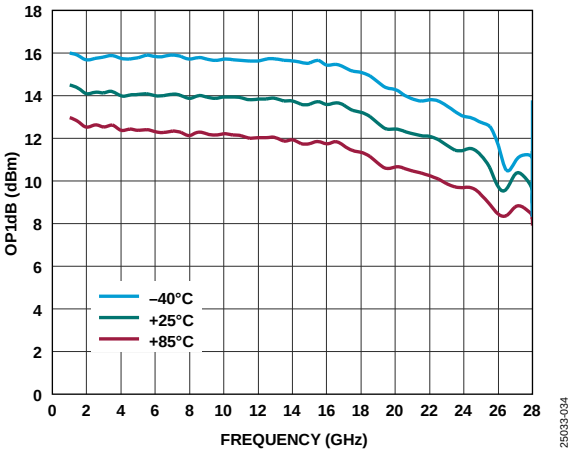


Figure 34. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

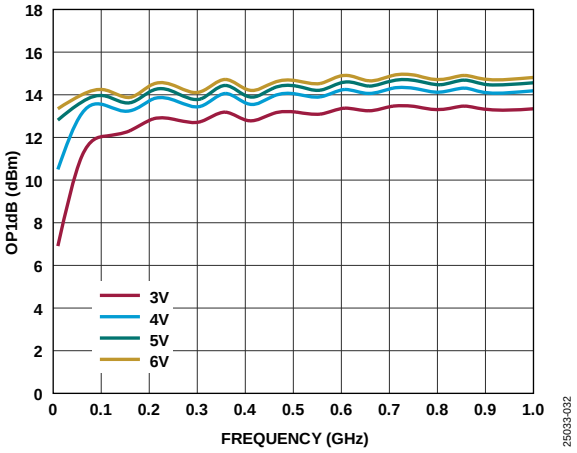


Figure 32. OP1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 80 mA, 0.01 GHz to 1 GHz

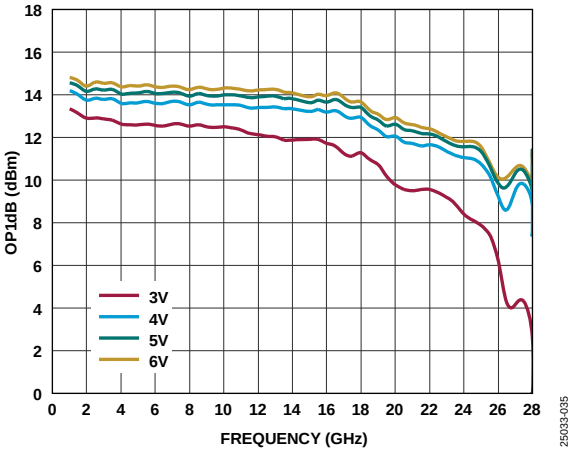


Figure 35. OP1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 80 mA, 1 GHz to 28 GHz

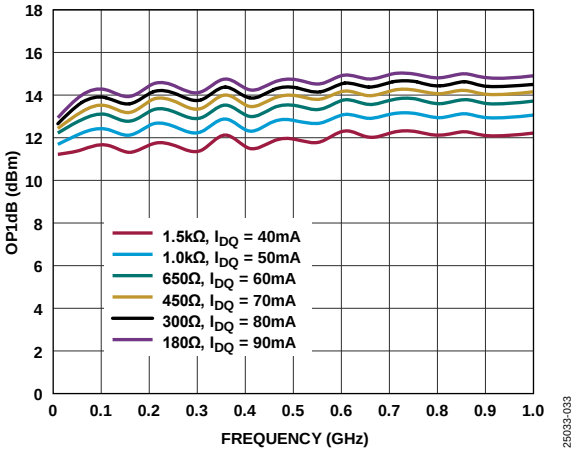


Figure 33. OP1dB vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

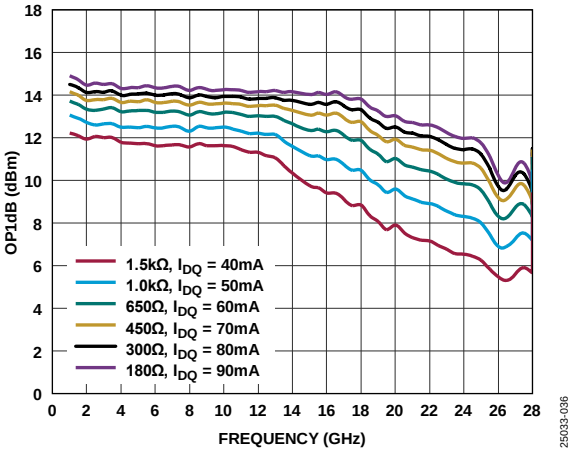


Figure 36. OP1dB vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

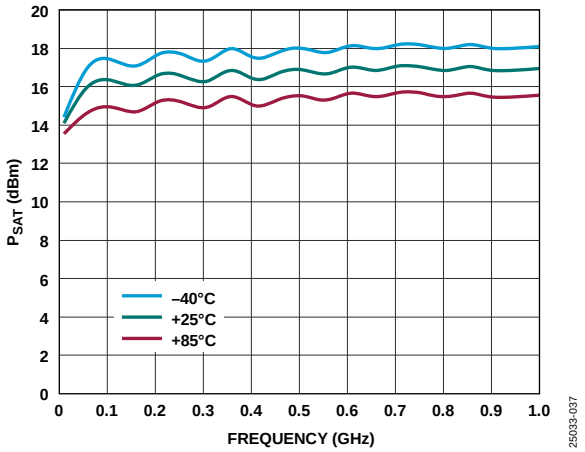


Figure 37. P_{SAT} vs. Frequency for Various Temperatures, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

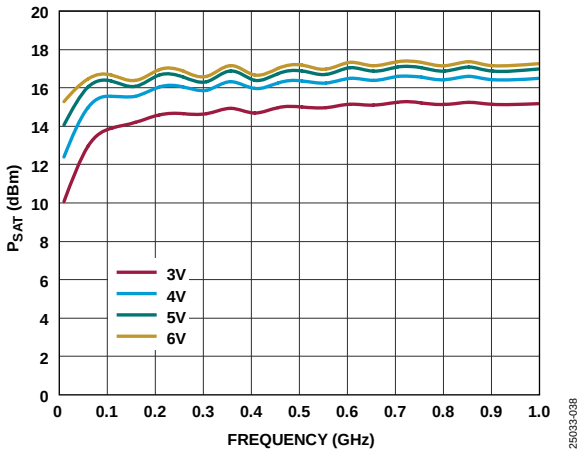


Figure 38. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 1 GHz

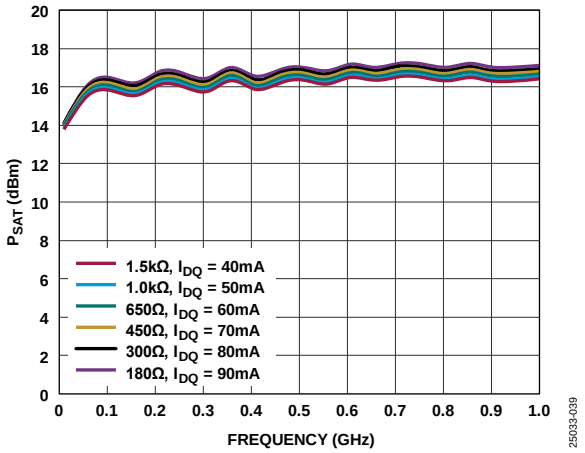


Figure 39. P_{SAT} vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

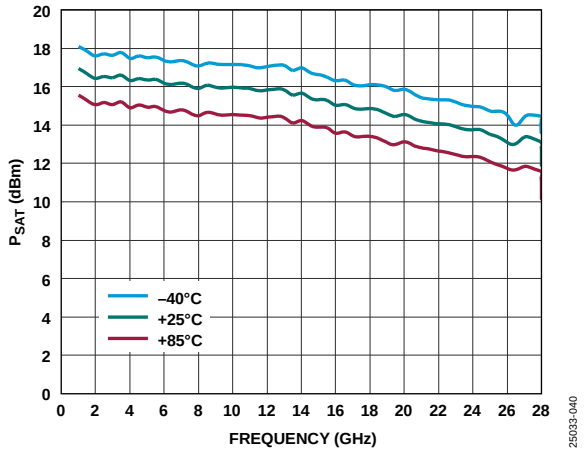


Figure 40. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

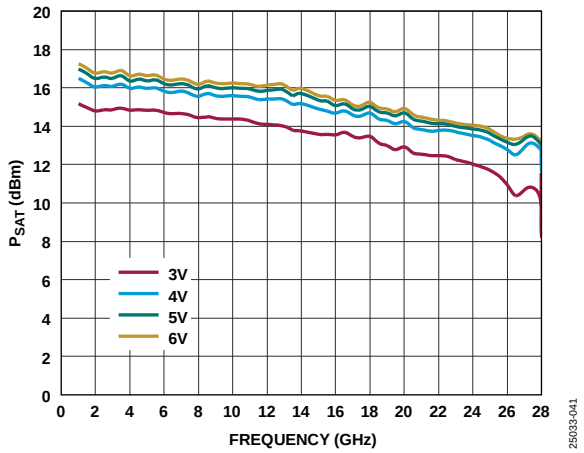


Figure 41. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 1 GHz to 28 GHz

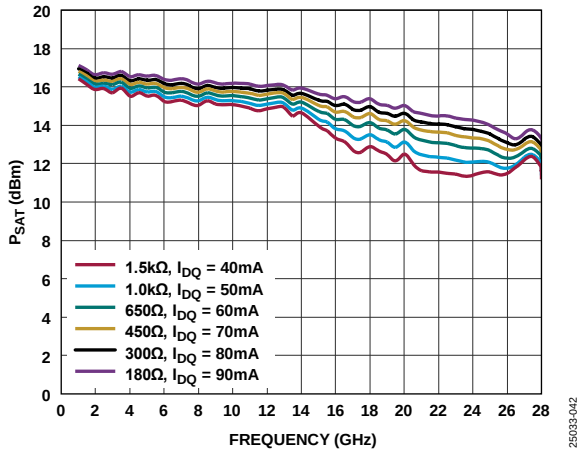


Figure 42. P_{SAT} vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

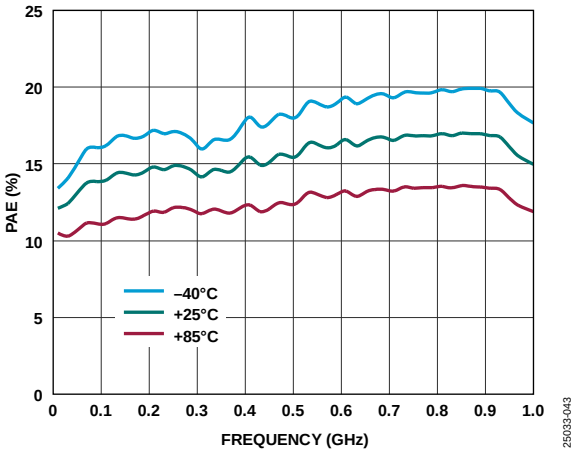


Figure 43. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

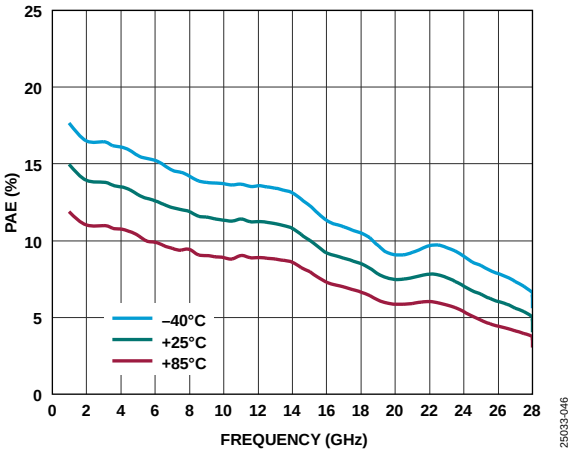


Figure 46. PAE vs. Frequency for Various Temperatures, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

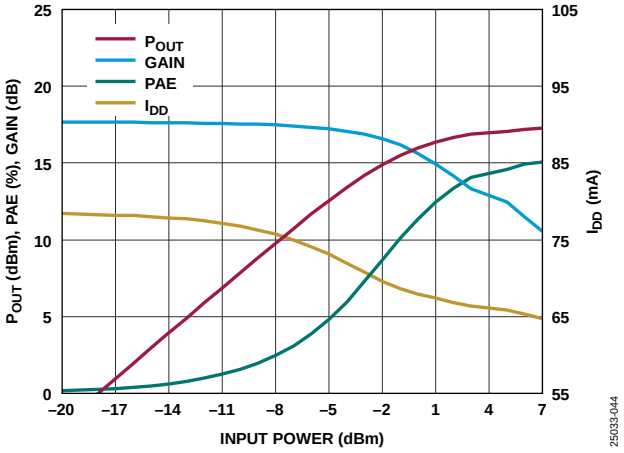


Figure 44. P_{OUT}, PAE, Gain, and Drain Current (I_{DD}) vs. Input Power, Power Compression at 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

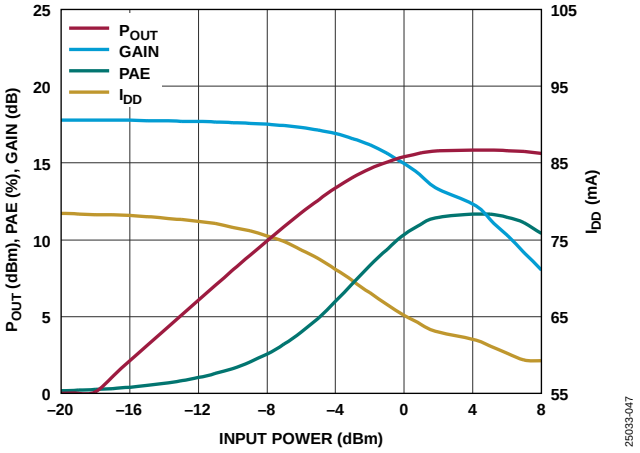


Figure 47. P_{OUT}, PAE, Gain, and I_{DD} vs. Input Power, Power Compression at 10 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

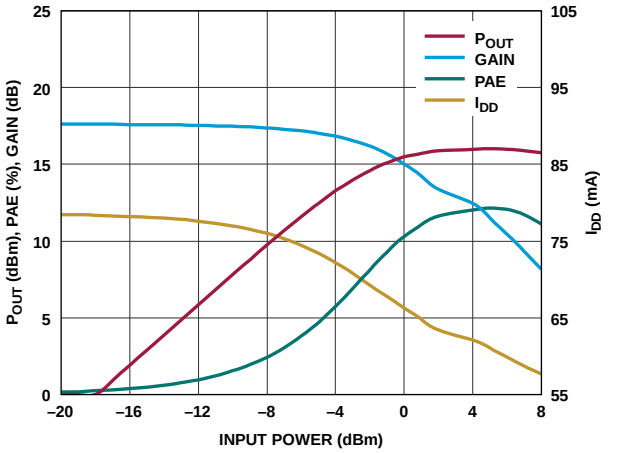


Figure 45. P_{OUT}, PAE, Gain, and I_{DD} vs. Input Power, Power Compression at 8 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

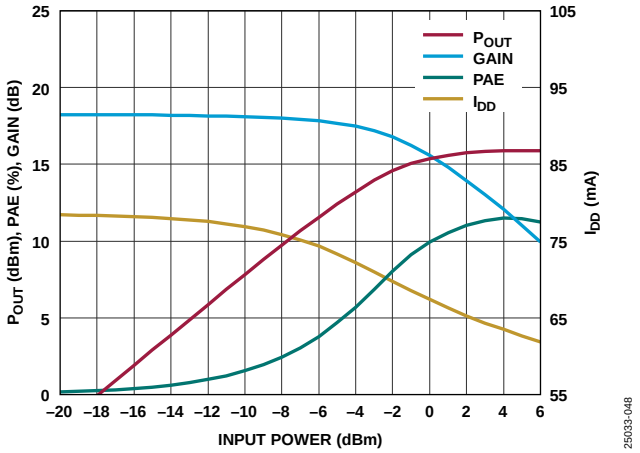


Figure 48. P_{OUT}, PAE, Gain, and I_{DD} vs. Input Power, Power Compression at 14 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

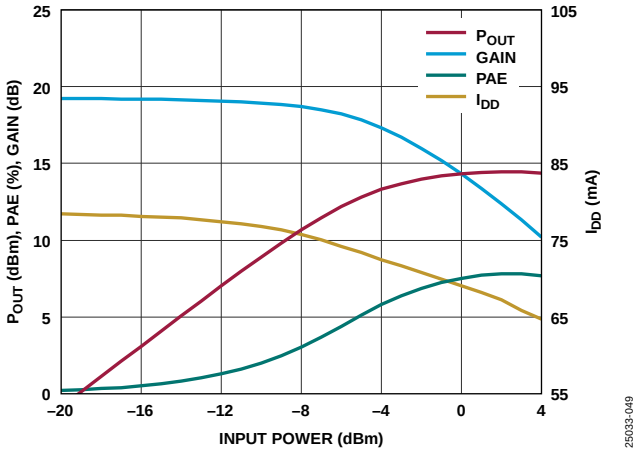


Figure 49. P_{OUT}, PAE, Gain, and I_{DD} vs. Input Power, Power Compression at 20 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

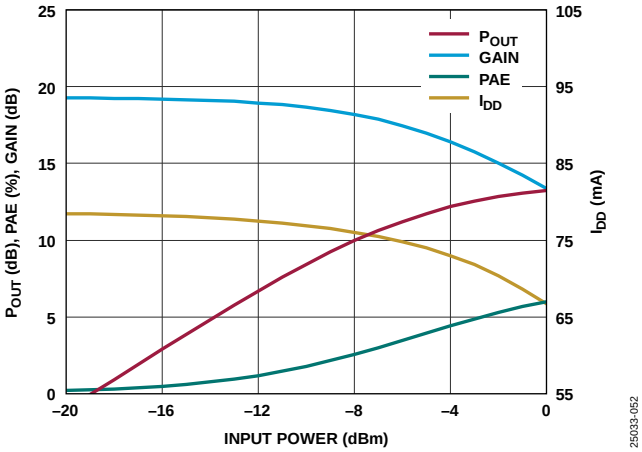


Figure 52. P_{OUT}, PAE, Gain, and I_{DD} vs. Input Power, Power Compression at 26 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

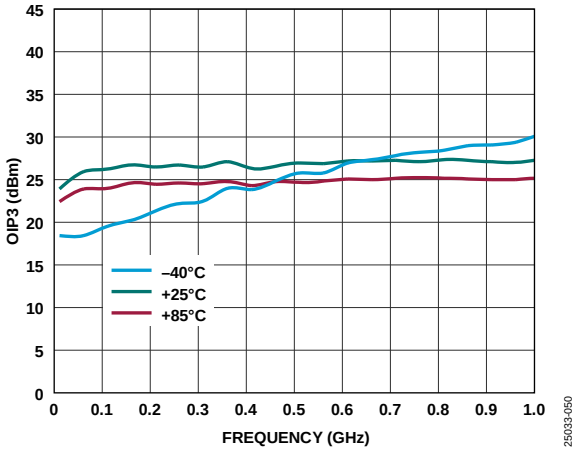


Figure 50. OIP3 vs. Frequency for Various Temperatures, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

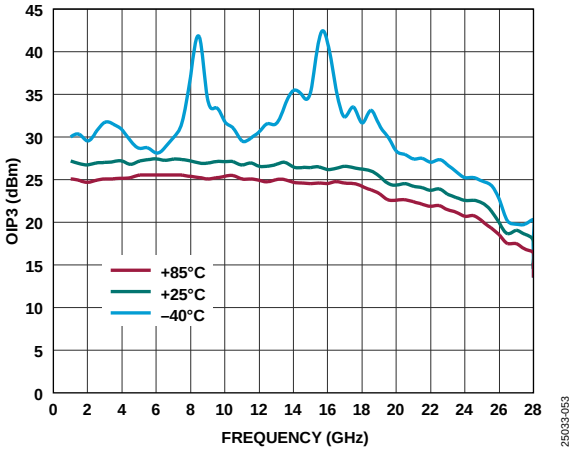


Figure 53. OIP3 vs. Frequency for Various Temperatures, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

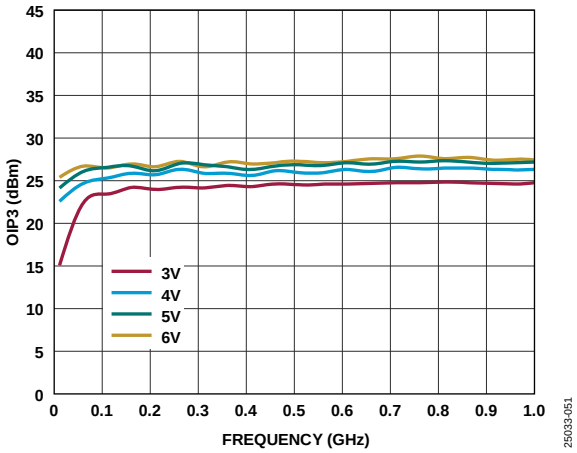


Figure 51. OIP3 vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 1 GHz

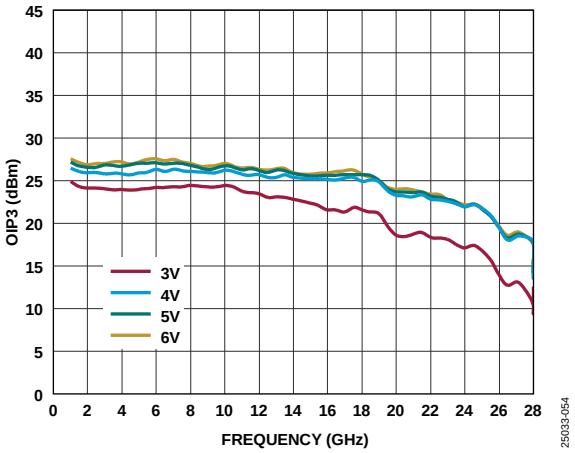


Figure 54. OIP3 vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 1 GHz to 28 GHz

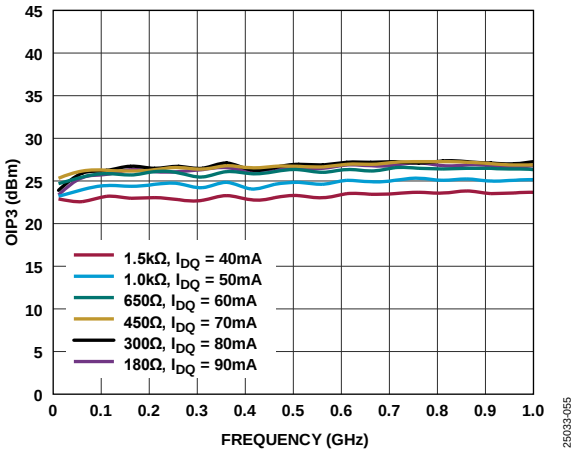


Figure 55. OIP3 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

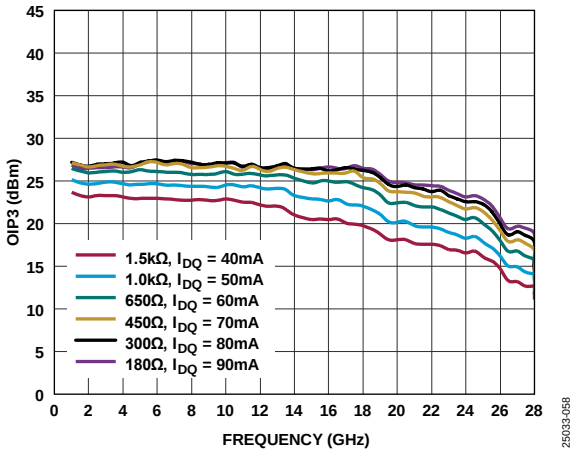


Figure 58. OIP3 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 28 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

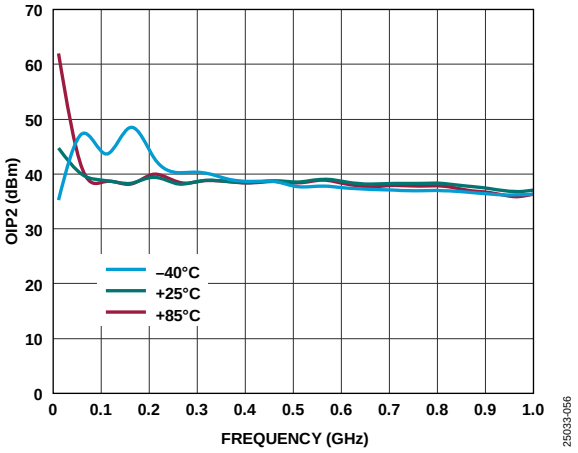


Figure 56. OIP2 vs. Frequency for Various Temperatures, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

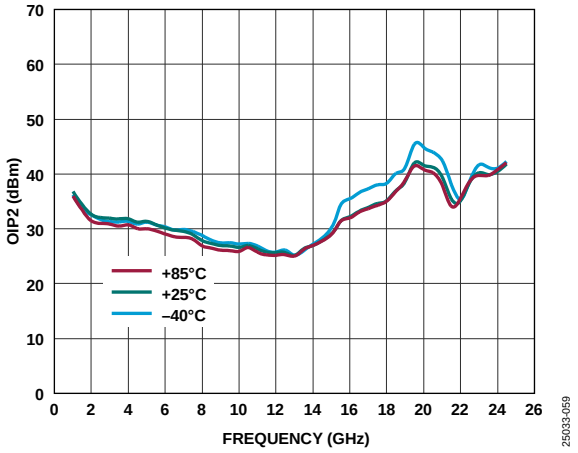


Figure 59. OIP2 vs. Frequency for Various Temperatures, 1 GHz to 24.5 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω

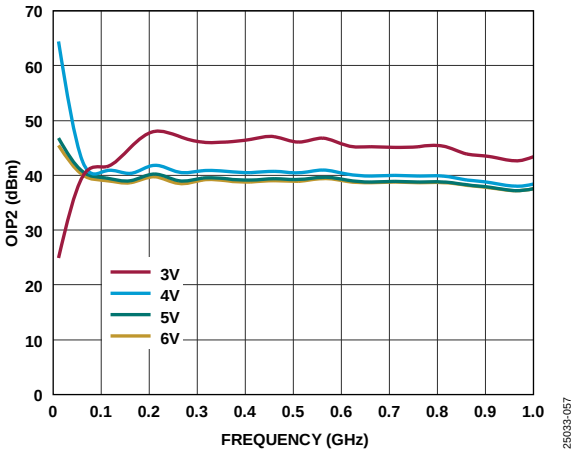


Figure 57. OIP2 vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 0.01 GHz to 1 GHz

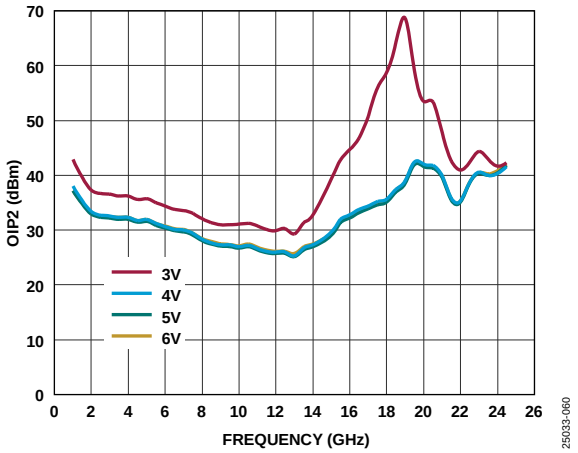


Figure 60. OIP2 vs. Frequency for Various V_{DD}, I_{DQ} = 80 mA, 1 GHz to 24.5 GHz

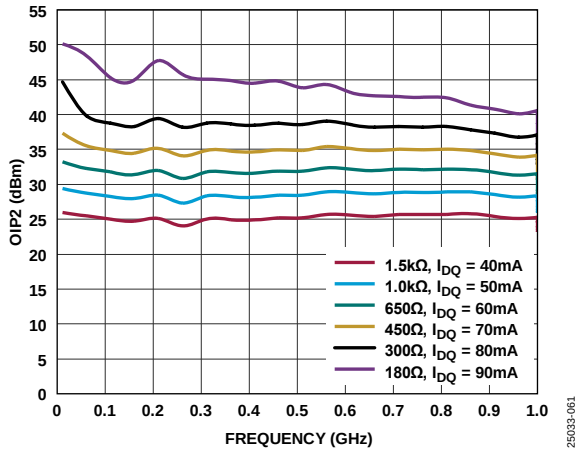


Figure 61. OIP2 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 0.01 GHz to 1 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

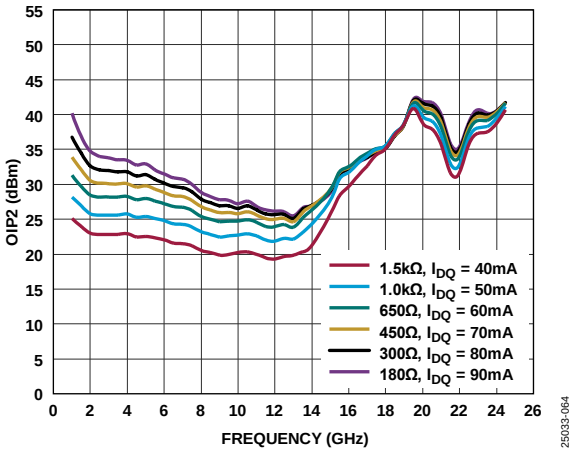


Figure 64. OIP2 vs. Frequency for Various Bias Resistor Values and I_{DQ}, 1 GHz to 24.5 GHz, V_{DD} = 5 V, V_{BIAS} = 5 V

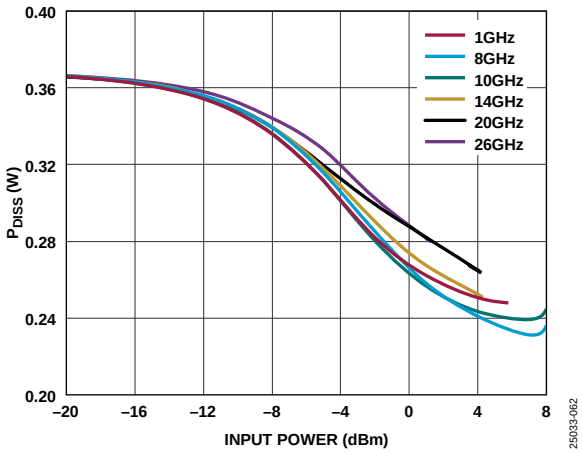


Figure 62. P_{DISS} vs. Input Power at Various Frequencies, T_A = 85°C, V_{DD} = 5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA

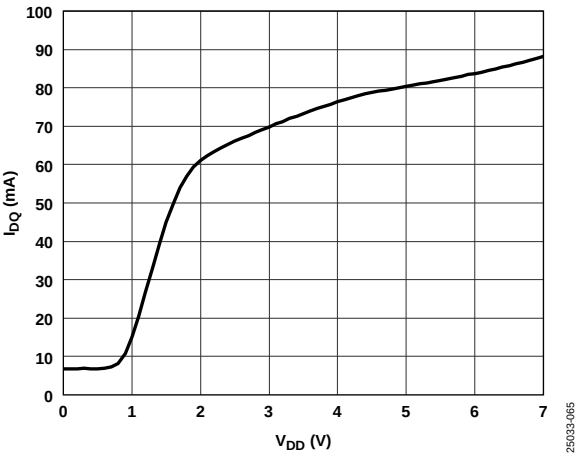


Figure 65. I_{DQ} vs. V_{DD}, V_{BIAS} = 5 V, R_{BIAS} = 300 Ω

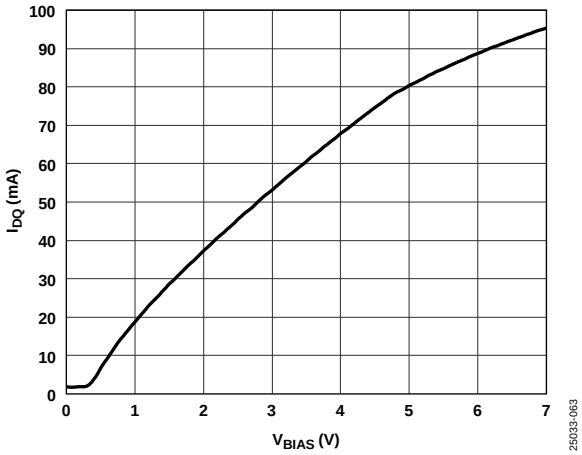


Figure 63. I_{DQ} vs. V_{BIAS}, V_{DD} = 5 V, R_{BIAS} = 300 Ω

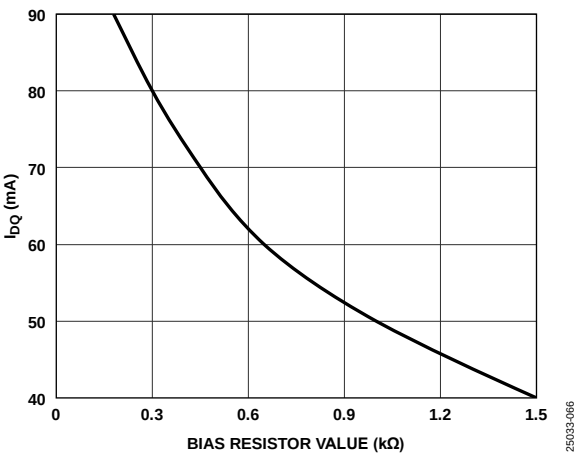


Figure 66. I_{DQ} vs. Bias Resistor Value, V_{BIAS} = 5 V, V_{DD} = 5 V

BIASING THROUGH THE ACG4/V_{DD2} PIN

V_{DD2} = 8.5 V, V_{BIAS} = 5 V, I_{DQ} = 80 mA, R_{BIAS} = 300 Ω, and frequency range = 0.01 GHz to 28 GHz.

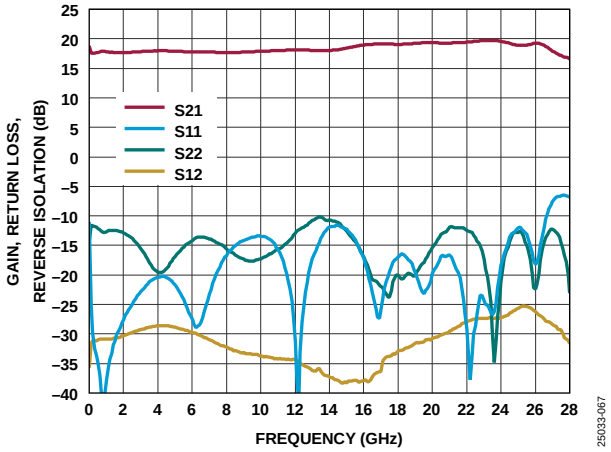


Figure 67. Gain, Return Loss, and Reverse Isolation vs. Frequency

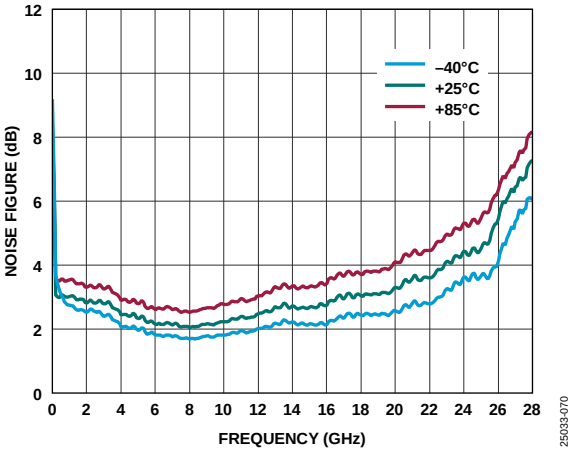


Figure 70. Noise Figure vs. Frequency for Various Temperatures

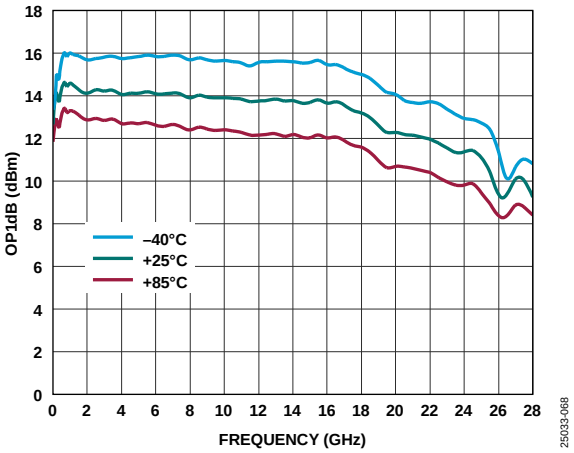


Figure 68. OP1dB vs. Frequency for Various Temperatures

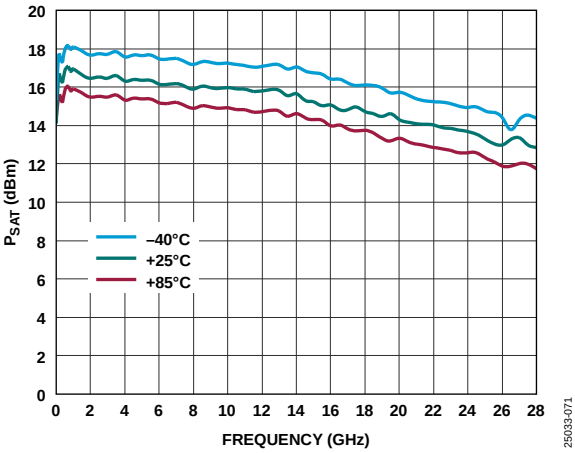


Figure 71. P_{SAT} vs. Frequency for Various Temperatures

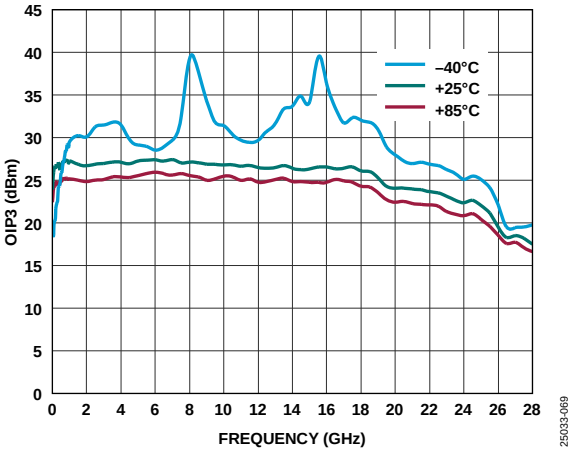


Figure 69. OIP3 vs. Frequency for Various Temperatures

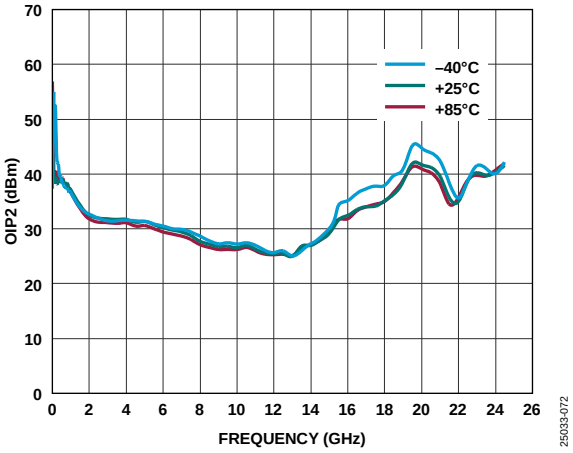


Figure 72. OIP2 vs. Frequency for Various Temperatures

THEORY OF OPERATION

The ADL9005 is a GaAs, MMIC, pHEMT, wideband LNA. A simplified block diagram is shown in Figure 73. The RF_{IN} and RF_{OUT} pins are dc-coupled and matched to 50 Ω.

The ADL9005 operates from a single positive supply. I_{DQ} is set by connecting a resistor between the R_{BIAS} pin and the external supply voltage. The drain bias voltage is normally provided via an external bias tee. However, the drain bias voltage can also be resistively biased by connecting the ACG4/V_{DD2} pin to an external supply.

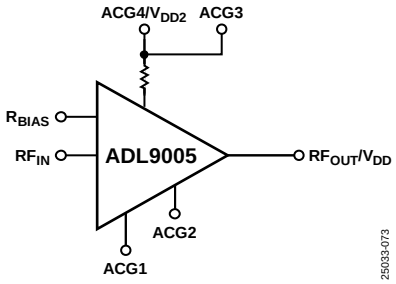


Figure 73. Simplified Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADL9005 are shown in Figure 74. Connect the recommended capacitor values to the ac ground pins (ACG1, ACG2, ACG3, and ACG4) as shown in Figure 74. The bias current is set by connecting a resistor between R_{BIAS} and V_{DD}. When using 5 V V_{DD}, a resistor value of 300 Ω is recommended to achieve an I_{DQ} of 80 mA. Table 9 shows the resulting I_{DQ} for the various R_{BIAS} values where the resistor is tied to 5 V. Decouple the R_{BIAS} pin with a 100 pF capacitor as shown in Figure 74.

Refer to ADL9005-EVALZ user guide (UG-1859) for the recommended part numbers of the manufacturers for all the external components required to operate the ADL9005.

Table 9. Recommended Bias Resistor Values

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{DQ_BIAS} (mA)
180	90	82.3	7.7
300	80	73.6	6.4
450	70	64.8	5.2
650	60	55.8	4.2
1000	50	46.8	3.2
1500	40	37.4	2.6

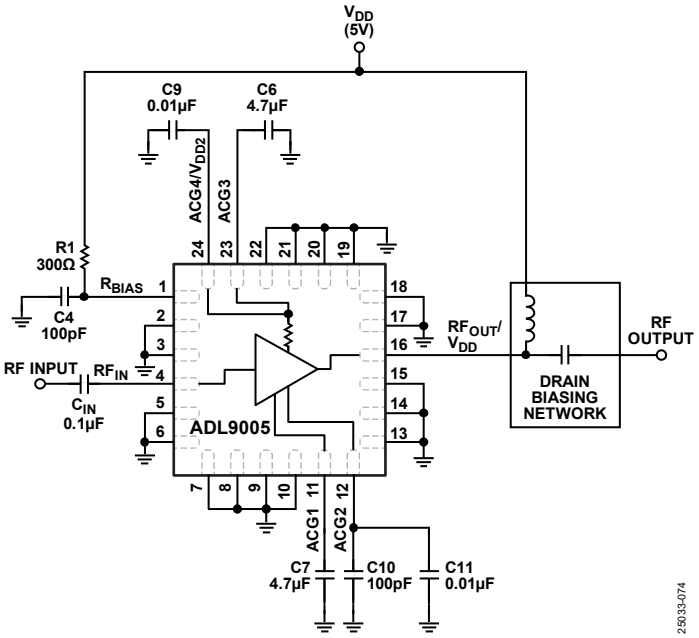


Figure 74. Typical Application Circuit

BIASING THE ADL9005 BY USING THE LTM8020

The LTM8020, µModule® regulator is suitable for the ADL9005 due to its compact size and wide input voltage range of 4 V to 36 V while maintaining high efficiency and output noise below the maximum allowable ripple of the ADL9005 due to its high power supply modulation ratio.

The ADL9005 can be powered by using a well regulated power source. The LTM8020 is a complete 200 mA, dc to dc, step-down power supply that provides a single 5 V supply to V_{DD} through a bias tee on R_{BIAS}. The recommended input voltage (V_{IN}) for the LTM8020 is from 6.5 V to 36 V to achieve a 5 V output voltage (V_{OUT}).

Figure 75 shows the application circuit for ADL9005 using the LTM8020 regulator.

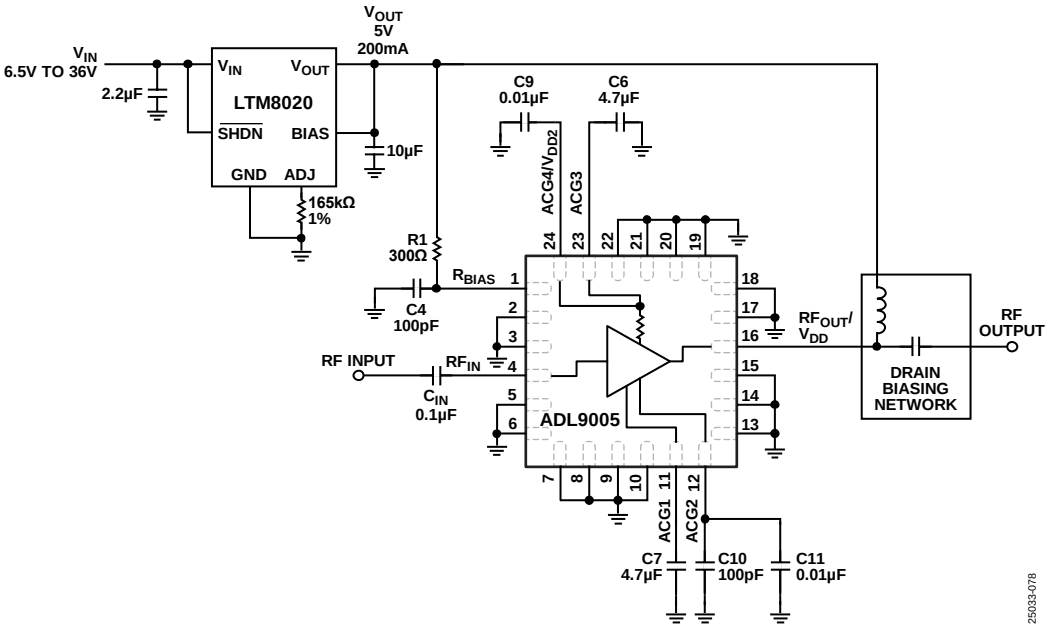


Figure 75. Application Circuit for the ADL9005 Using the LTM8020 Regulator

PROVIDING DRAIN BIAS

The ADL9005 was characterized using a connectorized wideband bias tee (Marki Microwave BT2-0040). In practice, the drain bias must be provided by a board mountable component. Drain biasing for a wideband amplifier, such as the ADL9005, is traditionally provided by connecting a wideband conical inductor between RF_{OUT}/V_{DD} and the 5 V power supply, as shown in Figure 74. Conical inductors are fragile and physically large. Figure 76 shows an alternative biasing circuit that uses 0402 sized, surface-mount components. The gain, input return loss, and output return loss over frequency are shown in Figure 77.

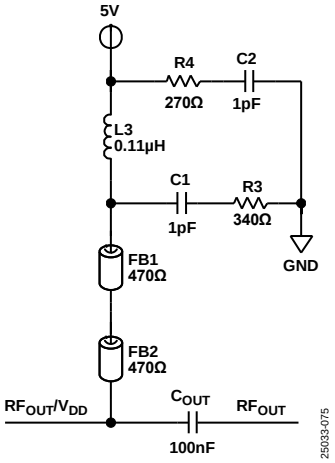


Figure 76. Surface-Mounted Bias Tee Schematic

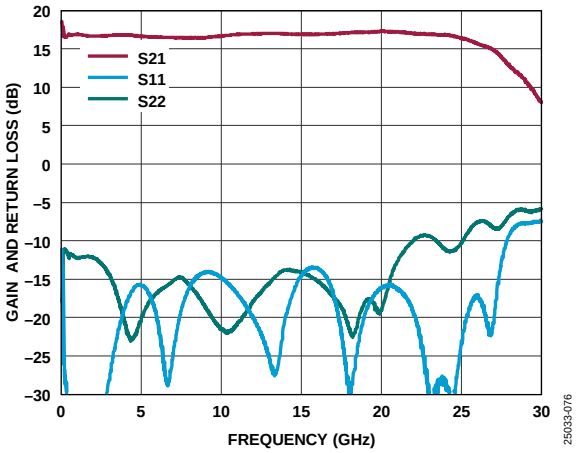


Figure 77. Gain and Return Loss vs. Frequency Using the Surface-Mount Bias Tee

The circuit consists of ferrite beads (FB1 and FB2), an ac coupling capacitor (C_{OUT}), an inductor (L3), de-Q resistors (R3 and R4), and bypass capacitors (C1 and C2).

The R3, R4, C1, and C2 decoupling components are used to reduce the RF coupling and to filter out power supply noise. R3 and R4 are de-Q resistors that can reduce frequency glitches caused by interactions between the PCB and the decoupling capacitors.

FB2 is critical to achieving high frequency operation. Optimal performance is achieved when FB2 touches down on the RF trace directly. FB1 is also a critical component that must be placed as close as possible to FB2 because a longer trace adds increased inductance and capacitance. FB1 mitigates resonances caused by the interaction between FB2 and the PCB.

The L3 inductor is only needed if operation at below 100 MHz is required. Otherwise, omit L3.

Table 10 lists the part numbers of the manufacturers and values used in the surface-mounted bias tee circuit shown in Figure 76.

Further details on design of surface-mount bias tee circuits can be found in Application Note AN-2061.

Table 10. Part Numbers of the Manufacturers and Values Used in the Surface-Mounted Bias Tee Circuit Shown in Figure 76

Component	Value	Manufacturer	Part Number
FB1, FB2	470 Ω	Murata	BLM15GG471SN1D
L3	0.11 µH	Coilcraft	0805LS-111X_E_
C_{OUT}	100 nF	American Technical Ceramics	ATC 560L
R3	340 Ω	Panasonic	ERA-2AEB3400X
C1, C2	1 pF	Murata	GJM1555C1H1R0CB01D
R4	270 Ω	Panasonic	ERJ-2GEJ271X

PROVIDING DRAIN BIAS THROUGH THE ACG4/V_{DD2} PIN

An alternative way to bias the ADL9005 is through the ACG4/V_{DD2} pin (Pin 24), which is shown in Figure 78. Because of the voltage drop across the internal bias resistor, a higher V_{DD} is required. If a 300 Ω bias resistor (R1) is used and connected to the 5 V power supply, which results in a total current of 80 mA, a V_{DD} of 8.5 V is recommended. R1 can also be connected to the V_{DD} of 8.5 V. In this case, to set I_{DQ} to 80 mA, use an R1 value of 850 Ω on R_{BIAS}. The performance of this circuit is summarized in Figure 67 to Figure 72.

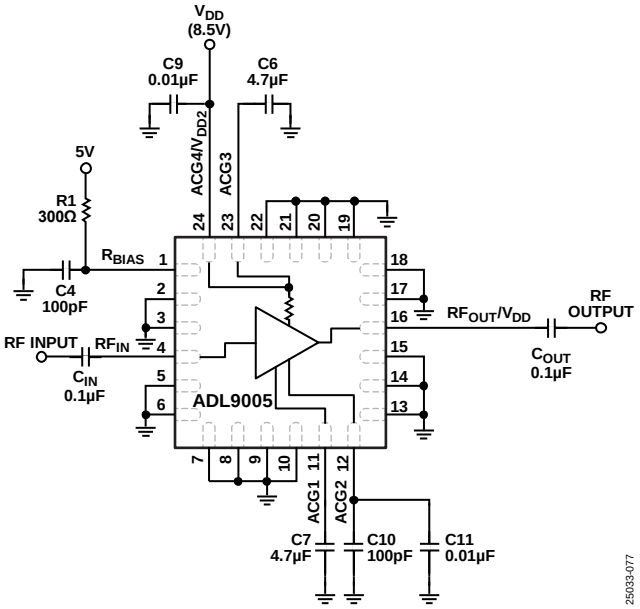
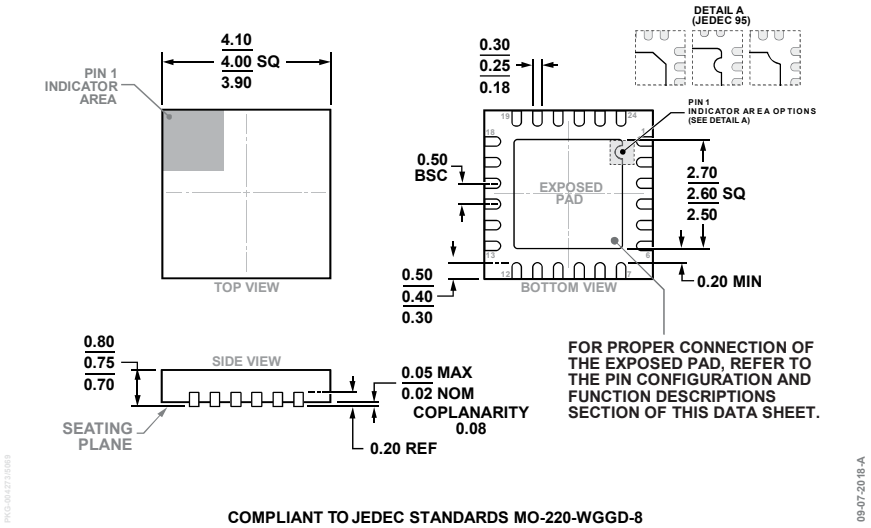


Figure 78. Providing Resistive Drain Bias Through the ACG4/V_{DD2} Pin

POWER-UP AND POWER-DOWN SEQUENCING

Apply the RF input signal after the main supply voltage and the voltage driving R_{BIAS} (R1 in Figure 74 and Figure 78) and remove the RF input signal before the main supply voltage and the voltage on R_{BIAS} are turned off. The voltage on R_{BIAS} can either be applied simultaneously with V_{DD} or after V_{DD} is applied.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 79. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm and 0.75 Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description[4]	Package Option
ADL9005ACPZN	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
ADL9005ACPZN-R7	−40°C to +85°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
ADL9005-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] When ordering the evaluation board only, reference the model number, ADL9005-EVALZ.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the ADL9005ACPZN and ADL9005ACPZN-R7 is nickel palladium gold (NiPdAu).

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