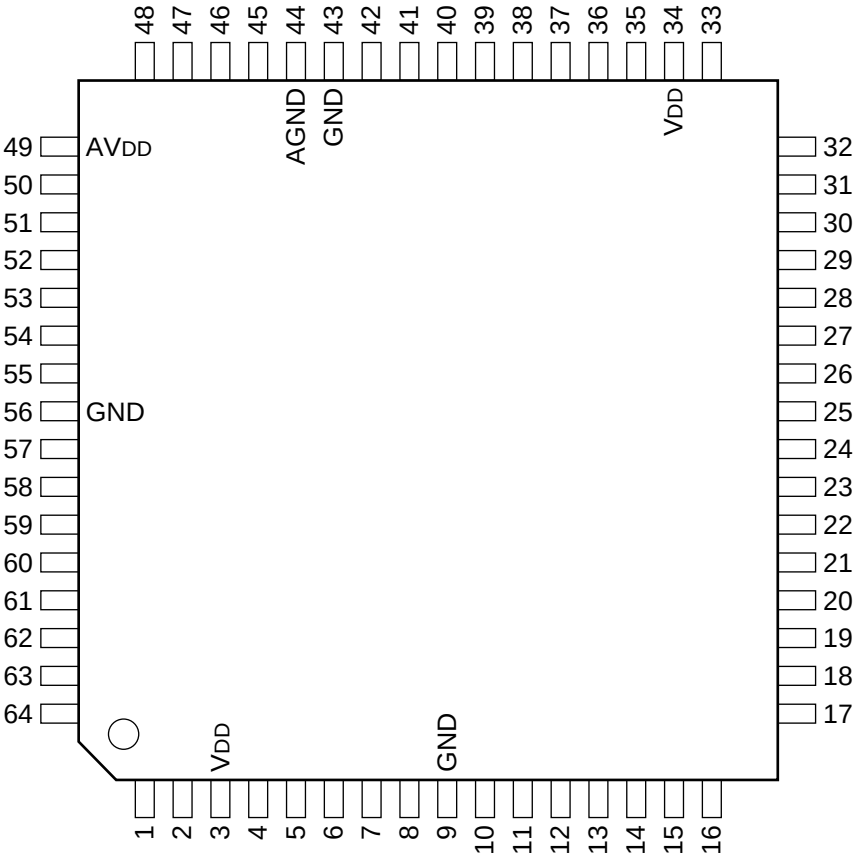

C-MOS MICRO COMPUTER
-TOP VIEW-



MODE 1

35	P50/TMCI	D0	10
36	P51/FTI1	D1	11
37	P52/FTI2/TMRI	D2	12
38	P53/TM0	D3	13
39	P54/FTOB1/FTCI1	D4	14
40	P55/FTOB2/FTCI2	D5	15
41	P56/FTOA1	D6	16
42	P57/FIOA2/∅	D7	17
		A0	18
45	P60/AN0	A1	19
46	P61/AN1	A2	20
47	P62/AN2	A3	21
48	P63/AN3	A4	22
		A5	23
		A6	24
50	P70/TXD2	A7	25
51	P71/RXD2	A8	26
52	P72/SCK2	A9	27
53	P73/TXD1	A10	28
54	P74/RXD1	A11	29
55	P75/SCK1	A12	30
		A13	31
		A14	32
59	P10/ $\overline{\text{WAIT}}$	A15	33
60	P11/ $\overline{\text{IRQ0}}$		
61	P12/ $\overline{\text{ADTRG}}/\overline{\text{IRQ1}}$	RD	1
62	P13/ $\overline{\text{IRQ2}}$	WR	2
63	P14/ $\overline{\text{IRQ3}}$		
		AS	64
4	MD0		
5	MD1		
6	MD2		
7	RES		
8	NMI		
57	EXTAL		
58	XTAL		

MODE 2

45	P60/AN0	D0	10
46	P61/AN1	D1	11
47	P62/AN2	D2	12
48	P63/AN3	D3	13
		D4	14
50	P70/TXD2	D5	15
51	P71/RXD2	D6	16
52	P72/SCK2	D7	17
53	P73/TXD1		
54	P74/RXD1	P30/A0	18
55	P75/SCK1	P31/A1	19
		P32/A2	20
		P33/A3	21
59	P10/ $\overline{\text{WAIT}}$	P34/A4	22
60	P11/ $\overline{\text{IRQ0}}$	P35/A5	23
61	P12/ $\overline{\text{ADTRG}}/\overline{\text{IRQ1}}$	P36/A6	24
62	P13/ $\overline{\text{IRQ2}}$	P37/A7	25
63	P14/ $\overline{\text{IRQ3}}$		
		P40/A8	26
4	MD0	P41/A9	27
5	MD1	P42/A10	28
6	MD2	P43/A11	29
		P44/A12/IRQ	30
7	RES	P45/A13/IRQ5	31
		P46/A14/IRQ6	32
8	NMI	P47/A15/IRQ7	33
57	EXTAL	P50/TMCI	35
58	XTAL	P51/FTI1	36
		P52/FTI2/TMRI	37
		P53/TM0	38
		P54/FTOB1/FTCI1	39
		P55/FTOB2/FTCI2	40
		P56/FTOA1	41
		P57/FIOA2/∅	42
		RD	1
		WR	2
		AS	64

MODE 3

35	P50/TMCI	D0	10
36	P51/FTI1	D1	11
37	P52/FTI2/TMRI	D2	12
38	P53/TM0	D3	13
39	P54/FTOB1/FTCI1	D4	14
40	P55/FTOB2/FTCI2	D5	15
41	P56/FTOA1	D6	16
42	P57/FIOA2/ø	D7	17
			18
		A0	19
45	P60/AN0	A1	20
46	P61/AN1	A2	21
47	P62/AN2	A3	22
48	P63/AN3	A4	23
		A5	24
		A6	25
50	P70/TXD2	A7	26
51	P71/RXD2	A8	27
52	A19	A9	28
53	P73/TXD1	A10	29
54	P74/RXD1	A11	30
55	P75/SCK1	A12	31
		A13	32
		A14	33
59	P10/ $\overline{\text{WAIT}}$	A15	63
60	P11/ $\overline{\text{IRQ0}}$		62
		A16	61
4	MD0	A17	
5	MD1	A18	
6	MD2		1
		WR	2
7	RES	RD	
			64
8	NMI	AS	
57	EXTAL		
58	XTAL		

MODE 4

35	P50/TMCI	D0	10
36	P51/FTI1	D1	11
37	P52/FTI2/TMRI	D2	12
38	P53/TM0	D3	13
39	P54/FTOB1/FTCI1	D4	14
40	P55/FTOB2/FTCI2	D5	15
41	P56/FTOA1	D6	16
42	P57/FIOA2/ø	D7	17
			18
		P30/A0	19
45	P60/AN0	P31/A1	20
46	P61/AN1	P32/A2	21
47	P62/AN2	P33/A3	22
48	P63/AN3	P34/A4	23
		P35/A5	24
		P36/A6	25
4	MD0	P37/A7	26
5	MD1	P40/A8	27
6	MD2	P41/A9	28
		P42/A10	29
7	RES	P43/A11	30
		P44/A12/ $\overline{\text{IRQ4}}$	31
8	NMI	P45/A13/ $\overline{\text{IRQ5}}$	32
		P46/A14/ $\overline{\text{IRQ6}}$	33
57	EXTAL	P47/A15/ $\overline{\text{IRQ7}}$	
58	XTAL		
		P10/ $\overline{\text{WAIT}}$	59
		P11/ $\overline{\text{IRQ0}}$	60
		P12/A18/ $\overline{\text{ADTRG}}/\overline{\text{IRQ1}}$	61
		P13/A17/ $\overline{\text{IRQ2}}$	62
		P14/A16/ $\overline{\text{IRQ3}}$	63
		P70/TXD2	50
		P71/RXD2	51
		P72/SCK2/A19	52
		P73/TXD1	53
		P74/RXD1	54
		P75/SCK1	55
		RD	1
		WR	2
		AS	64

MODE 7		
35	P50/TMCI	P10
36	P51/FTI1	P11/ $\overline{\text{IRQ0}}$
37	P52/FTI2/TMRI	P12/A18/ $\overline{\text{ADTRG}}/\overline{\text{IRQ1}}$
38	P53/TM0	P13/ $\overline{\text{IRQ2}}$
39	P54/FTOB1/FTCI1	P14/ $\overline{\text{IRQ3}}$
40	P55/FTOB2/FTCI2	P15
41	P56/FTOA1	P16
42	P57/FIOA2/ $\emptyset$	P17
		P20
45	P60/AN0	P21
46	P61/AN1	P22
47	P62/AN2	P23
48	P63/AN3	P24
		P25
		P26
50	P70/TXD2	P27
51	P71/RXD2	
52	P72/SCK2	P30
53	P73/TXD1	P31
54	P74/RXD1	P32
55	P75/SCK1	P33
		P34
		P35
4	MD0	P36
5	MD1	P37
6	MD2	
		P40
8	NMI	P41
		P42
57	EXTAL	P43
58	XTAL	P44/ $\overline{\text{IRQ4}}$
		P45/ $\overline{\text{IRQ5}}$
		P46/ $\overline{\text{IRQ6}}$
		P47/ $\overline{\text{IRQ7}}$
		RES

INPUTS			OPERATION MODE	CONTENTS
MD2	MD1	MD0		
0	0	1	MODE 1	EXTENSION MINIMUM MODE (ROM INVALID)
0	1	0	MODE 2	EXTENSION MINIMUM MODE (ROM VALID)
0	1	1	MODE 3	EXTENSION MAXIMUM MODE (ROM INVALID)
1	0	0	MODE 4	EXTENSION MAXIMUM MODE (ROM VALID)
1	1	1	MODE 7	SINGLE CHIP MODE

0; LOW LEVEL
1; HIGH LEVEL

