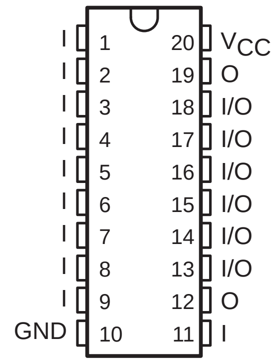
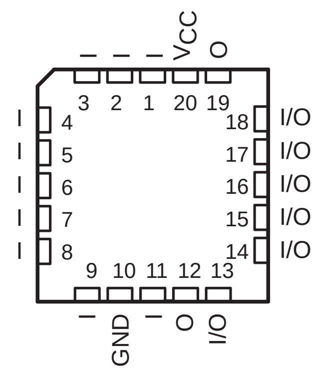
- **High-Performance Operation:**
  f_{max} (no feedback)
  TIBPAL16R’-7C Series . . . 100 MHz Min
  TIBPAL16R’-10M Series . . . 62.5 MHz Min
  f_{max} (internal feedback)
  TIBPAL16R’-7C Series . . . 100 MHz Min
  TIBPAL16R’-10M Series . . . 62.5 MHz Min
  f_{max} (external feedback)
  TIBPAL16R’-7C Series . . . 74 MHz Min
  TIBPAL16R’-10M Series . . . 52.5 MHz Min
  Propagation Delay
  TIBPAL16L’-7C Series . . . 7 ns Max
  TIBPAL16L’-10M Series . . . 10 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

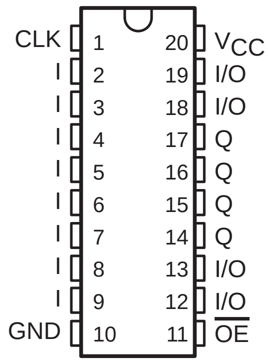
All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16’ C series is characterized from 0°C to 75°C. The TIBPAL16’ M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

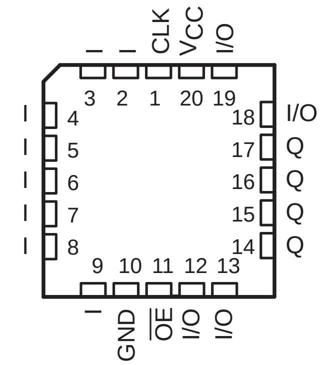
TIBPAL16R4’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



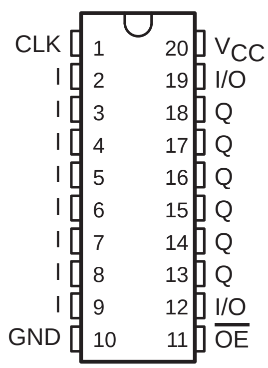
TIBPAL16R4’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



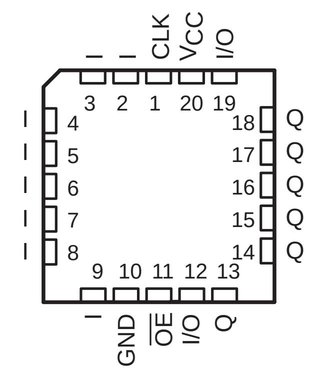
TIBPAL16R6’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



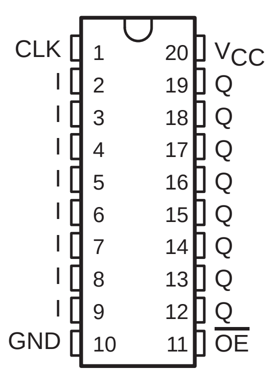
TIBPAL16R6’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



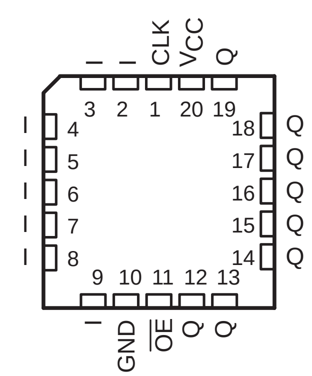
TIBPAL16R8’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

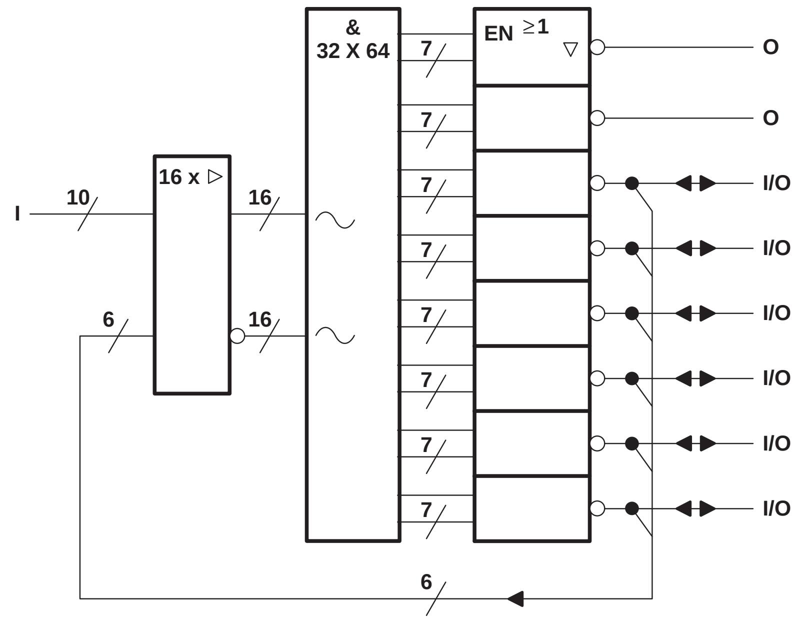
(TOP VIEW)



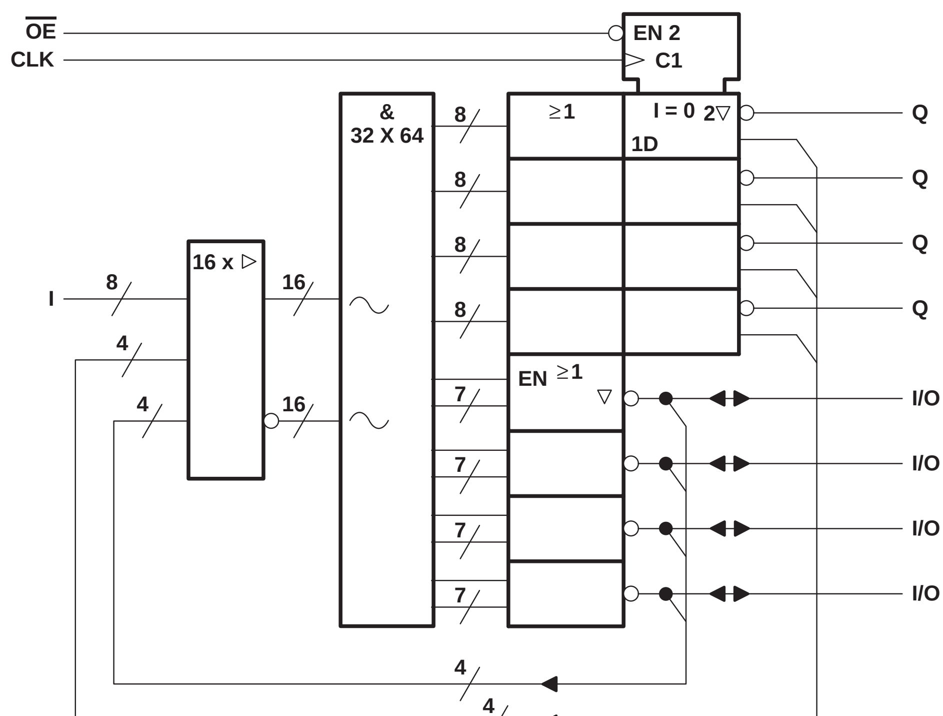
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8’



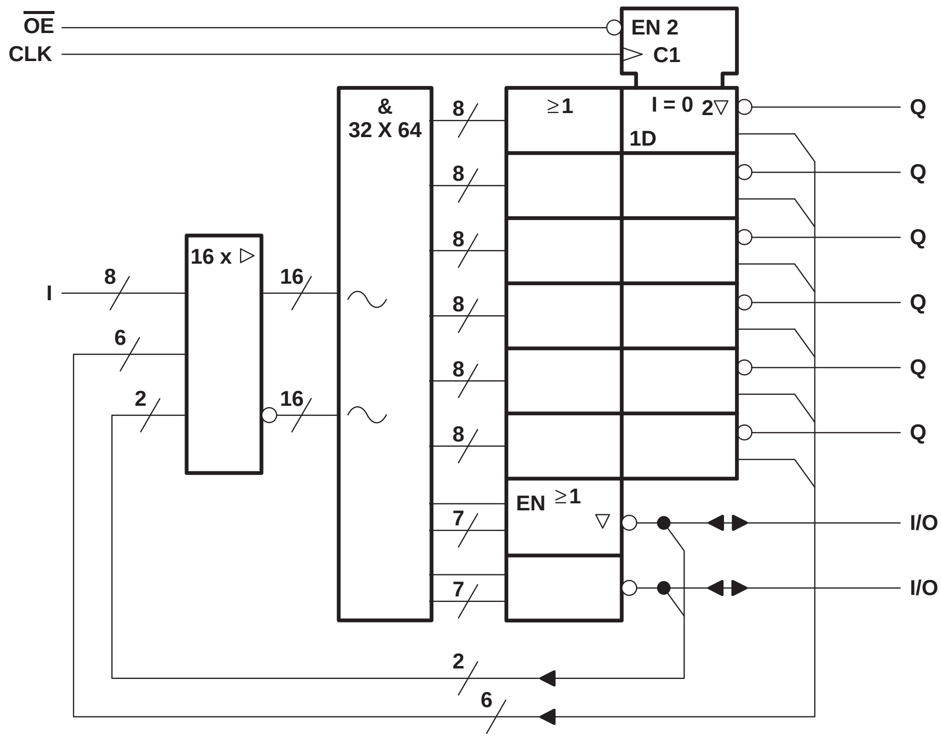
TIBPAL16R4’



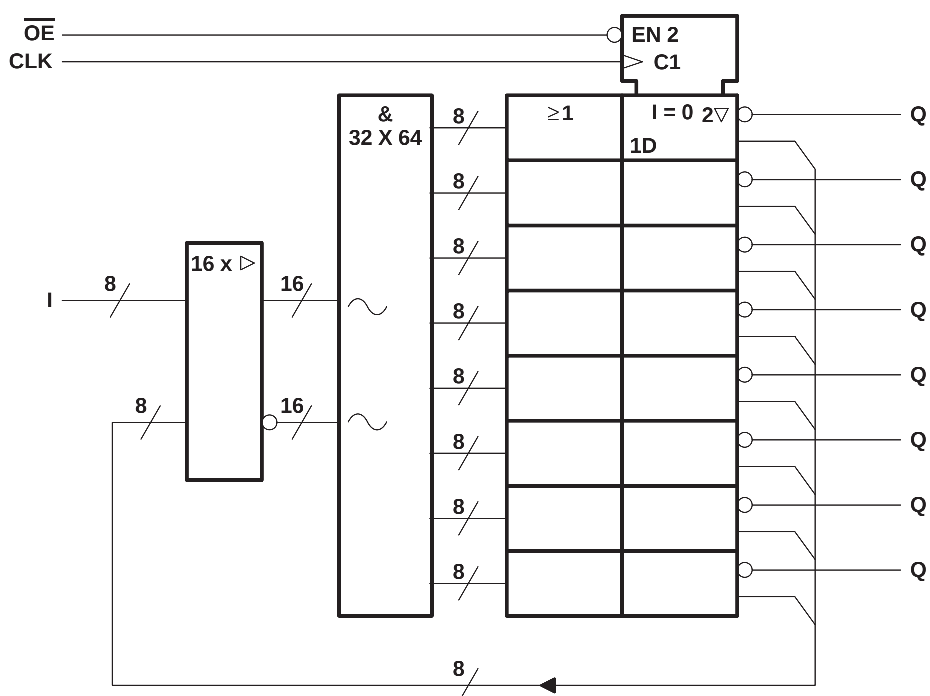
denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6’

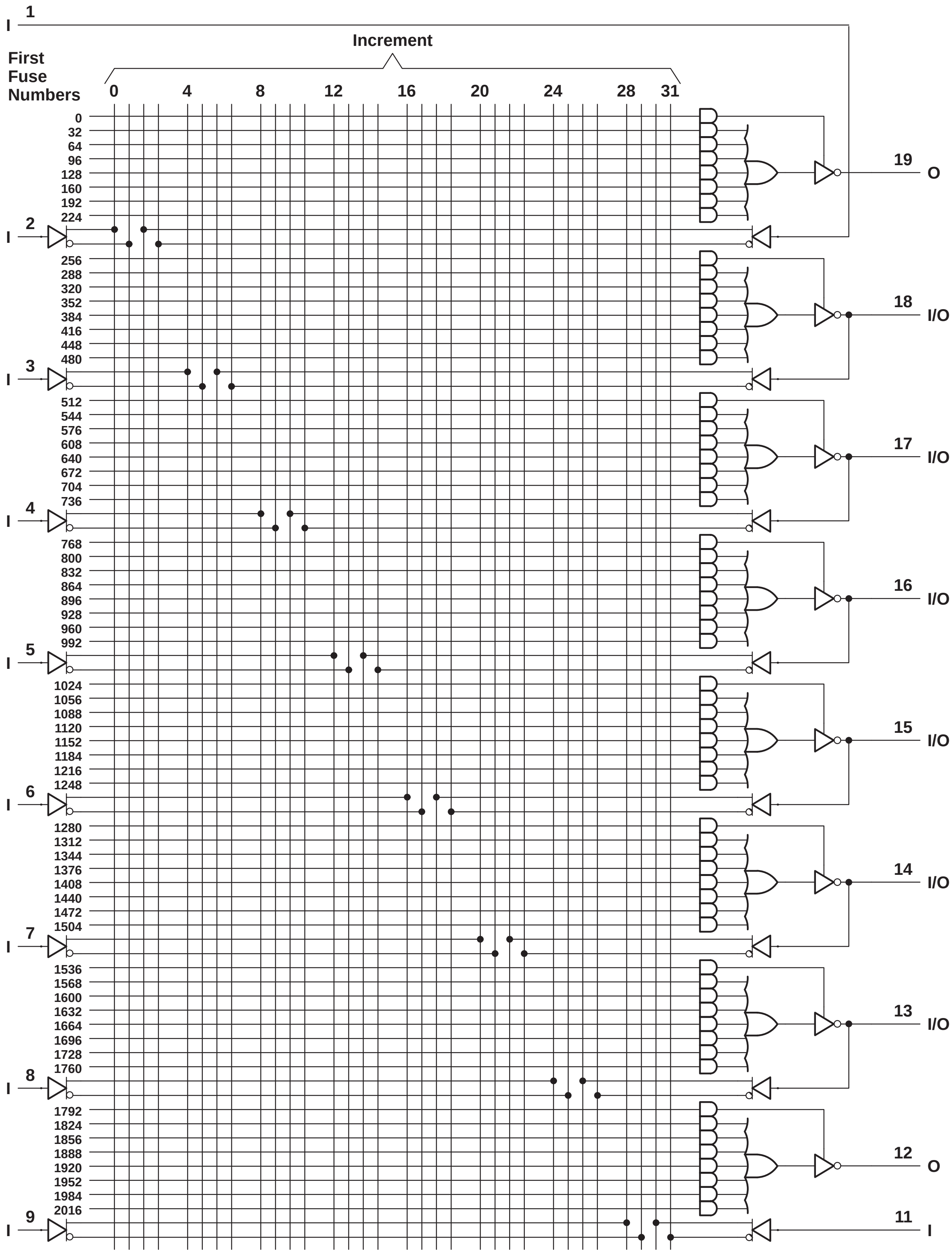


TIBPAL16R8’



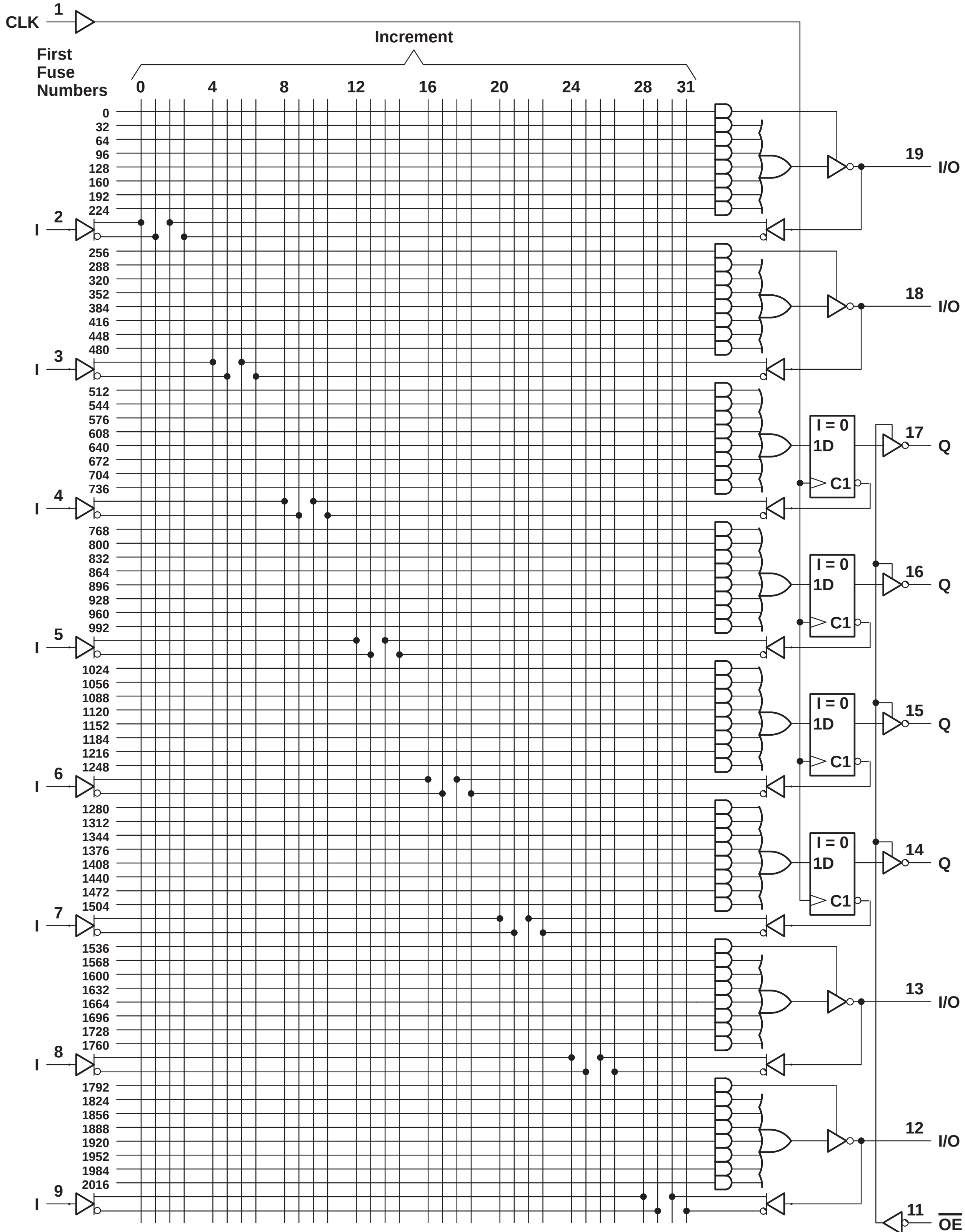
∼ denotes fused inputs

logic diagram (positive logic)



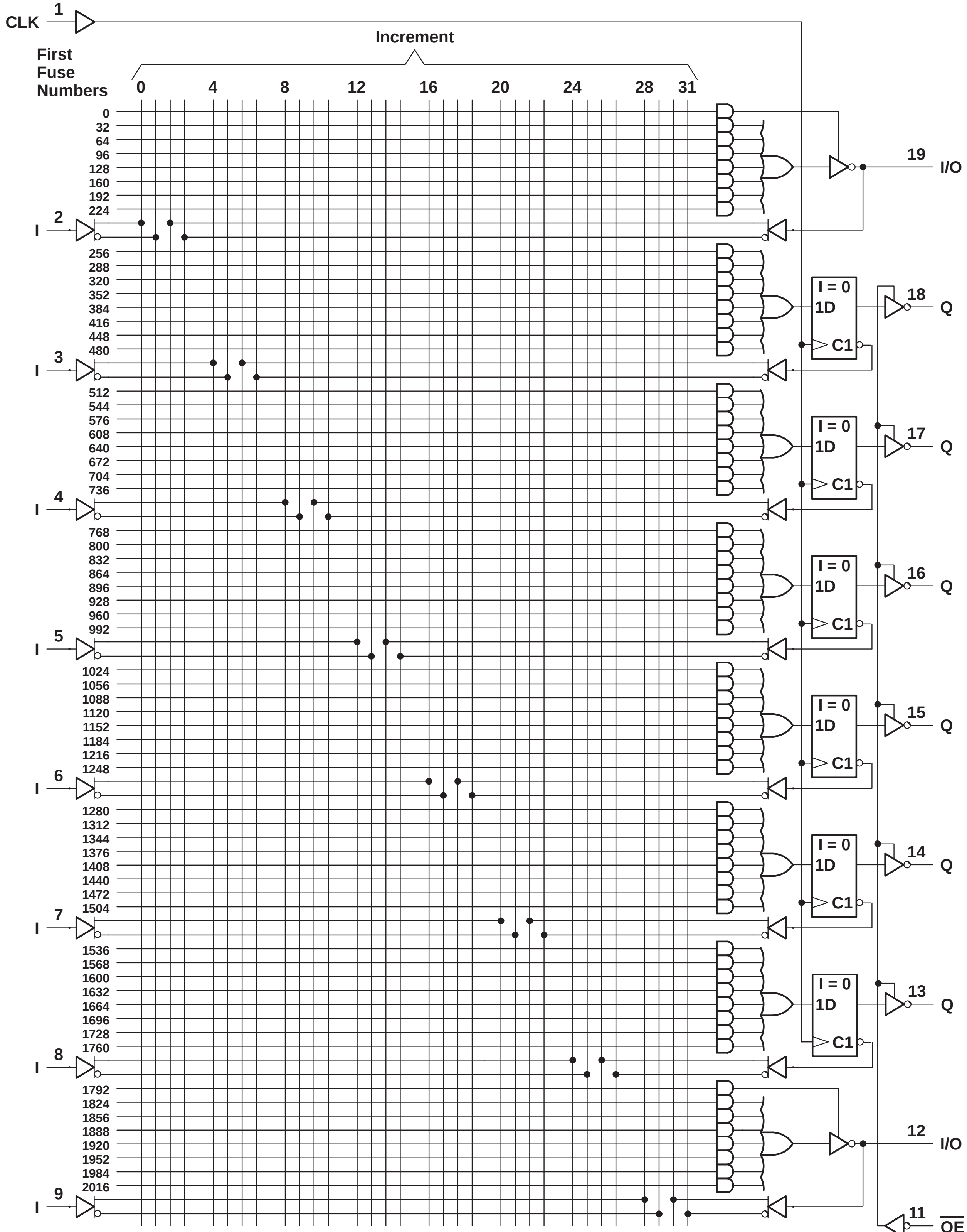
Fuse number = First fuse number + Increment

logic diagram (positive logic)



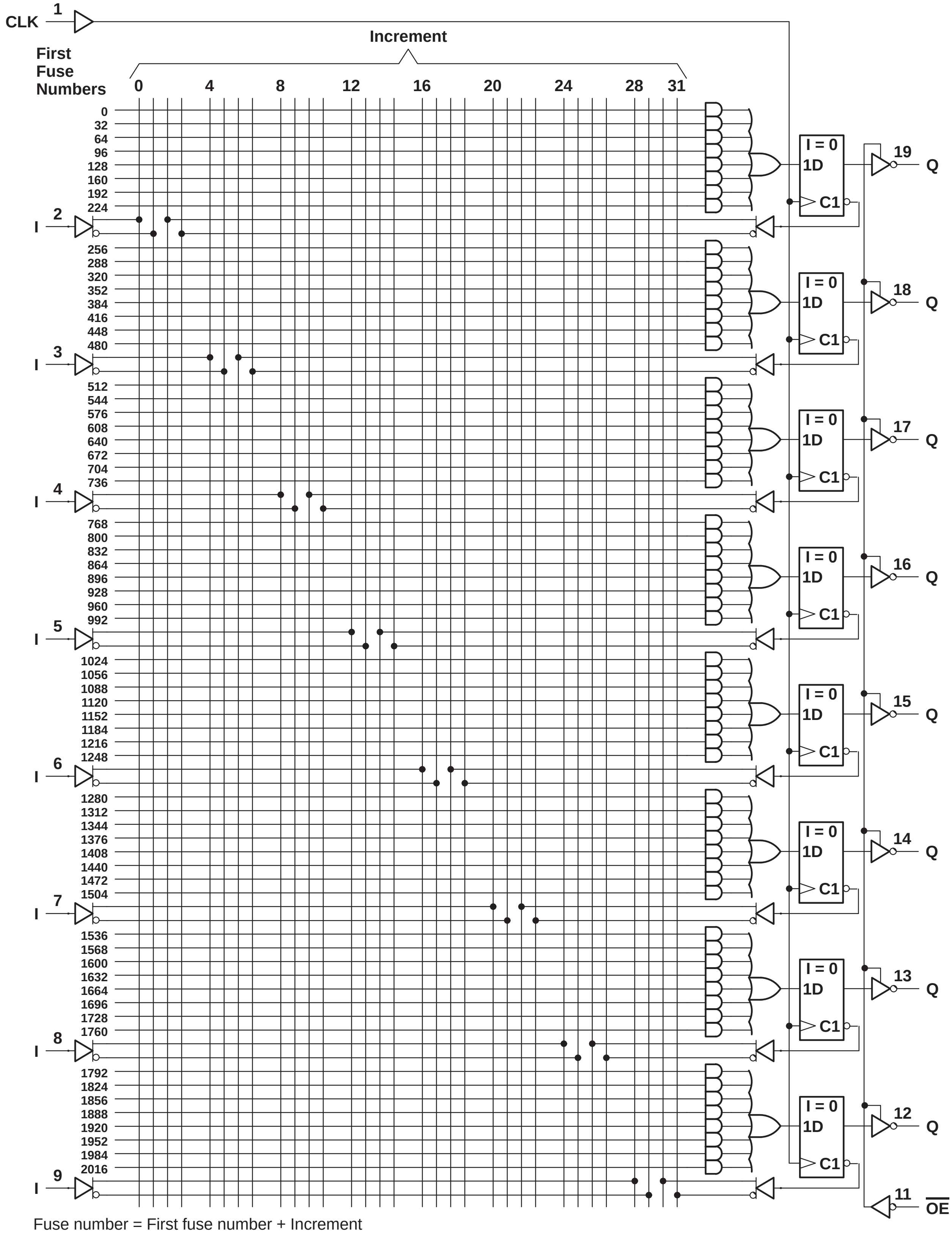
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	5			ns
		Low	5			
t_{su}	Setup time, input or feedback before clock↑		7			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	μA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	μA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			–80	–250	μA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		160	180	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

SRPS006D – D3115, MAY 1988 – REVISED MARCH 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	without feedback			R1 = 200 Ω, R2 = 390 Ω, See Figure 6	100			MHz
	with internal feedback (counter configuration)				100			MHz
	with external feedback				74			MHz
t_{pd}	I, I/O	O, I/O	1 or 2 outputs switching		3	5.5	7	ns
			8 outputs switching		3	6	7.5	ns
t_{pd}	CLK↑	Q			2	4	6.5	ns
t_{pd}§	CLK↑	Feedback input					3	ns
t_{en}	OE↓	Q				4	7.5	ns
t_{dis}	OE↑	Q				4	7.5	ns
t_{en}	I, I/O	O, I/O				6	9	ns
t_{dis}	I, I/O	O, I/O				6	9	ns
$t_{sk(o)}$¶	Skew between registered outputs					0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ See section for f_{max} specifications.
§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.
¶ This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . –55°C to 125°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}†	Setup time, input or feedback before clock↑		10			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	0, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–0.1	mA
	I/O ports						–0.25	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	µA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.08	–0.25	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	200	mA
C_i		f = 1 MHz,	V_I = 2 V			5		pF
C_o		f = 1 MHz,	V_O = 2 V			6		pF
$C_{clk/oe}$		f = 1 MHz,	$V_{CLK/OE}$ = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 6	62.5			MHz
	with internal feedback (counter configuration)			62.5			MHz
	with external feedback			52.5			MHz
t_{pd}	I, I/O	O, I/O		2	6	10	ns
t_{pd}	CLK↑	Q		1	4	9	ns
t_{pd}§	CLK↑	Feedback input				5	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		2	6	12	ns
t_{dis}	I, I/O	O, I/O		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ See section for f_{max} specifications. f_{max} with external feedback is not production tested but is calculated from the equation found in the f_{max} section.
§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

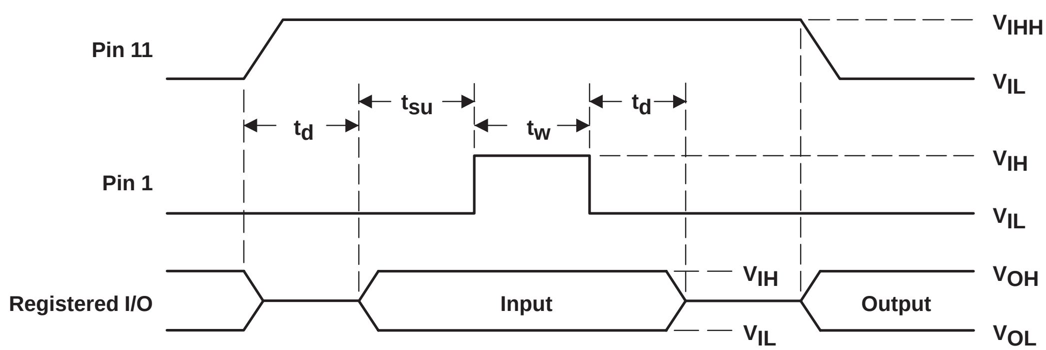
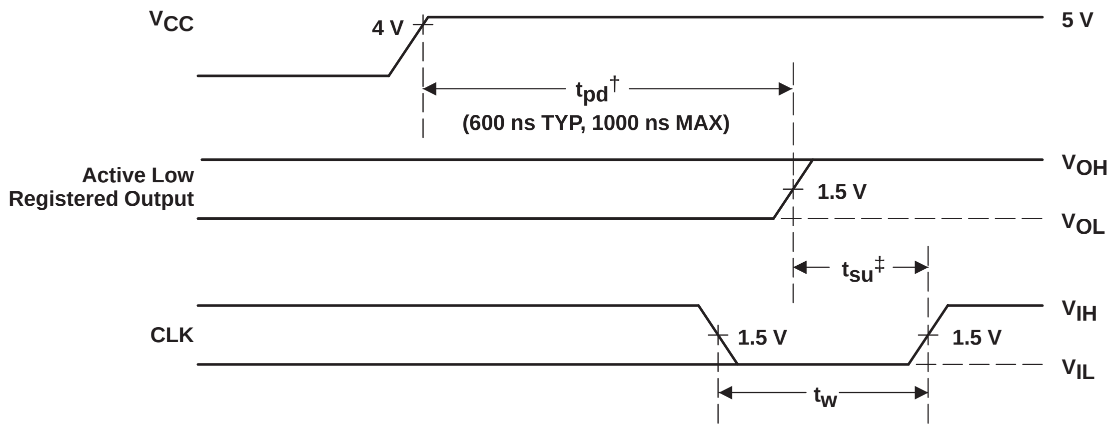


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time (t_{su} + t_h). However, the minimum f_{max} is determined by the minimum clock period (t_w high + t_w low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w\text{high} + t_w\text{low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

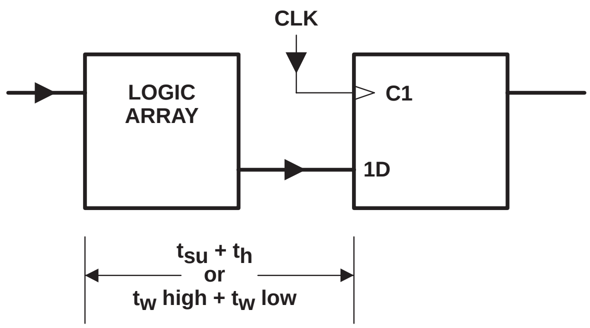


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK} - \text{to} - \text{FB})}$.

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

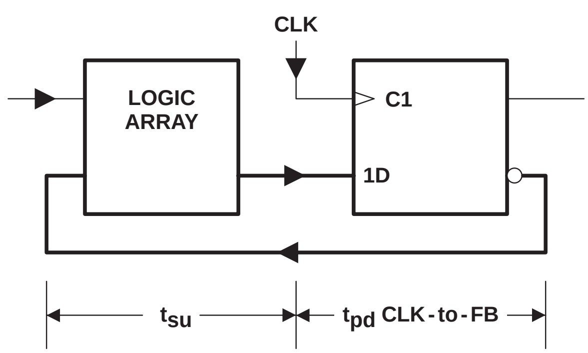


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK} - \text{to} - \text{Q})}$.

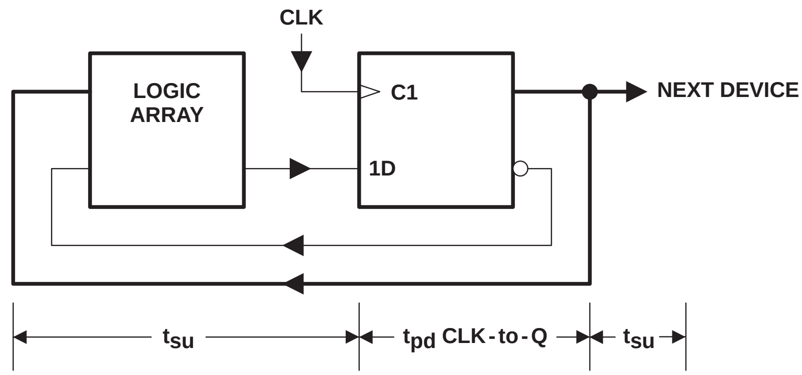
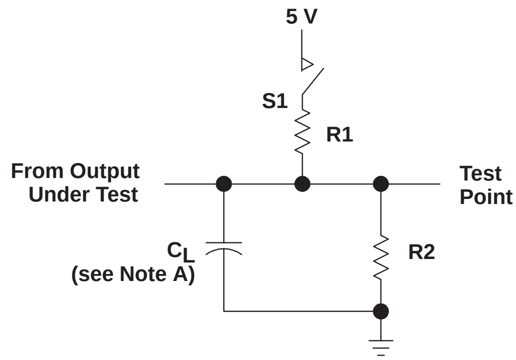
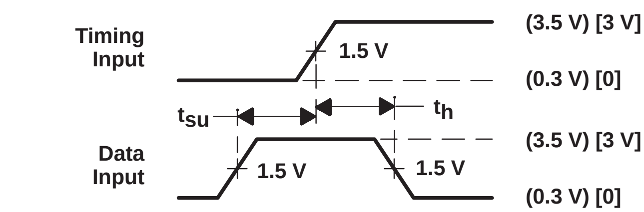


Figure 5. f_{max} With External Feedback

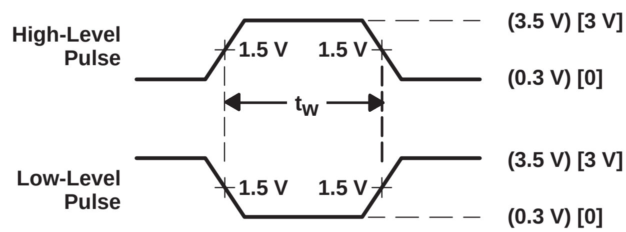
PARAMETER MEASUREMENT INFORMATION



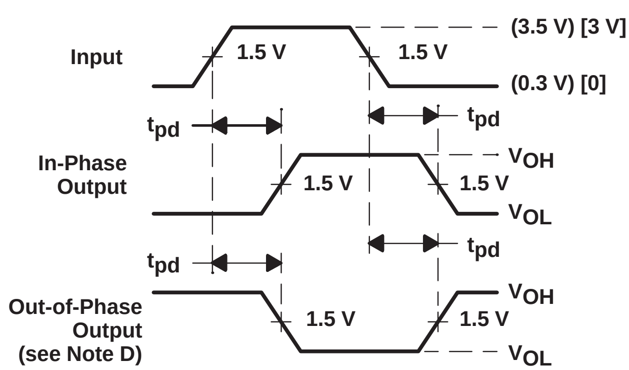
LOAD CIRCUIT FOR 3-STATE OUTPUTS



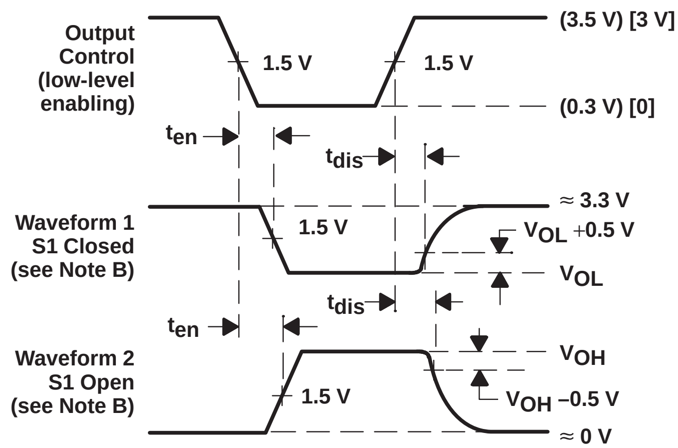
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%; For M suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

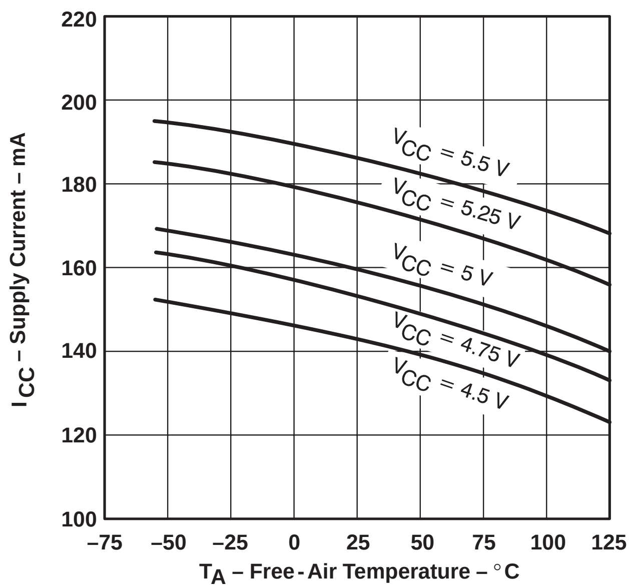


Figure 7

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

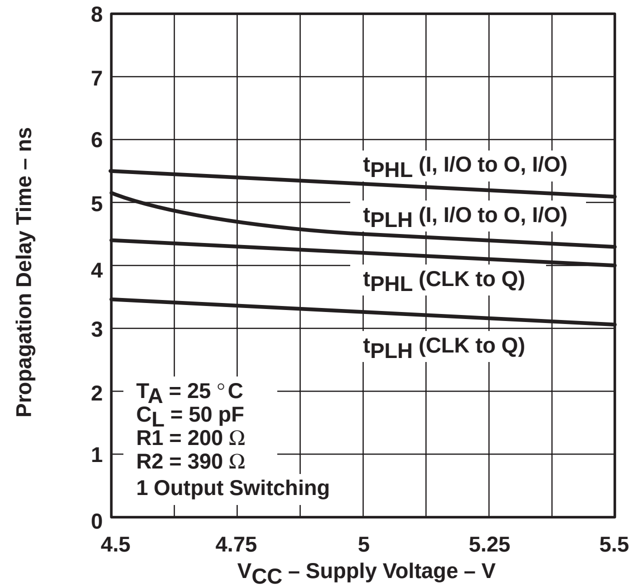


Figure 8

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

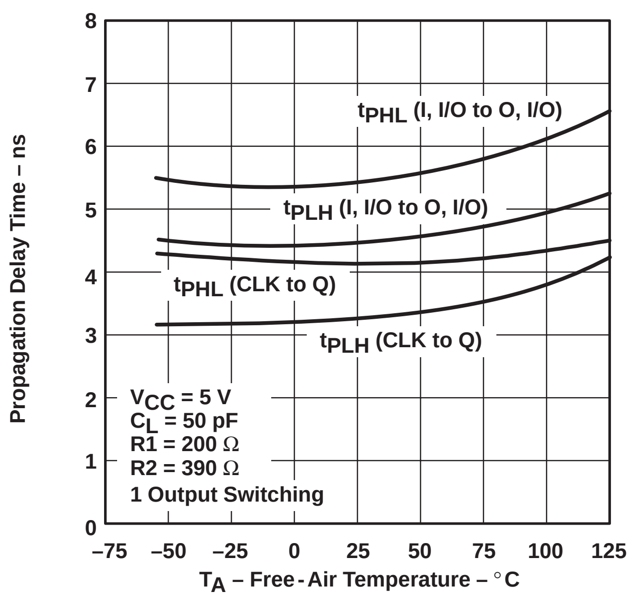


Figure 9

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

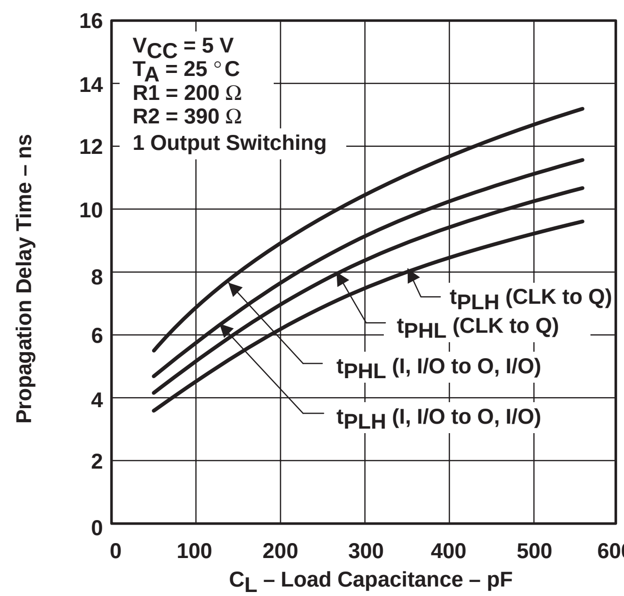


Figure 10

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

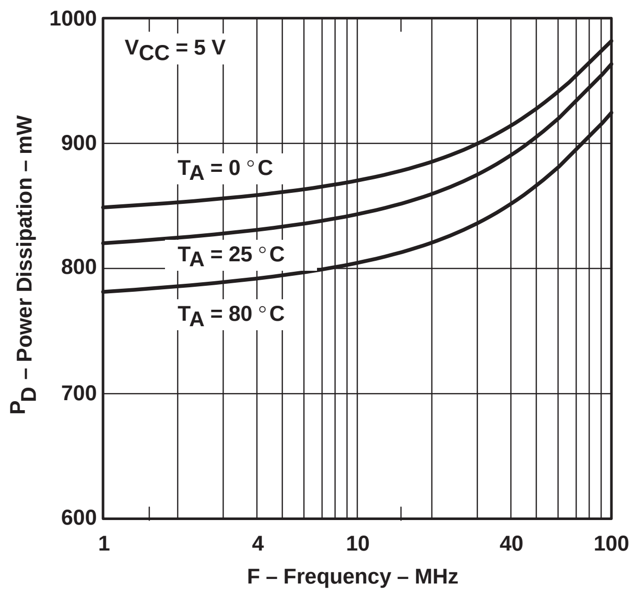


Figure 11

PROPAGATION DELAY TIME† vs NUMBER OF OUTPUTS SWITCHING

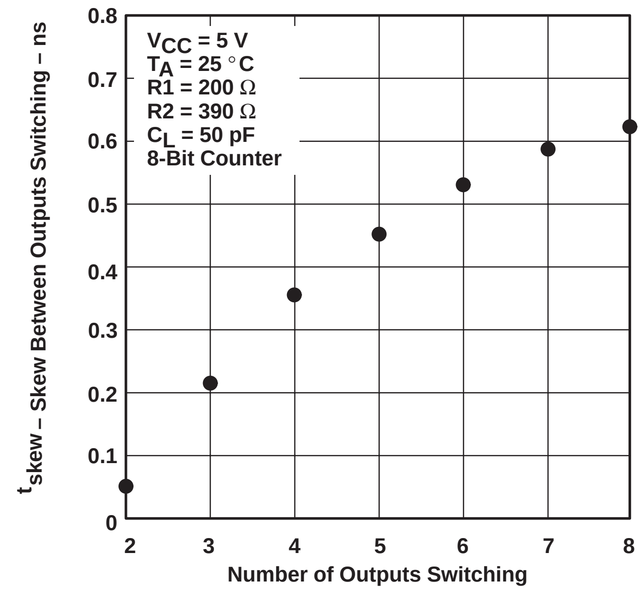


Figure 12

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

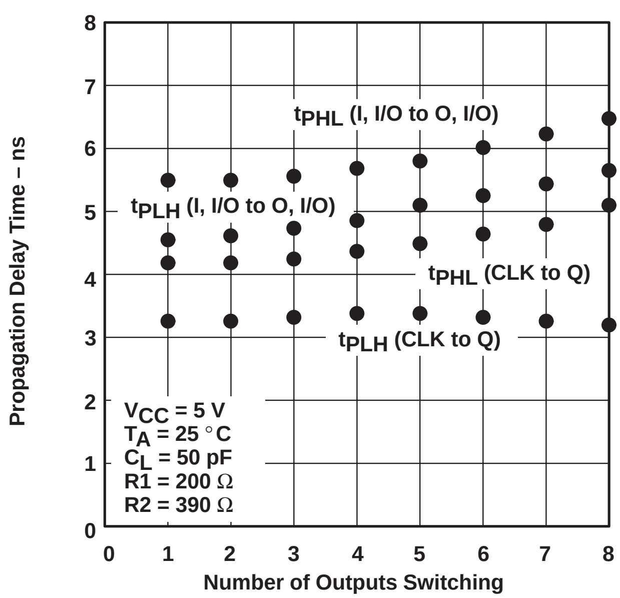


Figure 13

†Outputs switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

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TEXAS INSTRUMENTS

D0892

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Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-85155172A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515517RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515517SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155182A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515518RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515518SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155192A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515519RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515519SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-85155202A	LIFEBUY	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8515520RA	LIFEBUY	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8515520SA	LIFEBUY	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-10MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-10MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-10MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16L8-7CFN	ACTIVE	PLCC	FN	20	46	None	Call TI	Level-1-220-UNLIM
TIBPAL16L8-7CN	ACTIVE	PDIP	N	20	20	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-10MFKB	LIFEBUY	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-10MJB	LIFEBUY	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-10MWB	LIFEBUY	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R4-7CFN	OBSOLETE	PLCC	FN	20		None	Call TI	Call TI
TIBPAL16R4-7CN	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
TIBPAL16R6-10MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-10MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-10MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R6-7CFN	ACTIVE	PLCC	FN	20	46	None	Call TI	Level-1-220-UNLIM
TIBPAL16R6-7CN	NRND	PDIP	N	20	20	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-10MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-10MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-10MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
TIBPAL16R8-7CFN	OBSOLETE	PLCC	FN	20		None	Call TI	Call TI
TIBPAL16R8-7CN	OBSOLETE	PDIP	N	20		None	Call TI	Call TI

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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