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TECHNICAL DATA

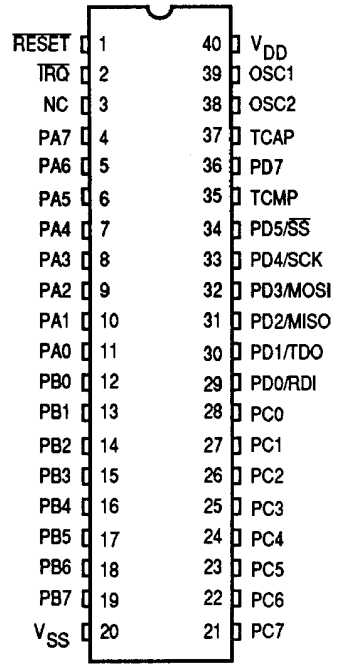
MC68HC05C9

Technical Summary
8-Bit Microcontroller Unit

The MC68HC05C9 high-density, complementary metal-oxide semiconductor (HCMOS) microcontroller unit (MCU) is a member of the M68HC05 Family of microcontrollers. This high-performance, low-cost MCU is a complete system on a single chip. On-chip resources include memory, parallel input/output (I/O), two serial I/O subsystems, and a 16-bit capture/compare timer subsystem.

Features

- 15936 Bytes of User ROM plus 240 Bytes of Self-Check ROM and 352 Bytes of RAM
- Memory Mapped I/O
- Selectable Memory Configurations
- 31 Bidirectional I/O Lines
- Fully Static Operation (No Minimum Clock Speed)
- On-Chip Oscillator with Crystal/Ceramic Resonator
- 16-Bit Capture/Compare Timer Subsystem
- Synchronous Serial Peripheral Interface (SPI) System
- Asynchronous Serial Communication Interface (SCI) System
- Power Saving STOP, WAIT, and Data-Retention Modes
- Single 3.0- to 5.5-Volt Supply (2-Volt Data-Retention Mode)
- Computer Operating Properly (COP) Watchdog Timer
- Clock Monitor
- Software-Programmable External Interrupt Sensitivity



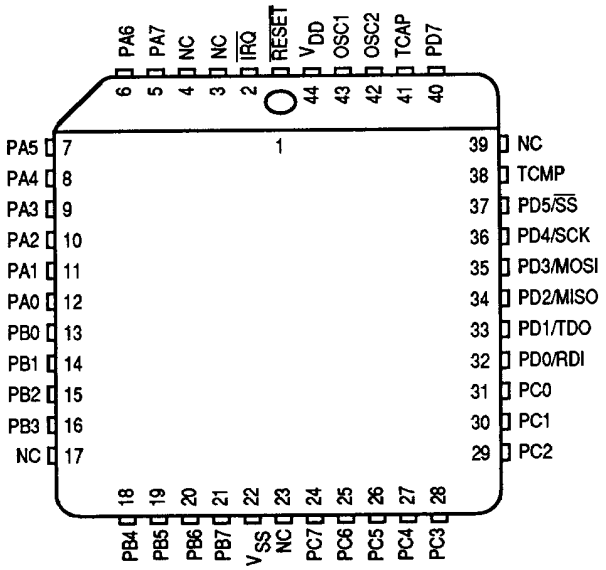
40-Pin DIP Pin Assignments

Package Type	Order Number
40-Pin DIP (P Suffix)	MC68HC05C9P
44-Pin PLCC (FN Suffix)	MC68HC05C9FN
44-Pin QFP (FU Suffix)	MC68HC05C9FU

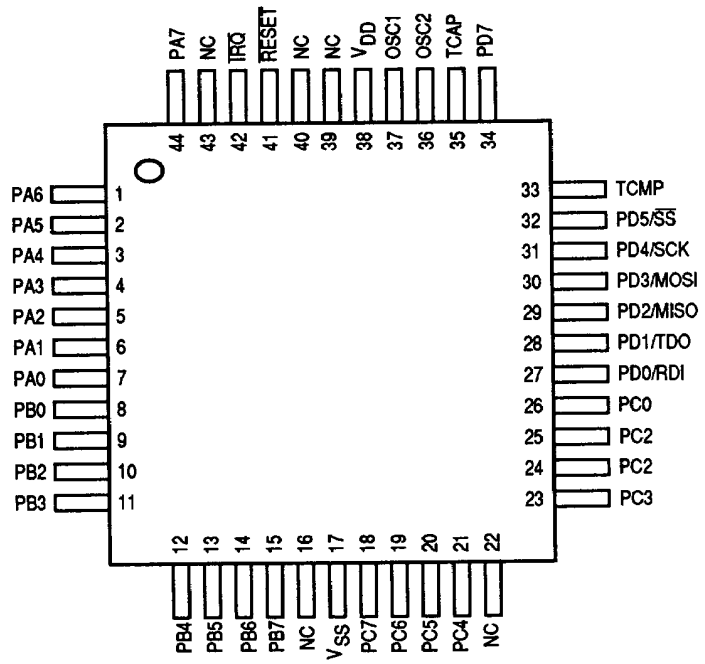
This document contains information on a new product. Specifications and information herein are subject to change without notice.

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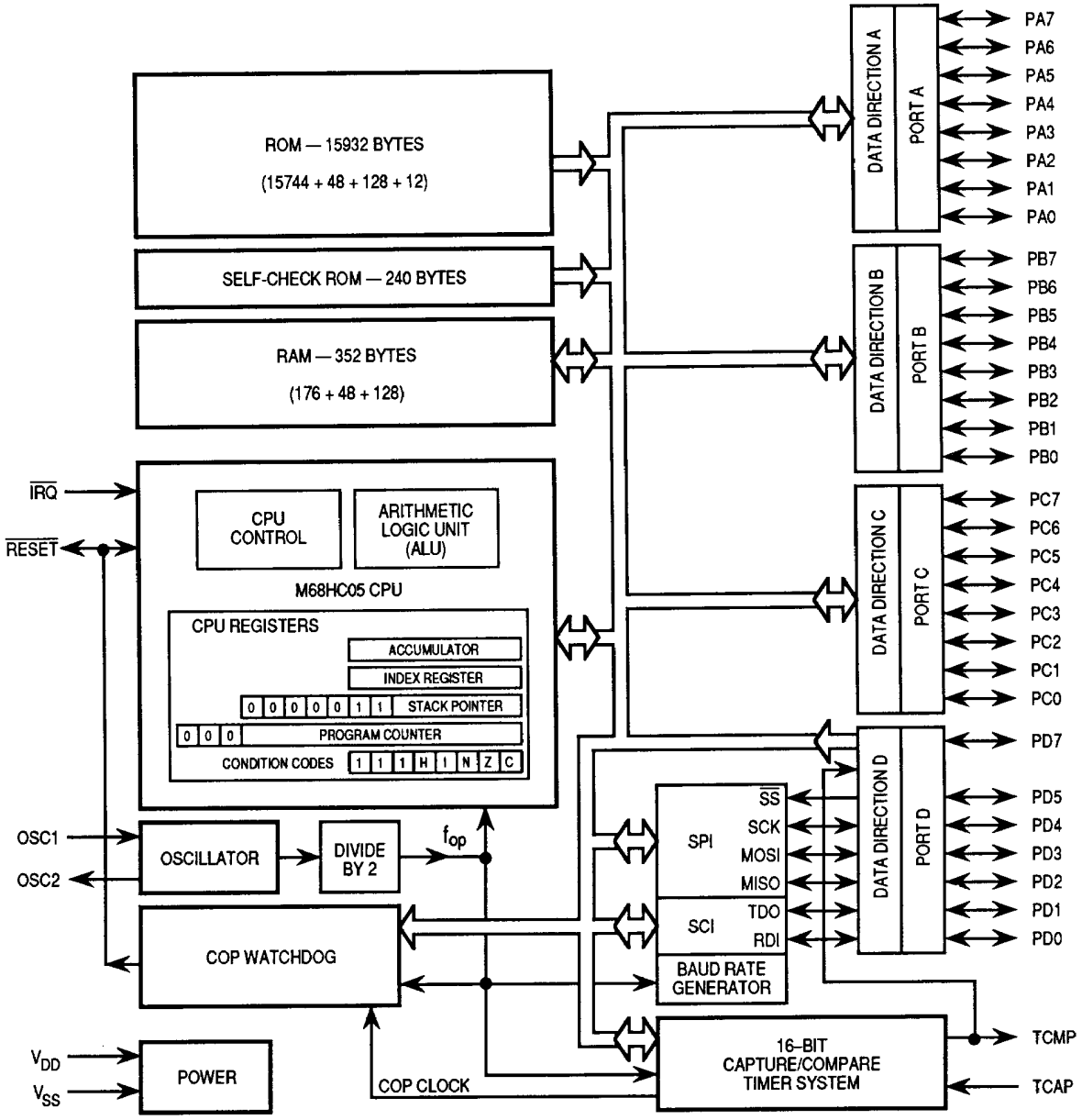
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44-Pin PLCC Pin Assignments



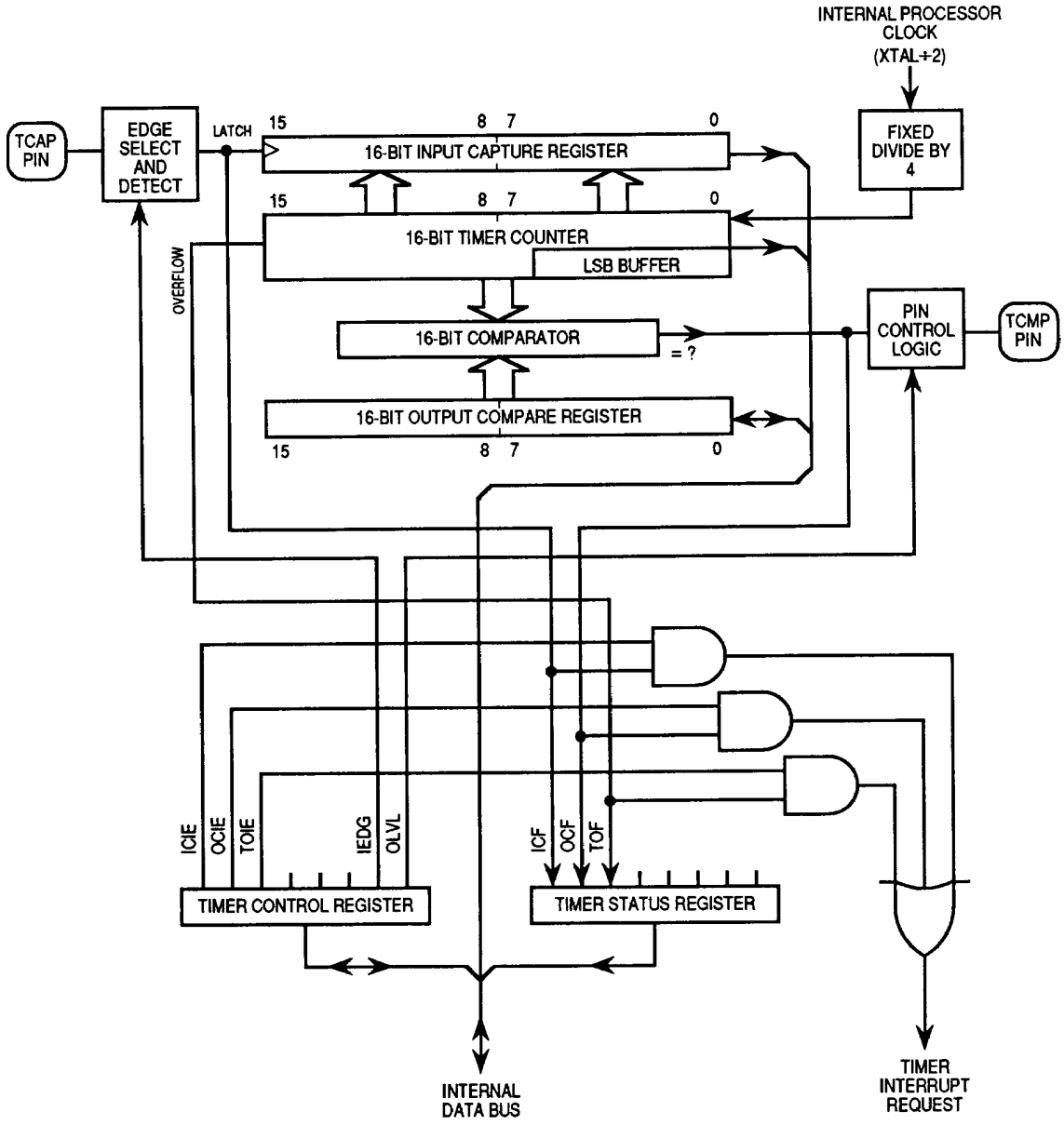
44-Pin QFP Pin Assignments



MC68HC05C9 Block Diagram

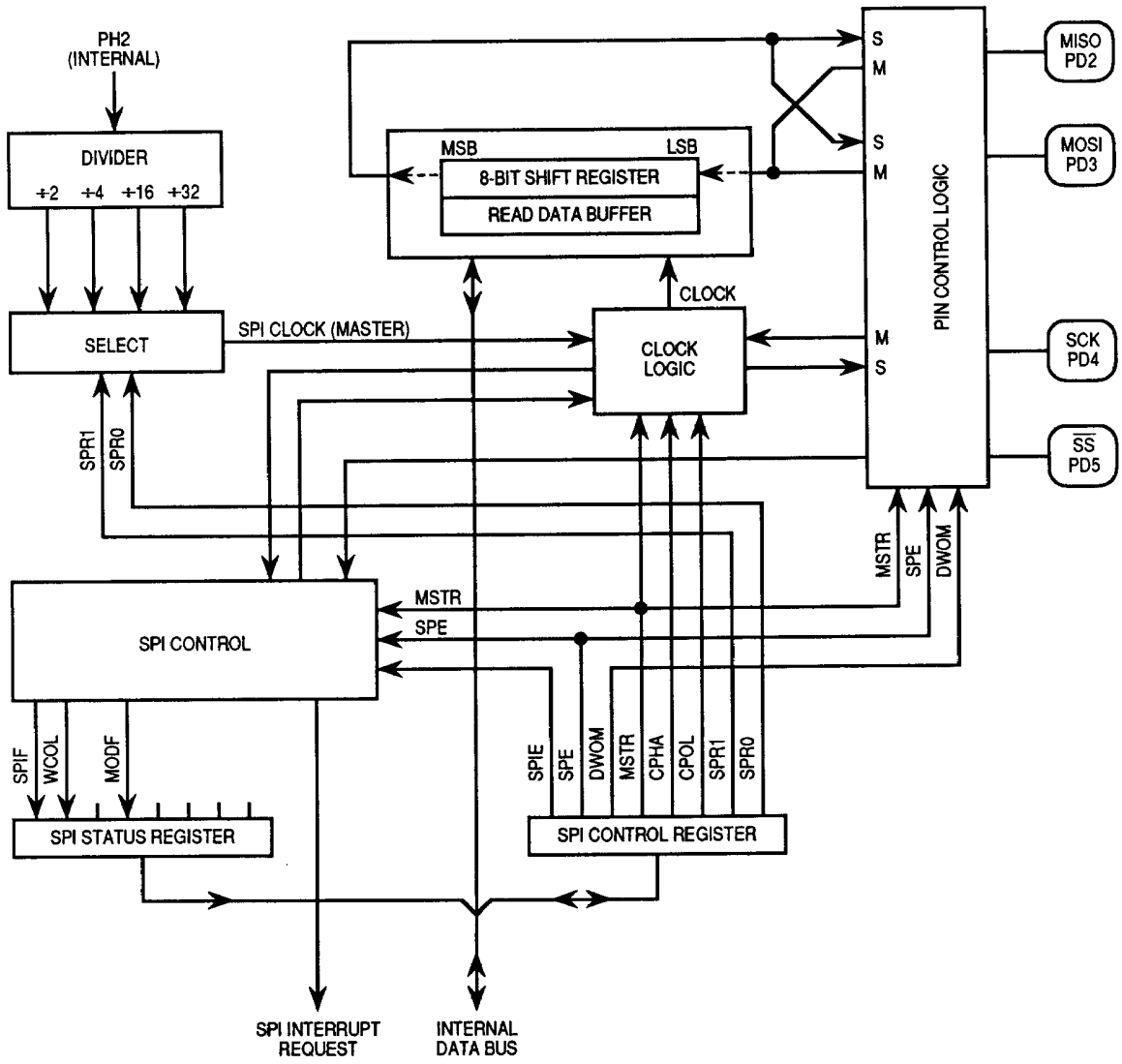
The 16-bit capture/compare timer system is based on a free-running 16-bit counter. Selected input edges cause the current counter value to be latched into a 16-bit input capture register so that software can later read this value to determine when the edge occurred. Output changes are scheduled to occur at a specific time by writing a value to a 16-bit output compare register. When the free-running counter value matches the output compare value, the planned pin action occurs.

For a 4-MHz oscillator frequency this timer has a basic resolution of 2 µs and a basic range of 131.1 ms. A timer overflow flag allows the range to be extended to any length of time period through software.



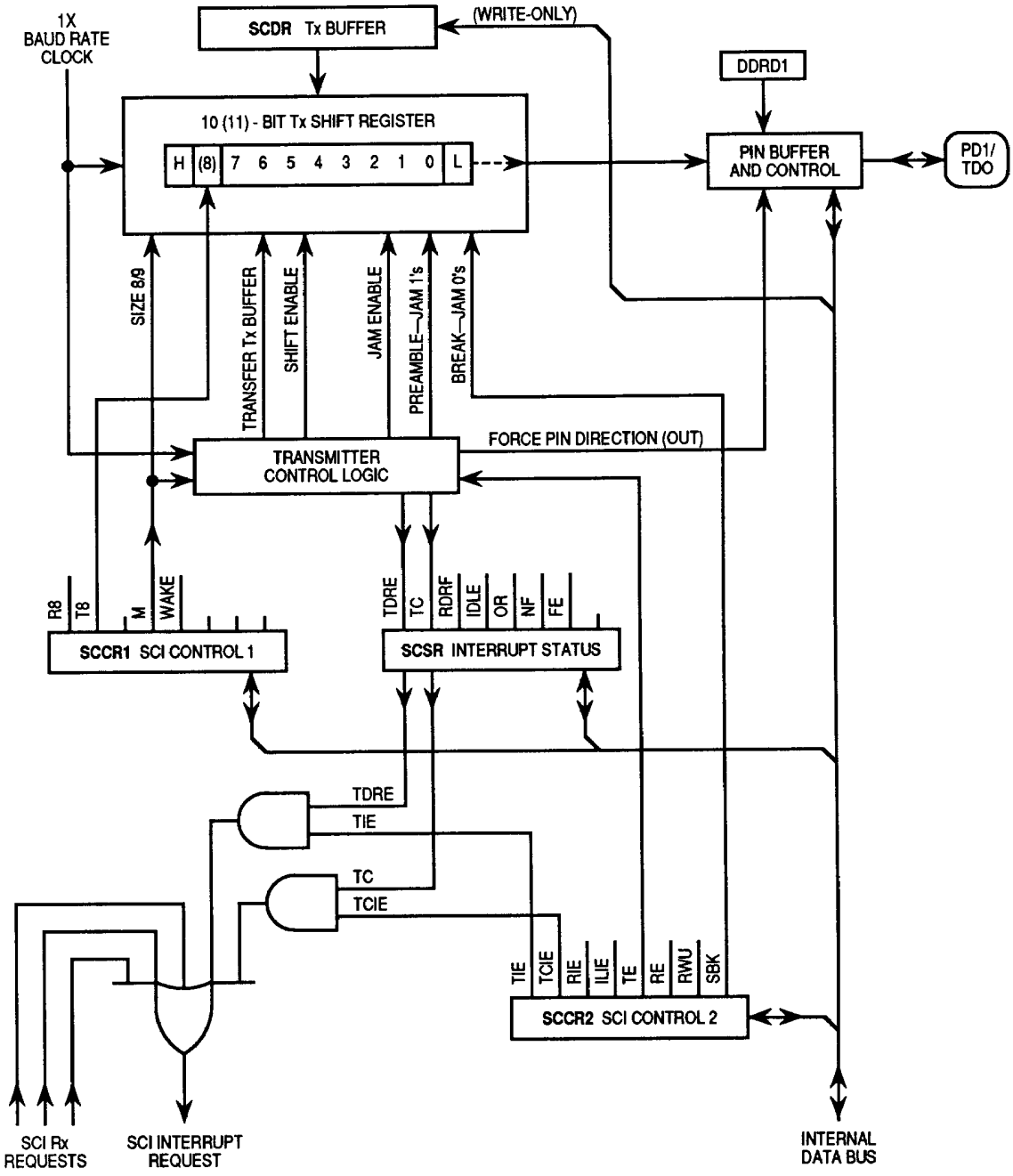
Capture/Compare Timer Block Diagram

The serial peripheral interface is one of two independent serial communications subsystems included on the MC68HC05C9. As its name implies it is primarily used to allow the MCU to communicate with peripheral devices, although it is also capable of interprocessor communications in a multimaster system. Peripheral devices can be as simple as an ordinary TTL shift register or as complex as a complete subsystem such as an LCD display driver or an analog to digital (A/D) converter subsystem. The SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The system can be configured as a master or a slave device. Data rates as high as 1M bits per second can be accommodated when the system is configured as a master and 2M bits per second when the system is operated as a slave.

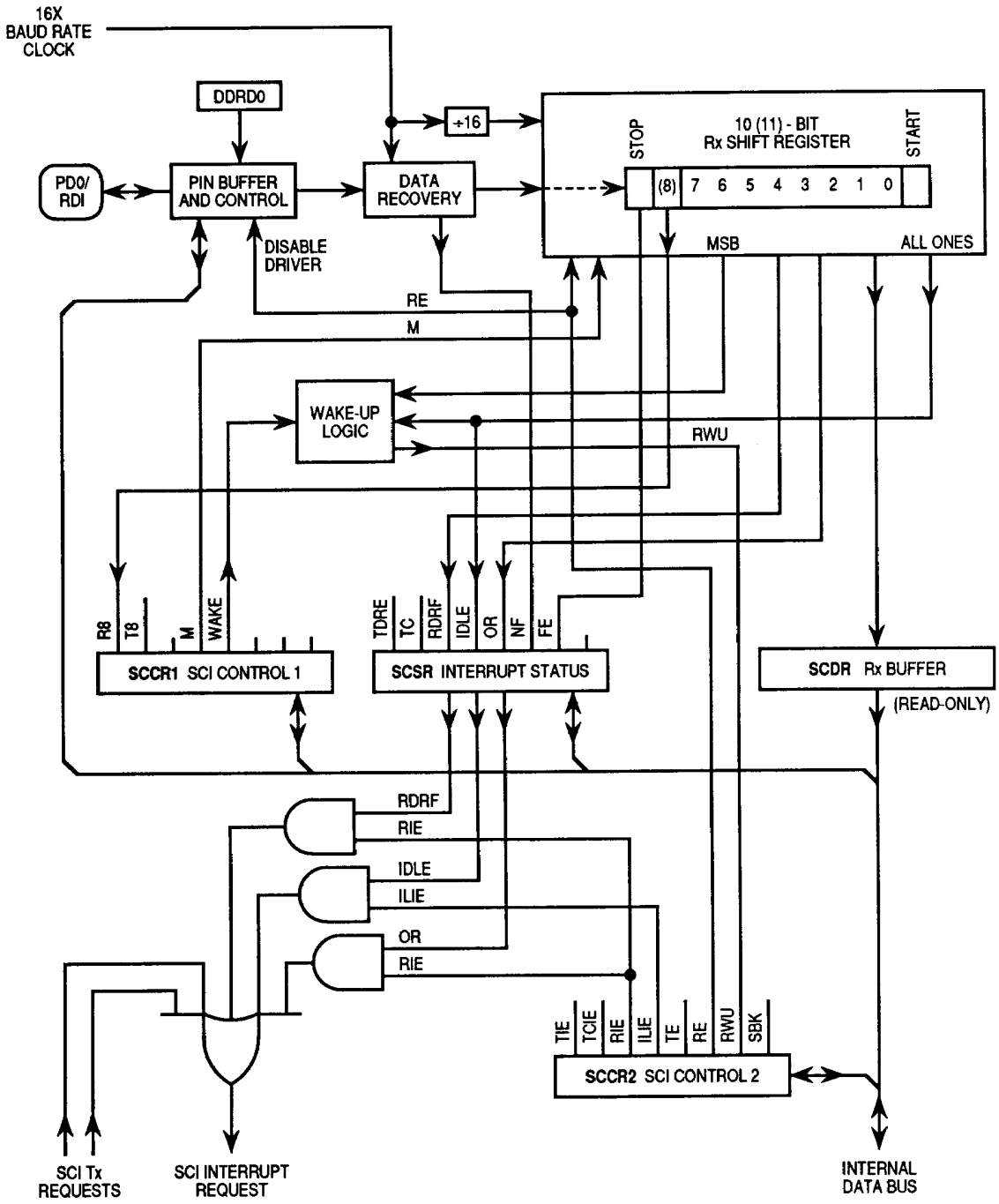


SPI System Block Diagram

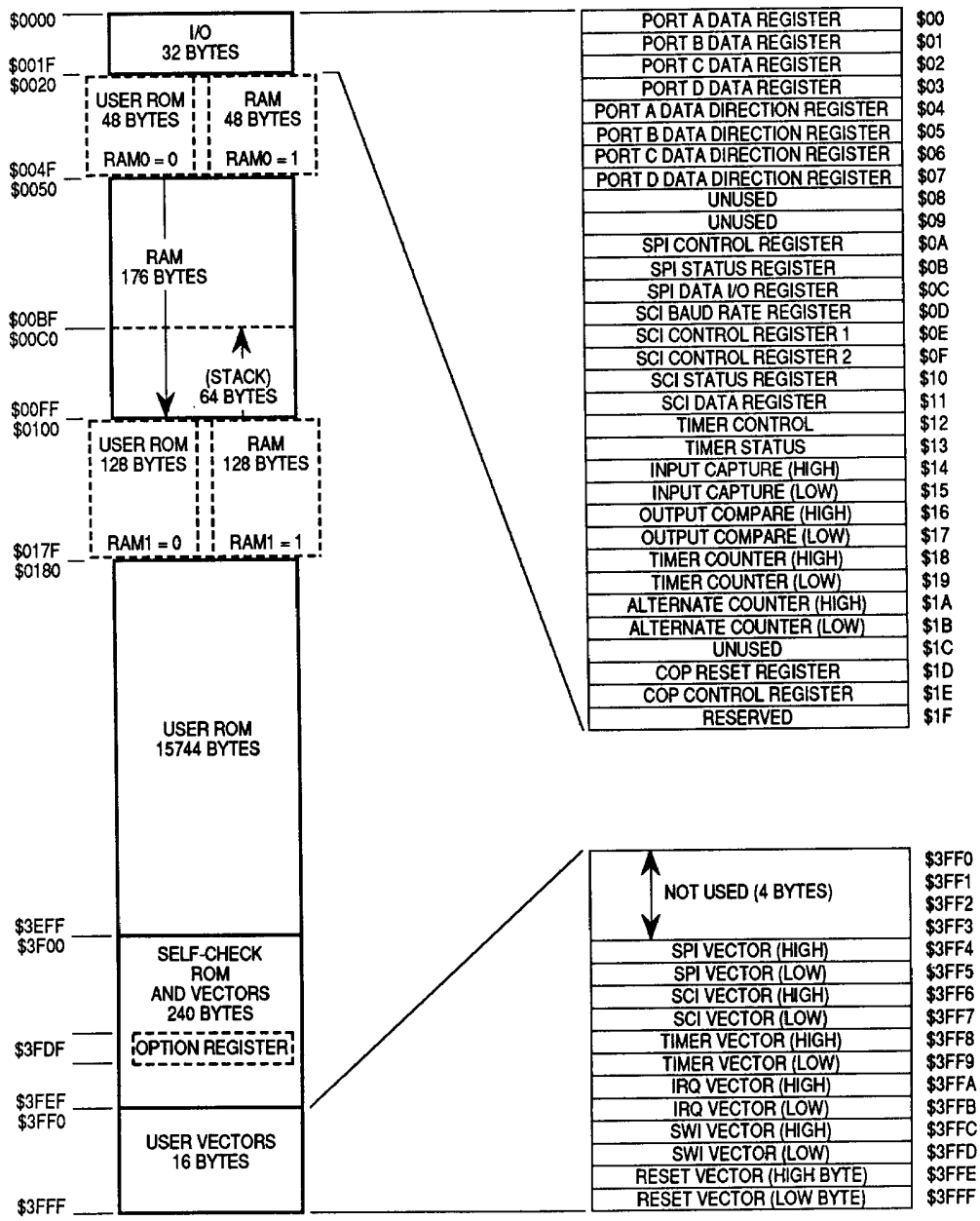
The SCI is a full-duplex asynchronous system, using standard nonreturn-to-zero (NRZ) format and a variety of baud rates. An on-chip baud-rate generator derives standard buad-rate frequencies from the MCU oscillator. Both the transmitter and receiver are double buffered; thus, back-to-back characters can be handled easily, even if the central processing unit (CPU) is delayed in responding to the completion of an individual character. The SCI transmitter and receiver are functionally independent but use the same data format and baud rate.



SCI Transmitter Block Diagram



SCI Receiver Block Diagram



MC68HC05C9 Memory Map

MC68HC05C9 Register and Control Bit Summary

	Bit-7	6	5	4	3	2	1	Bit-0	
$0000	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PORT A
	4/5	5/6	6/7	7/8	8/9	9/10	10/11	11/12	Port A Pin # (Ref.) DIP/PLCC
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A Pin Names (Ref.)
$0001	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PORT B
	19/21	18/20	17/19	16/18	15/16	14/15	13/14	12/13	Port B Pin # (Ref.) DIP/PLCC
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	Port B Pin Names (Ref.)
$0002	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PORT C
	21/24	22/24	23/25	24/27	25/28	26/29	27/30	28/31	Port C Pin # (Ref.) DIP/PLCC
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Port C Pin Names (Ref.)
$0003	I/O	—	I/O	I/O	I/O	I/O	I/O	I/O	PORT D
	36/40	—	34/37	33/36	32/35	31/34	30/33	29/32	Port D Pin # (Ref.) DIP/PLCC
	PD7	—	PD5/ $\overline{SS}$	PD4/ SCK	PD3/ MOSI	PD2/ MISO	PD1/ TDO	PD0/ RDI	Port D Pin Names (Ref.)
$0004	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	DDRA
$0005	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	DDRB
$0006	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	DDRC
$0007	DDRD7	—	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	DDRD
$0008									Unused
$0009									Unused
$000A	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$000B	SPIF	WCOL	—	MODF	—	—	—	—	SPSR
$000C	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0	SPDR
$000D	—	—	SCP1	SCP0	—	SCR2	SCR1	SCR0	BAUD
$000E	R8	T8	—	M	WAKE	—	—	—	SCCR1
$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE	—	SCSR
$0011	SCD7	SCD6	SCD5	SCD4	SCD3	SCD2	SCD1	SCD0	SCDAT
$0012	ICIE	OCIE	TOIE	—	—	—	IEDG	OLVL	TCR
$0013	ICF	OCF	TOF	—	—	—	—	—	TSR
$0014	Bit-15	14	13	12	11	10	9	Bit-8	ICR (High)
$0015	Bit-7	6	5	4	3	2	1	Bit-0	ICR (Low)
$0016	Bit-15	14	13	12	11	10	9	Bit-8	OCR (High)
$0017	Bit-7	6	5	4	3	2	1	Bit-0	OCR (Low)
$0018	Bit-15	14	13	12	11	10	9	Bit-8	TCNT (High)
$0019	Bit-7	6	5	4	3	2	1	Bit-0	TCNT (Low)
$001A	Bit-15	14	13	12	11	10	9	Bit-8	ALTCNT (High)
$001B	Bit-7	6	5	4	3	2	1	Bit-0	ALTCNT (Low)
$001C									Unused
$001D									COPRST
$001E	—	—	—	COPF	CME	COPE	CM1	CM0	COPCR
$001F									Reserved
$3FDF	RAM0	RAM1	0	0	0	0	IRQ	0	OPTION

ALTCNT — Alternate Timer Count Register

(Same as TCNT register except automatic flag clearing sequences are not triggered.)

Bit-7	6	5	4	3	2	1	Bit-0	
Bit-15	14	13	12	11	10	9	Bit-8	$1A ALTCNT (HIGH)
Bit-7	6	5	4	3	2	1	Bit-0	$1B ALTCNT (LOW)
RESET TO $FFFC								RESET CONDITION

Low byte may be read at any time. Reading the high byte causes the low-byte value to be latched until the low-byte address is read. Counting is not affected by this latching mechanism. Writes have no effect.

BAUD — Baud-Rate Register

Bit-7	6	5	4	3	2	1	Bit-0	
—	—	SCP1	SCP0	—	SCR2	SCR1	SCR0	$0D BAUD
—	—	0	0	—	U	U	U	RESET CONDITION

The baud-rate register is used to select the SCI transmitter and receiver baud rate. SCP1 and SCP0 prescaler bits are used in conjunction with the SCR2–SCR0 baud-rate bits to provide multiple baud-rate combinations for a given crystal frequency.

SCP1 — SCI Prescaler Bit-1

SCP0 — SCI Prescaler Bit-0

The two SCI prescaler bits define the value by which the internal clock frequency is divided. The SCR2–SCR0 then uses the prescaler value to determine baud rate. Prescaler internal clock division versus bit levels are listed in the table below.

SCP1	SCP0	Clock Divided By	Crystal Frequency MHz		
			4.194304	4.0	2.0
0	0	1	131.072 kHz	125.000 kHz	62.50 kHz
0	1	3	43.691 kHz	41.666 kHz	20.833 kHz
1	0	4	32.768 kHz	31.250 kHz	15.625 kHz
1	1	13	10.082 kHz	9600 Hz	4800 Hz

SCR2 — SCI Baud Rate Bit-2

SCR1 — SCI Baud Rate Bit-1

SCR0 — SCI Baud Rate Bit-0

The three SCI baud-rate bits define the value used to divide the prescaler value. The result is the baud rate of the SCI transmitter and receiver. Baud rates vs bit levels are listed in the table below.

SCR2	SCR1	SCR0	Prescaler Divided By	Prescaler Output		
				131.072 kHz	19.20 kHz	9600 Hz
0	0	0	1	131.072 kbaud	19.20 kbaud	9600 baud
0	0	1	2	65.536 kbaud	9600 kbaud	4800 baud
0	1	0	4	32.768 kbaud	4800 kbaud	2400 baud
0	1	1	8	16.384 kbaud	2400 kbaud	1200 baud
1	0	0	16	8192 baud	1200 kbaud	600 baud
1	0	1	32	4096 baud	600 kbaud	300 baud
1	1	0	64	2048 baud	300 kbaud	150 baud
1	1	1	128	1024 baud	150 kbaud	75 baud

COPCR — COP Control Register

Bit-7	6	5	4	3	2	1	Bit-0	
—	—	—	COPF	CME	COPE	CM1	CM0	$1E COPCR
0	0	0	0	0	0	0	0	RESET CONDITION

COPF — Computer Operating Properly Failure
1 = COP or clock monitor reset has occurred
0 = No COP or clock monitor reset has occurred
After reading the COP control register, COPF is cleared.

CME — Clock Monitor Enable
1 = Clock monitor enabled
0 = Clock monitor disabled
CME is read/write all the time.

COPE — Computer Operating Properly Enable
1 = COP timeout enabled
0 = COP timeout disabled
COPE is readable any time, but can be written only once.

CM1, CM0 — COP Mode Bits
The COP mode bits select one of four timeout durations for the COP timer. CM1 and CM0 are cleared by reset and can only be written once.

CM1	CM0	$F_{OP}/2^{15}$ Divided By	XTAL=4.0 MHZ F_{OP}=2.0 MHZ	XTAL=3.5795 MHZ F_{OP}=1.7897 MHz	XTAL=2.0 MHz F_{OP}=1.0 MHz	XTAL=1.0 MHz F_{OP}=0.5 MHz
0	0	1	16.38 ms	18.31 ms	32.77 ms	65.54 ms
0	1	4	65.54 ms	73.24 ms	131.07 ms	262.14 ms
1	0	16	262.14 ms	292.95 ms	524.29 ms	1.048 s
1	1	64	1.048 s	1.172 s	2.097 s	4.194 s

F_{OP} = Crystal ÷ 2

COPRST — COP Reset Register

Bit-7	6	5	4	3	2	1	Bit-0	
								$1D COPRST
0	0	0	0	0	0	0	0	RESET CONDITION

The sequence required to reset the COP timer is as follows:
1. Write $55 to the COP reset register.
2. Write $AA to the COP reset register.

Both write operations must occur in the order listed, but any number of instructions may be executed between the two write operations. The elapsed time between software resets must not be greater than the COP timeout period as set by the CM1 and CM0 bits. Reading the COP reset register does not return valid data and does not affect the watchdog timer.

DDRA — Data Direction Register for Port A

Bit-7	6	5	4	3	2	1	Bit-0	
DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	$04 DDRA
0	0	0	0	0	0	0	0	RESET CONDITION

DDRB — Data Direction Register for Port B

Bit-7	6	5	4	3	2	1	Bit-0	
DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	$05 DDRB
0	0	0	0	0	0	0	0	RESET CONDITION

DDRC — Data Direction Register for Port C

Bit-7	6	5	4	3	2	1	Bit-0	
DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	$06 DDRC
0	0	0	0	0	0	0	0	RESET CONDITION

DDRD — Data Direction Register for Port D

Bit-7	6	5	4	3	2	1	Bit-0	
DDRD7	—	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	$07 DDRD
0	—	0	0	0	0	0	0	RESET CONDITION

For all DDRx bits, 0 = input and 1 = output.

ICR — Input Capture Register

Bit-7	6	5	4	3	2	1	Bit-0	
Bit-15	14	13	12	11	10	9	Bit-8	$14 ICR (HIGH)
Bit-7	6	5	4	3	2	1	Bit-0	$15 ICR (LOW)
INPUT CAPTURE REGISTER NOT AFFECTED BY RESET								RESET CONDITION

Two 8-bit registers, which make up the 16-bit input capture register, are read-only and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The level of transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value that corresponds to the most recent input capture.

After a read of the input capture register most significant bit (MSB) ($14), the counter transfer is inhibited until the least significant bit (LSB) ($15) is also read.

OCR — Output Compare Register

Bit-7	6	5	4	3	2	1	Bit-0	
Bit-15	14	13	12	11	10	9	Bit-8	$16 OCR (HIGH)
Bit-7	6	5	4	3	2	1	Bit-0	$17 OCR (LOW)
OUTPUT COMPARE REGISTER NOT AFFECTED BY RESET								RESET CONDITION

The 16-bit output compare register is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The output compare register is used for several purposes, such as indicating when a period of time has elapsed. All bits are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

The output compare register contents are compared with the contents of the free-running counter continually, and if a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is transferred to the TCMP pin.

After a processor write cycle to the output compare register containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare function. The free-running counter is updated every four internal bus clock cycles. The minimum time required to update the output compare register is a function of the program rather than the internal hardware.

OPTION — Option Register

Bit-7	6	5	4	3	2	1	Bit-0	
RAM0	RAM1	0	0	0	0	IRQ	0	$3FDF OPTION
0	0	0	0	0	0	1	0	RESET CONDITION

RAM0 — Random Access Memory Control Bit 0

1 = Maps 48 bytes of RAM into page zero starting at address $0020. This replaces 48 bytes of ROM, allowing memory configuration to be changed during program execution.

RAM1 — Random Access Memory Control Bit 1

1 = Maps 128 bytes of RAM into page zero starting at address $0100. This replaces 128 bytes of ROM, allowing memory configuration to be changed during program execution.

IRQ — Interrupt Request

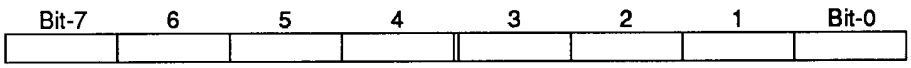
1 = Selects the edge and level of interrupt option.

0 = Select the edge only option

This bit is not readable and can only be written once after reset

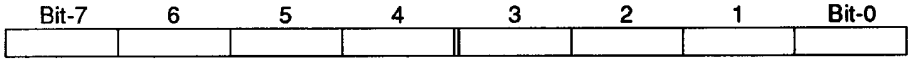
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PORTA — I/O Port A



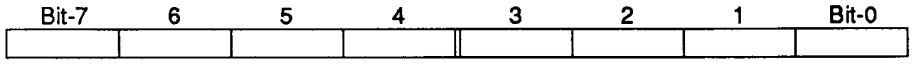
Bit-7	6	5	4	3	2	1	Bit-0	
								$00 PORTA
PORT OUTPUT REGISTER STATES NOT CHANGED BY RESET								RESET CONDITION
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PIN DIRECTIONS (REF.)
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PIN NAMES (REF.)

PORTB — I/O Port B



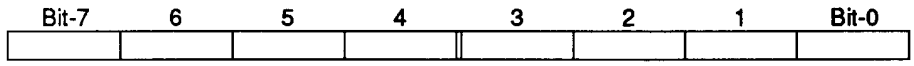
Bit-7	6	5	4	3	2	1	Bit-0	
								$01 PORTB
PORT OUTPUT REGISTER STATES NOT CHANGED BY RESET								RESET CONDITION
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PIN DIRECTIONS (REF.)
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PIN NAMES (REF.)

PORTC — I/O Port C



Bit-7	6	5	4	3	2	1	Bit-0	
								$02 PORTC
PORT OUTPUT REGISTER STATES NOT CHANGED BY RESET								RESET CONDITION
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PIN DIRECTIONS (REF.)
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PIN NAMES (REF.)

PORTD — I/O Port D



Bit-7	6	5	4	3	2	1	Bit-0	
								$03 PORTD
PORT OUTPUT REGISTER STATES NOT CHANGED BY RESET								RESET CONDITION
I/O	—	I/O	I/O	I/O	I/O	I/O	I/O	PIN DIRECTIONS (REF.)
PD7	—	PD5	PD4	PD3	PD2	PD1	PD0	PIN NAMES (REF.)
—	—	$\overline{SS}$	SCK	MOSI	MISO	TDO	RDI	ALT. PIN NAMES (REF.)

SCCR1 — Serial Communication Control Register 1

Bit-7	6	5	4	3	2	1	Bit-0	
R8	T8	—	M	WAKE	—	—	—	$0E SCCR1
U	U	—	U	U	—	—	—	RESET CONDITION

The SCCR1 provides control bits which determine word length and select the wakeup method.

R8 — Receive Data Bit-8
R8 bit provides storage location for the ninth bit in the receive data character (if M = 1).

T8 — Transmit Data Bit-8
T8 bit provides storage location for the ninth bit in the transmit data character (if M = 1).

Bits 5 and 2–0 — Not used; can read either one or zero

M — SCI Character Word Length
1 = one start bit, nine data bits, one stop bit
0 = one start bit, eight data bits, one stop bit

WAKE — Wakeup Select
Wake bit selects the receiver wakeup method. (See also RWU in SCCR2.)
1 = Address bit (most significant bit)
0 = Idle line condition

SCCR2 — Serial Communication Control Register 2

Bit-7	6	5	4	3	2	1	Bit-0	
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$0F SCCR2
0	0	0	0	0	0	0	0	RESET CONDITION

The SCCR2 provides control of individual SCI functions such as interrupts, transmit/receive enabling, receiver wakeup, and send break code.

TIE — Transmit Interrupt Enable
1 = SCI interrupt enabled
0 = TDRE interrupt disabled

TCIE — Transmit Complete Interrupt Enable
1 = SCI interrupt enabled
0 = TC interrupt disabled

RIE — Receive Interrupt Enable
1 = SCI interrupt enabled
0 = RDRF and OR interrupts disabled

ILIE — Idle Line Interrupt Enable

1 = SCI interrupt enabled

0 = Idle interrupt disabled

TE — Transmit Enable

1 = Transmit shift register output is applied to the TDO line. Depending upon the SCCR1 M bit, a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted.

0 = Transmitter disabled at the next character boundary. After last byte is transmitted, TDO (PD1) line becomes a general-purpose I/O line.

RE — Receive Enable

1 = Receiver shift register input is applied to the RDI line.

0 = Receiver disabled and RDRF, IDLE, OR, NF, and FE status bits are inhibited. RDI (PD0) becomes a general-purpose I/O line.

RWU — Receiver Wakeup

1 = Places receiver in sleep mode and enables wakeup function.

0 = If the WAKE bit = 1, the RWU bit is cleared after receiving a data word with the MSB set. If WAKE = 0, the RWU bit is cleared after receiving 10 (M = 0) or 11 (M = 11) consecutive ones.

SBK — Send Break

1 = Transmitter continually sends blocks of zeros (sets of 10 or 11) until cleared. Upon completion of break condition, transmitter sends one high bit for recognition of valid start bit.

0 = Transmitter configured for normal SCI communication. If transmitter is empty and idle, setting and clearing the SBK bit may queue up to two character times of break because the first break can transfer almost immediately to the shift register, and the second is queued into the parallel transmit buffer.

SCDAT — Serial Communications Data Register

Bit-7	6	5	4	3	2	1	Bit-0	
SCD7	SCD6	SCD5	SCD4	SCD3	SCD2	SCD1	SCD0	$11 SCDAT
U	U	U	U	U	U	U	U	RESET CONDITION

SCDAT functions as two separate registers. Transmit data register (TDR) provides the parallel interface from the internal data bus to the transmit shift register. Receive data register (RDR) provides interface from the receive shift register to the internal data bus. SCI data is double buffered in both directions

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SCSR — Serial Communication Status Register

Bit-7	6	5	4	3	2	1	Bit-0	
TDRE	TC	RDRF	IDLE	OR	NF	FE	—	$10 SCSR
0	0	0	0	0	0	0	—	RESET CONDITION

The SCSR provides inputs to the SCI interrupt logic circuits. Noise flag and framing error bits are also contained in the SCSR.

TDRE — Transmit Data Register Empty Flag
Set if transmit data may be written to SCDR; if TDRE = 0, transmit data register is busy.
Cleared by SCSR1 read with TDRE set, followed by SCDR write.

TC — Transmit Complete Flag
Set if transmitter is idle (no data, preamble, or break transmission in progress).
Cleared by SCSR1 read with TC set, followed by SCDR write.

RDRF — Receive Data Register Full Flag
Set if a received character is ready to be read from SCDR.
Cleared by SCSR1 read with RDRF set, followed by SCDR read.

IDLE — Idle Line Detected Flag
Set if the RxD line is idle.
Cleared by SCSR1 read with IDLE set, followed by SCDR read.
Once cleared, IDLE will not be set again until the RxD line has been active and becomes idle again.

OR — Overrun Error Flag
Set if a new character is received before a previously received character is read from SCDR.
Cleared by SCSR1 read with OR set, followed by SCDR read.

NF — Noise Error Flag
Set if majority sample logic detects anything other than a unanimous decision.
Cleared by SCSR1 read with NF set, followed by SCDR read.

FE — Framing Error
Set if a 0 is detected where a stop bit was expected.
Cleared by SCSR1 read with FE set, followed by SCDR read.

Bit-0 — Not used; can read either one or zero.

SPCR — SPI Control Register

Bit-7	6	5	4	3	2	1	Bit-0	
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	$0A SPCR
0	0	0	0	U	U	U	U	RESET CONDITION

SPIE — Serial Peripheral Interrupt Enable
1 = SPI interrupt enabled
0 = SPI interrupt disabled

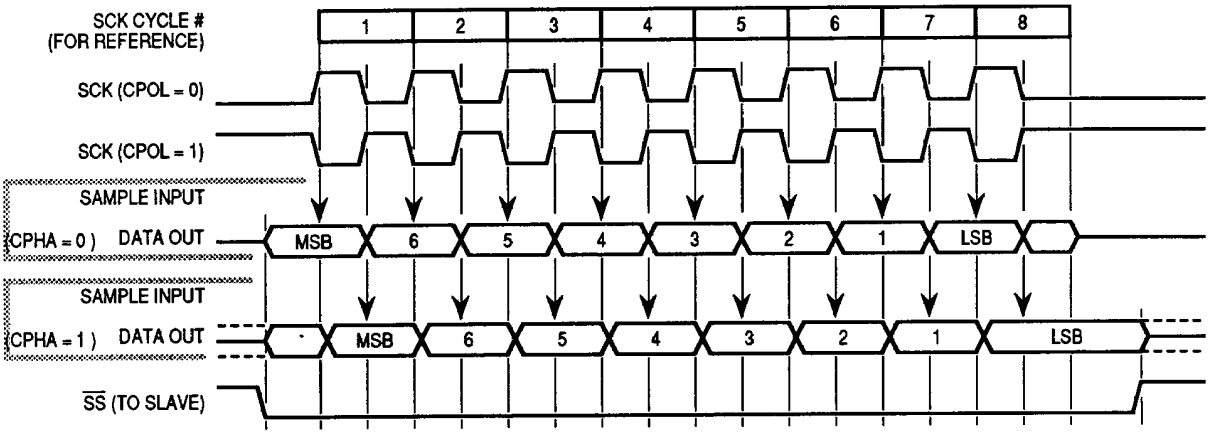
SPE — Serial Peripheral System Enable
1 = SPI system is on.
0 = SPI system is off; PD5–PD2 become general-purpose I/O lines.

DWOM — Port D Wire-OR Mode Option
This bit affects all seven port D pins.
1 = Port D outputs act as open-drain outputs.
0 = Port D outputs are normal CMOS outputs.

MSTR — Master Mode Select
1 = Master mode
0 = Slave mode

CPOL — Clock Polarity
The CPOL controls the clock value and is used in conjunction with the clock phase (CPHA) bit.
1 = SCK line idles high.
0 = SCK line idles low.

CPHA — Clock Phase
Clock phase bit along with CPOL controls the clock-data relationship between the master and slave devices. CPHA selects one of two fundamentally different clocking protocols.
1 = $\overline{SS}$ is an output enable control.
0 = Shift clock is the OR of SCK with $\overline{SS}$. When $\overline{SS}$ is low, first edge of SCK invokes first data sample.



SPR1, SPR0 — SPI Clock Rate Bits

Two clock rate bits are used to select one of four clock rates to be used as SCK in the master mode. In the slave mode, the two clock rate bits have no effect.

SPR1	SPR0	Internal Processor Clock* Divided By
0	0	2
0	1	4
1	0	16
1	1	32

*Internal processor clock equals f_{OSC} divided by two.

SPDR — SPI Data Register

Bit-7	6	5	4	3	2	1	Bit-0	
SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0	$0C SPDR
U	U	U	U	U	U	U	U	RESET CONDITION

A write to the SPDR places data directly into the shift register for transmission. Only a write to the SPDR register of the master SPI device will initiate the transmission/reception of a byte. On completion of the byte transmission, the SPIF status bit is set in both master and slave devices.

A read to the SPCR causes the buffer to be read. The SPIF status bit must be cleared by the time a new data transfer finishes and data is transferred from the shift register to the read buffer, or an overrun condition will exist. In overrun cases, the new byte is written into the read buffer, whether the previous data was read are not.

SPSR — SPI Status Register

Bit-7	6	5	4	3	2	1	Bit-0	
SPIF	WCOL	—	MODF	—	—	—	—	$0B SPSR
0	0	0	0	—	—	—	—	RESET CONDITION

SPIF — SPI Transfer Complete Flag

Set when an SPI transfer is complete.
Cleared by reading SPSR with SPIF set, followed by SPDR access.

WCOL — Write Collision

Set when SPDR is written while transfer is in progress.
Cleared by SPSR with WCOL set, followed by SPDR access.

MODF — Mode Fault (A Mode Fault Terminates SPI Operation)

Set when $\overline{SS}$ is pulled low while MSTR = 1.
Cleared by SPCR read with MODF set, followed by SPCR write.

Bits 5 and 3–0 — Not used

TCNT — Timer Count Register

Bit-7	6	5	4	3	2	1	Bit-0	
Bit-15	14	13	12	11	10	9	Bit-8	$18 TCNT (HIGH)
Bit-7	6	5	4	3	2	1	Bit-0	$19 TCNT (LOW)
RESET TO $FFFC								RESET CONDITION

Free-running 16-bit counter. Low byte may be read at any time. Reading high byte causes low byte to be latched until the low byte is read. Counting is not affected by this latching mechanism. Writes have no meaning or effect.

TCR — Timer Control Register

Bit-7	6	5	4	3	2	1	Bit-0	
ICIE	OCIE	TOIE	—	—	—	IEDG	OLVL	$12 TCR
U	U	U	—	—	—	0	0	RESET CONDITION

ICIE — Input Capture Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

OCIE — Output Compare Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

TOIE — Timer Overflow Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

IEDG — Input Edge
Value of input edge determines which level of transition on TCAP pin will trigger free-running counter transfer to the input capture register.
1 = Positive edge
0 = Negative edge
Reset does not affect the IEDG bit.

OLVL — Output Level
Value of output level is transferred to the TCMP pin at the next successful output compare.
1 = High output
0 = Low output

Bits 4, 3, and 2 — Not used

TSR — Timer Status Register

Bit-7	6	5	4	3	2	1	Bit-0	
ICF	OCF	TOF	—	—	—	—	—	$13 TSR
U	U	U	—	—	—	—	—	RESET CONDITION

ICF — Input Capture Flag

1 = Flag set when selected polarity edge is sensed by input capture edge detector.

0 = When the TSR and then input capture low register ($0015) are accessed, the flag is cleared.

OCF — Output Compare Flag

1 = Flag set when output compare register contents match the free-running counter contents.

0 - When the TSR and output compare low register ($0017) are accessed, the flag is cleared.

TOF — Timer Overflow Flag

1 = Flag set when free-running counter transition from $FFFF to $0000 occurs.

0 = When the TSR and counter low register ($0019) are accessed, the flag is cleared.

Bits 4–0 — Not used

Accessing the TSR satisfies the first condition required to clear status bits. The remaining step is to access the register corresponding to the status bit.