TDA10046HT

Single-chip DVB-T channel decoder

Delivering a low cost system solution for DVB-T channel decoding, the TDA10046HT single chip channel decoder demonstrates Philips Semiconductors' continuing leader-ship in digital broadcast reception, offering advanced features such as adaptive echo cancellation, fast channel scanning and a unique 'Pulse Killer' algorithm that reduces impulsive noise disturbances.

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The TDA10046HT performs all DVB-T channel decoding functions from IF input to transport stream output, using an internal DSP core for synchronization and control.Thanks to its sharp adjacent channel digital ilter, this single-chip receiver achieves excellent performance with low cost tuners (one SAW only). It requires only a low cost crystal oscillator (4 MHz) as a clock source, which can be shared with the tuner. After sampling of the 1st or 2nd IF by a 10-bit ADC, the signal is converted to baseband and passes through the FFT demodulator. Channel frequency response is then estimated and iltered in both time and frequency domains, and used to equalize the signal. A common phase error correction handles tuner phase noise.

The TDA10046HT implements a number of advanced features including a high-performance 'Pulse Killer' algorithm to reduce the disturbing effects of short and strong impulsive noise interference caused by electrical domestic devices and/or car trafic. For maximum ease of use, the TDA10046HT features fully automatic transmission parameters detection, ultra fast scan of the whole UHF/VHF band, and fast zapping facilities.

Evaluation boards are available with most commercial tuners.They are provided with all the necessary software including a tailored Graphical User Interface (GUI) that allows easy evaluation and development.

Key features

- 2K and 8K COFDM demodulator, fully ETS 300-744 compliant
- TPS and Cell Identiier^{2}I C-bus readable
- 2nd or 1st IF analog input
- On chip 10-bit ADC and PLL
- Single or dual AGC loop (with programmable takeover point)
- Adjacent channel digital iltering (only one external SAW ilter is required)
- Automatic frequency offset detection (±1, 2 or 3 standard offsets)
- Dynamic FFT window positioning, and adaptive echo equalization
- Consolidated algorithm for impulsive noise reduction
- DSP based synchronization enables on the ly irmware upgrades
- No extra-host software required
- Fast UHF/VHF band scanning
- Simultaneous tri-state parallel and serial Transport Stream interfaces
- 4 GPIO pins with ΣΔ
- I^{2}C-bus interface
- 5V tolerant I/O pins
- Low power consumption (450mW)
- TQFP64 package, CMOS 0.18 µm technology

modulator

Applications

- Integrated Digital TV (iDTV)
- Set-Top-Boxes (STB)
- Personal Video Recorder (PVR) with DVB-T reception
- Digital TV PCI card for Personal Computers

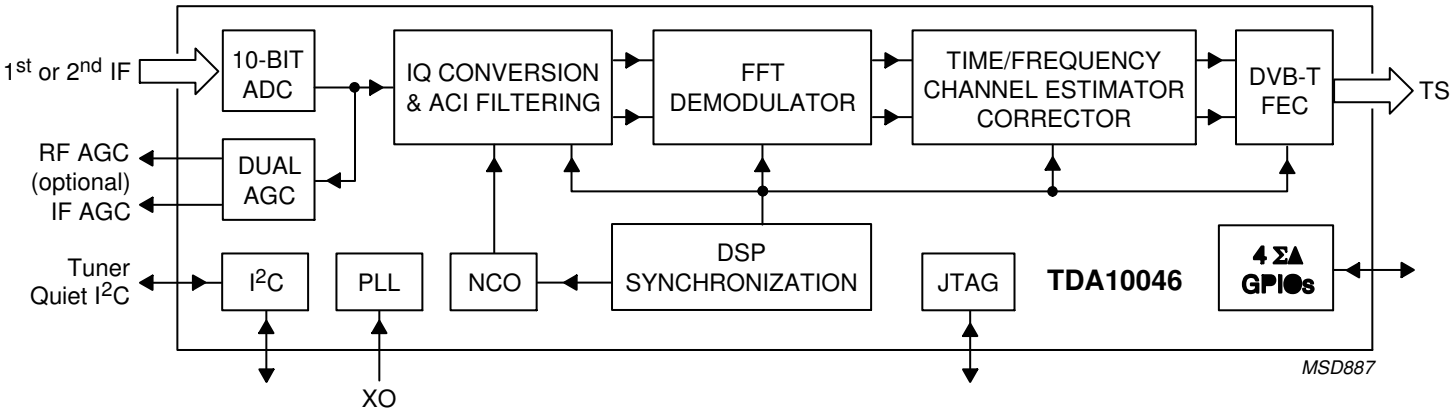
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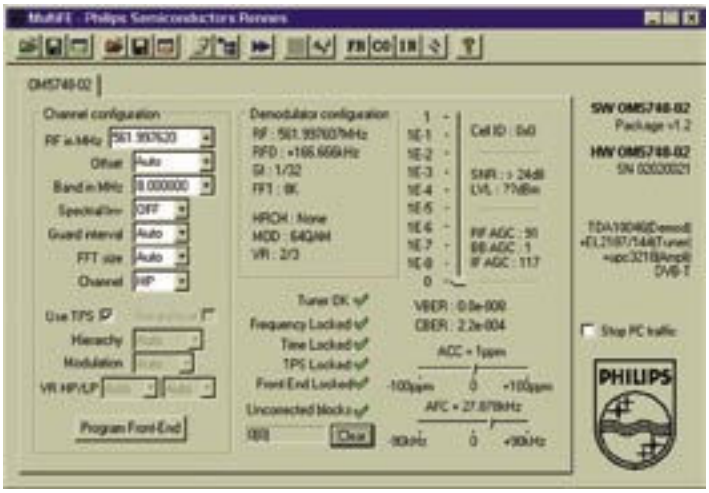
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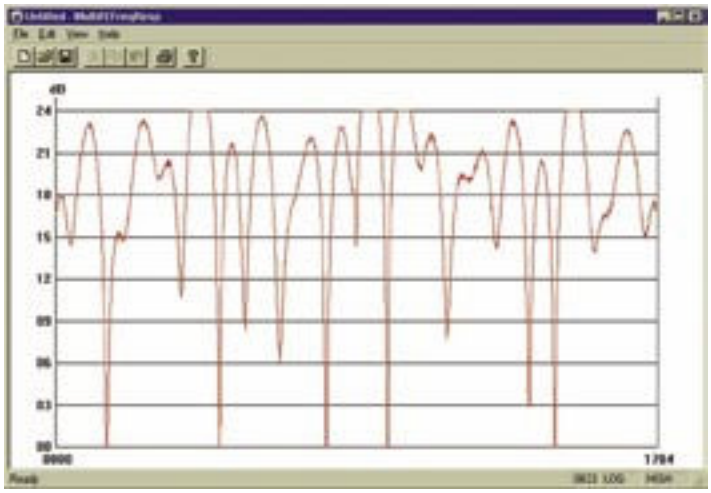


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Evaluation software with Graphical User Interface



Channel frequency response

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