2 GHz to 67 GHz, 500 MHz Bandwidth Envelope Detector

Data Sheet **ADL6012**

FEATURES

- Over 500 MHz wide envelope bandwidth
- Fast response times
  - 0.6 ns output rise time
  - 1.3 ns fall time from 10 dBm to no RF input
  - 0.5 ns output propagation delay (rising edge)
  - 1.3 ns propagation delay at 10 dBm (falling edge)
- Broadband 50 Ω input impedance
- Flat frequency response with minimal slope variation
  - ±1 dB error up to 43.5 GHz
- Input range of −25 dBm to +15 dBm up to 43.5 GHz
- Quasi differential 100 Ω output interface suitable to drive 100 Ω differential load
- Adjustable output common-mode voltage
- Flexible supply voltage: 3.15 V to 5.25 V
- 3 mm × 2 mm, 10-lead LFCSP

APPLICATIONS

- Envelope tracking
- Microwave point to point links
- Microwave instrumentation
- Military radios
- Pulse radar receivers
- Wideband power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

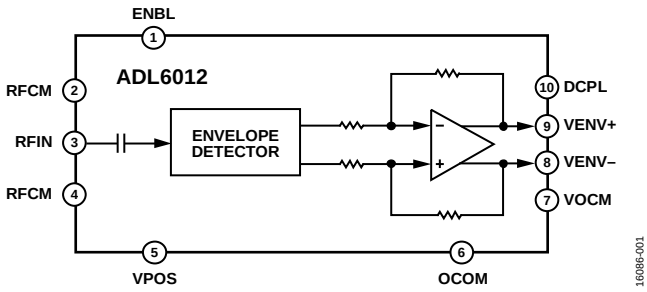


Figure 1.

GENERAL DESCRIPTION

The ADL6012 is a versatile, broadband envelope detector that operates from 2 GHz to 67 GHz. The combination of a wide, 500 MHz envelope bandwidth and a fast, 0.6 ns rise time makes the device suitable for a wide range of applications, including wideband envelope tracking, transmitter local oscillator (LO) leakage corrections, and high resolution pulse (radar) detection.

The response of the ADL6012 is stable over a wide frequency range and features excellent temperature stability. Enabled by propriety technology, the device independently detects the positive and the negative envelopes of the RF input. Even order distortion at the RF input due to nonlinear source loading is also reduced when compared to classic diode detector architectures.

The quasi differential output interface formed by the VENV+ and VENV− pins has a matched, 100 Ω differential output impedance designed to drive a 100 Ω differential load and up to 2 pF of capacitance to ground on each output. The output interface provides the detected and amplified positive and negative envelopes, which are level shifted using an externally applied voltage to the VOCM interface. This configuration simplifies interfacing to a high speed analog-to-digital converter (ADC).

The ADL6012 is specified for operation from −55°C to +125°C, and is available in a 10-lead, 3 mm × 2 mm LFCSP.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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Technical Support www.analog.com

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REVISION HISTORY

5/2020—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 5.0 V, ENBL = 5.0 V, VOCM = 2.5 V, case temperature (T_C) = 25°C, continuous wave (CW) input, 50 Ω source impedance, input power (P_{IN}) = 10 dBm, RF frequency (f_{RF}) = 18 GHz, unless otherwise noted. Envelope outputs are with a differential, open load, unless otherwise noted. See Figure 68 for the schematic.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE	RFIN (Pin 3)				
Operating Frequency Range		2		67	GHz
Operating Input Power Range		−25		+15	dBm
Input Return Loss	Reference characteristic impedance (Z_O) = 50 Ω		10		dB
DETECTOR RESPONSE	RFIN to differential VENV± output				
OUTPUT DRIFT vs. TEMPERATURE[1]					
−55°C < T_C < +125°C					
2 GHz			±0.5		dB
5.8 GHz			±0.5		dB
10 GHz			±0.5		dB
18 GHz			±0.5		dB
28 GHz			±0.5		dB
38 GHz			±0.6		dB
40 GHz			±1		dB
43.5 GHz			±1		dB
52 GHz			±1		dB
60 GHz			±1		dB
67 GHz			±1.2		dB
−40°C < T_C < +105°C					
2 GHz			±0.4		dB
5.8 GHz			±0.4		dB
10 GHz			±0.4		dB
18 GHz			±0.4		dB
28 GHz			±0.4		dB
38 GHz			±0.5		dB
40 GHz			±0.9		dB
43.5 GHz			±0.9		dB
52 GHz			±0.8		dB
60 GHz			±0.8		dB
67 GHz			±1.0		dB
DETECTOR GAIN[2]					
2 GHz			1.967		V/V_{PEAK}
5.8 GHz			1.82		V/V_{PEAK}
10 GHz			1.776		V/V_{PEAK}
18 GHz			1.677		V/V_{PEAK}
28 GHz			1.868		V/V_{PEAK}
38 GHz			1.554		V/V_{PEAK}
40 GHz			1.718		V/V_{PEAK}
43.5 GHz			1.799		V/V_{PEAK}
52 GHz			1.095		V/V_{PEAK}
60 GHz			0.505		V/V_{PEAK}
67 GHz			0.294		V/V_{PEAK}

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT INTERCEPT[2]					
2 GHz			−0.266		V
5.8 GHz			−0.167		V
10 GHz			−0.166		V
18 GHz			−0.154		V
28 GHz			−0.161		V
38 GHz			−0.165		V
40 GHz			−0.155		V
43.5 GHz			−0.217		V
52 GHz			−0.177		V
60 GHz			−0.145		V
67 GHz			−0.070		V
DIFFERENTIAL ENVELOPE OUTPUT VOLTAGE	RFIN = 10 dBm				
2 GHz			1.681		V
5.8 GHz			1.681		V
10 GHz			1.604		V
18 GHz			1.519		V
28 GHz			1.706		V
38 GHz			1.383		V
40 GHz			1.577		V
43.5 GHz			1.577		V
52 GHz			0.896		V
60 GHz			0.298		V
67 GHz			0.205		V
ENVELOPE OUTPUT INTERFACE	VENV+ (Pin 8), VENV− (Pin 9)				
Output Impedance	Differential,10 MHz		100//0.3		Ω//pF
Envelope Bandwidth (−3 dB)	100 Ω differential load		500		MHz
Relative Gain[3]					
100 MHz to 500 MHz		−4.3	−3.1		dB
100 MHz to 700 MHz		−8.2	−6.2		dB
Output Rise Time[4]	10% to 90%,100 Ω load		0.6		ns
Output Fall Time[5]	90% to 10%,100 Ω load				
10 dBm to No RF Input			1.3		ns
0 dBm to No RF Input			0.5		ns
−5 dBm to No RF Input			0.4		ns
Output Propagation Delay[6]					
Rising Edge	10 dBm		0.5		ns
Falling Edge	10 dBm		1.3		ns
	5 dBm		1		ns
	−5 dBm		0.5		ns
Common-Mode Voltage Range	Operating input range, VOCM pin	0.9		VPOS/2	V
Common-Mode Voltage[7]	VPOS = 5 V, VOCM is open	2.49	2.51	2.53	V
Minimum Output Common-Mode Voltage	VOCM (Pin 7) = 0.9 V		0.96		V
Maximum Output Common-Mode Voltage	VOCM = 2.625 V		2.65		V
Short-Circuit Output Current	Differential load = 0 Ω, RFIN = 10 dBm		9.7		mA
Differential Output Noise Density	200 MHz, RFIN = 3 GHz		−145		dBm/Hz
Output Offset	No signal at RFIN, differential output (VENV+) − (VENV−)	0	2	4.5	mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOCM INTERFACE	VOCM				
VOCM Input Impedance			10		kΩ
VOCM Input Voltage Range		0.9		2.625	V
Current In to Pin			1.8	3.8	µA
ENBL INPUT	ENBL (Pin 1)				
Logic High Voltage, V_{IH}		1.5			V
Logic Low Voltage, V_{IL}				0.5	V
Input Current	ENBL = 1.5 V		5	50	µA
Turn On Time[8]	RFIN = 10 dBm		200		µs
Turn Off Time[9]			90		ns
POWER SUPPLY	VPOS (Pin 5)				
Operating Supply Voltage		3.15	5.0	5.25	V
Active Supply Current	No signal at RFIN	25.6	28.6	31.7	mA
Shutdown Supply Current	ENBL = 0 V		2	26	µA

[1] Output drift over temperature is relative to 25°C, calculated by Equation 4 in the Applications Information section.
[2] Detector gain is the slope of the best fit straight line obtained by linear regression on the input peak voltage range from 0.2 V to 1.6 V vs. the differential envelope output voltage. Output intercept is the calculated differential envelope output voltage when the input is 0 V, based on the best fit line from linear regression.
[3] Envelope bandwidth relative gain is the delta, in dB, of the VENV± differential output measured relative to 100 MHz.
[4] Output rise time is the time required to change the voltage at the output pin from 10% to 90% of the final value. The input power is stepped from a no RF input to 10 dBm.
[5] Output fall time is the time required to change the voltage at the output pin from 90% to 10% of the initial value. The input power is stepped from a specified power level to a no RF input.
[6] Propagation delay is the delay from a 50% change in RFIN to a 50% change in the output voltage.
[7] Refer to Figure 50 and the Applications Information section to set the output common-mode voltage.
[8] ENBL turn on time is from a 50% change in the voltage on the ENBL pin to 90% of the settled envelope output.
[9] ENBL turn off time is from a 50% change in the voltage on the ENBL pin to a shut off condition in the supply current.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VPOS to OCOM, RFCM)	5.5 V
RFIN Input Signal Power[1]	
Average	20 dBm
Peak	23 dBm
DC Voltage at RF_{IN}, VOCM, ENBL	−0.3 V to VPOS + 0.3 V
Case Operating Temperature Range	
ADL6012ACPZN	−40°C to +105°C
ADL6012SCPZN	−55°C to +125°C
Junction Temperature (T_J)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Guaranteed by design. Not production tested.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal impedance, and θ_{JC} is the junction to case (exposed pad) thermal impedance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}[2]	Unit
CP-10-12	74.69	11.64	°C/W

[1] Thermal impedance simulated value is based on no airflow with the exposed pad soldered to a 4-layer JEDEC board.
[2] θ_{JC} is the thermal impedance from junction to the exposed pad on the underside of the package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

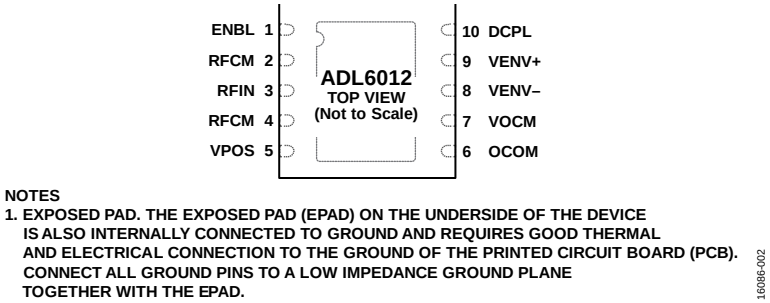


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ENBL	Device Enable. Connect this pin to VPOS to enter an enabled state. Connect this pin to ground to enter a disabled state. This pin can also be driven from a 3 V logic output.
2, 4	RFCM	RF Input Ground Pins. The RFCM pins are connected to the exposed pad (EPAD) at the bottom of the package. Connect the RFCM pins to the system ground using a low impedance ground plane together with the EPAD.
3	RFIN	Signal Input. The RFIN pin is ac-coupled and has a nominal 100 Ω RF input impedance.
5	VPOS	Supply Voltage. The operational range of this pin is from 3.15 V to 5.25 V. Decouple the power supply using suggested capacitor values of 100 pF and 0.1 µF and place these capacitors as close as possible to the VPOS pin.
6	OCOM	Output Common. Connect this pin to a low impedance ground plane together with the EPAD.
7	VOCM	Output Common-Mode Control Input. This pin is internally biased to VPOS/2, nominal. An acceptable range on this pin is 0.9 V to VPOS/2.
8, 9	VENV–, VENV+	Envelope Detector Pseudo Differential Outputs. VENV– and VENV+ are the negative and positive outputs, respectively, for the envelope detector output. A 50 Ω output impedance per pin forms a 100 Ω differential output impedance. These pins feature a 100 Ω differential load and a 2 pF to ground per pin drive capability.
10	DCPL	Bypass Pin for an Internal Bias Node. Connect this pin through a 0.1 µF capacitor to ground for best common-mode noise rejection.
	EPAD	Exposed Pad. The exposed pad (EPAD) on the underside of the device is also internally connected to ground and requires good thermal and electrical connection to the ground of the printed circuit board (PCB). Connect all ground pins to a low impedance ground plane together with the EPAD.

TYPICAL PERFORMANCE CHARACTERISTICS

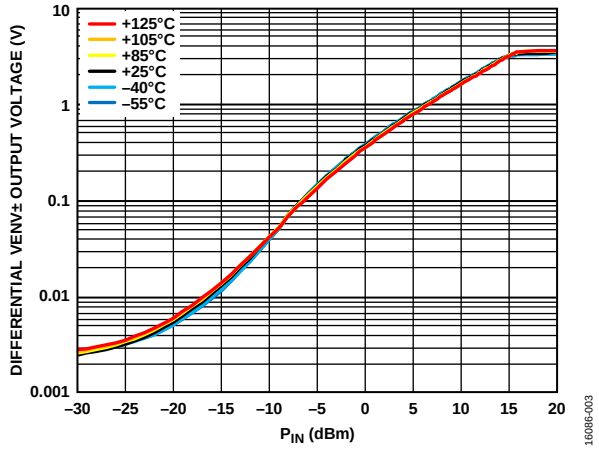


Figure 3. Differential VENV± Output Voltage vs. Input Power (P_{IN}) for Various Temperatures at 2 GHz

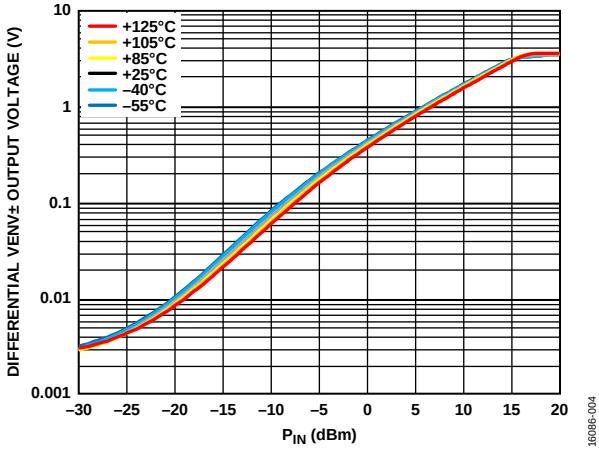


Figure 4. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 5.8 GHz

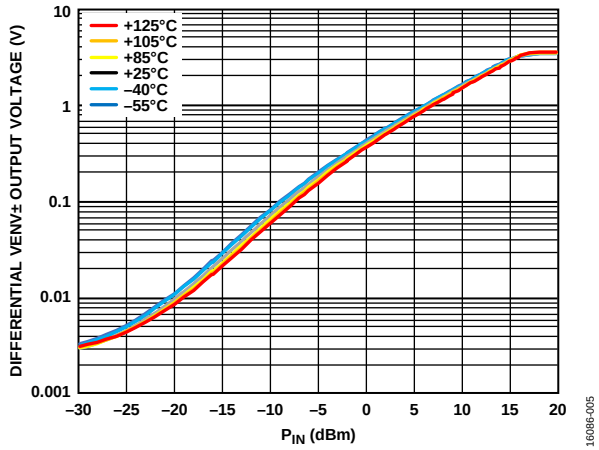


Figure 5. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 10 GHz

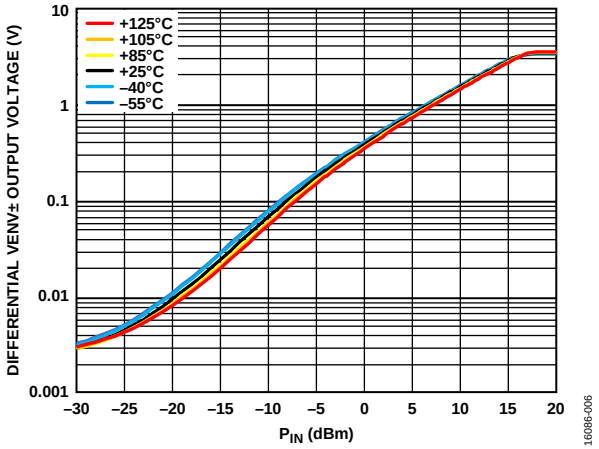


Figure 6. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 18 GHz

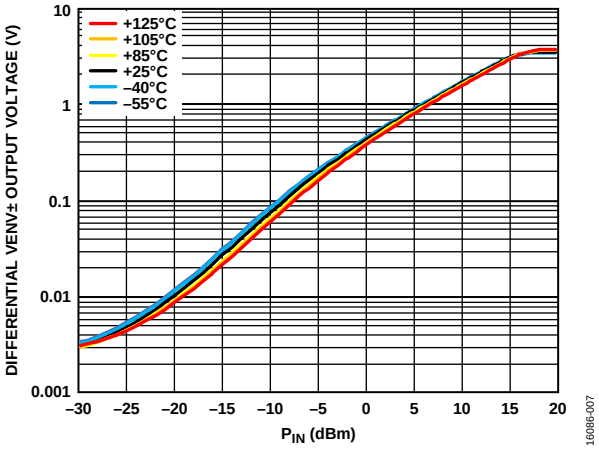


Figure 7. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 28 GHz

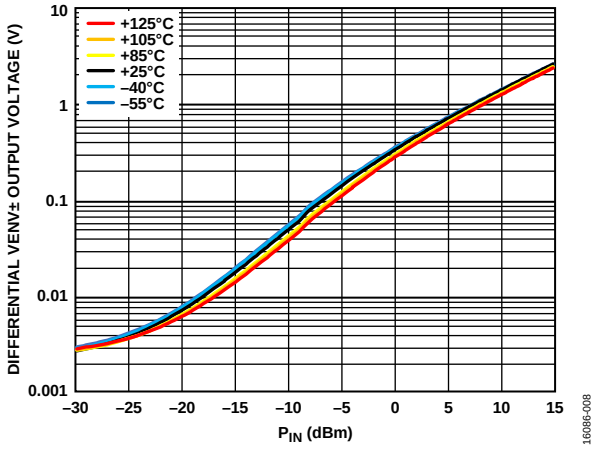


Figure 8. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 38 GHz

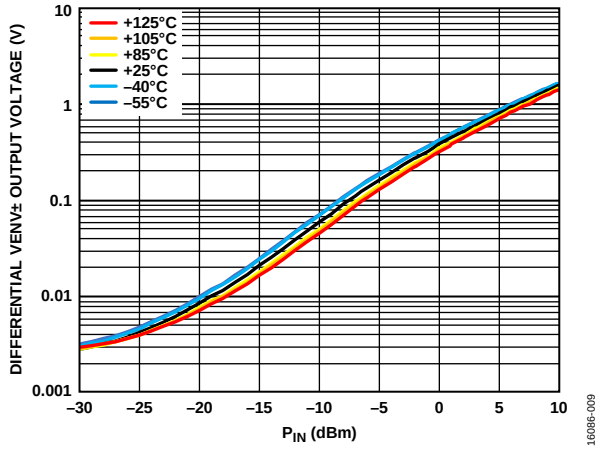


Figure 9. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 40 GHz

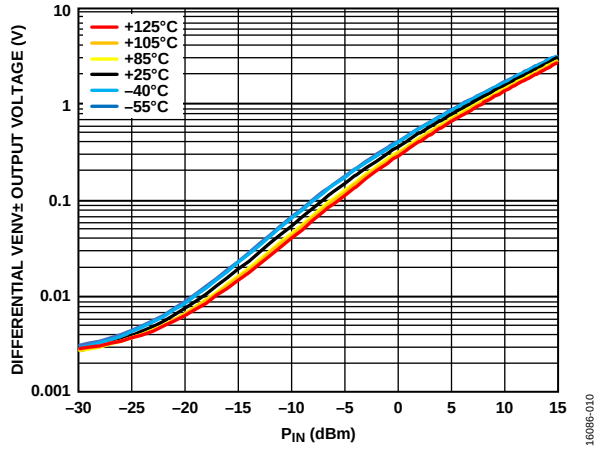


Figure 10. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 43.5 GHz

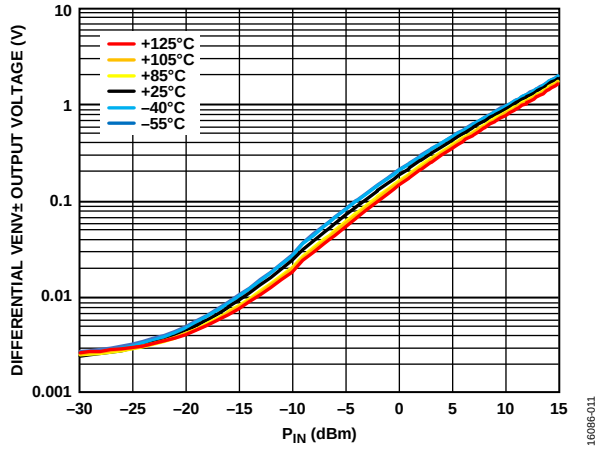


Figure 11. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 52 GHz

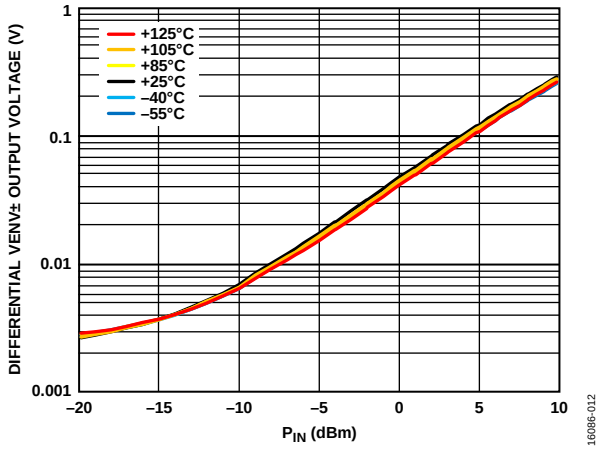


Figure 12. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 60 GHz

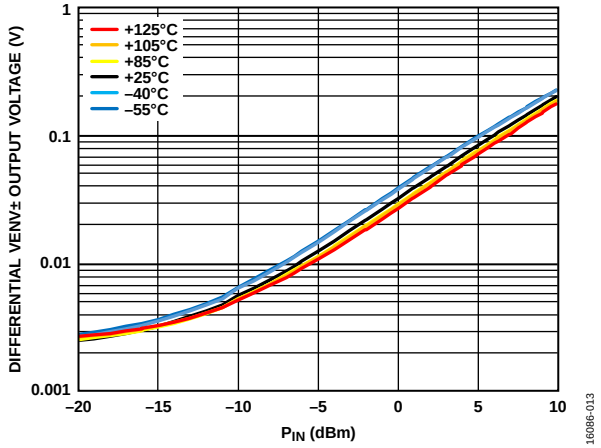


Figure 13. Differential VENV± Output Voltage vs. P_{IN} for Various Temperatures at 67 GHz

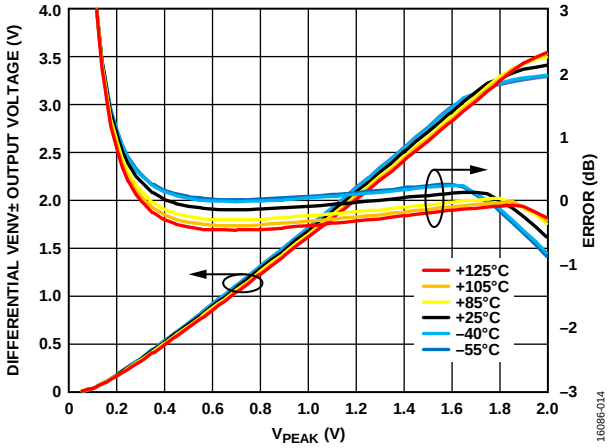


Figure 14. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 2 GHz

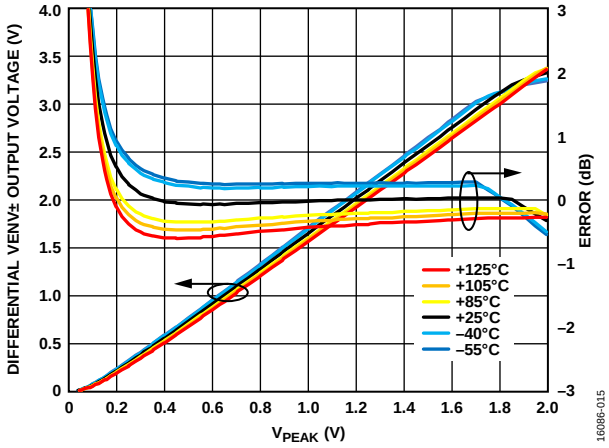


Figure 15. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 5.8 GHz

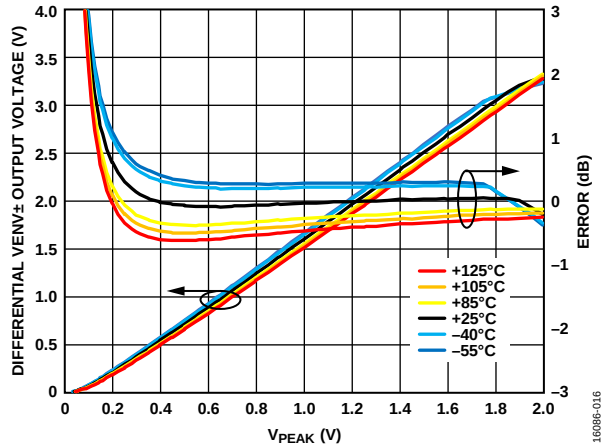


Figure 16. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 10 GHz

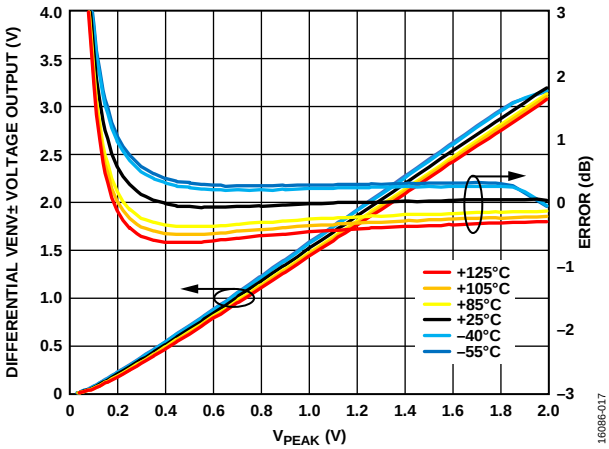


Figure 17. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 18 GHz

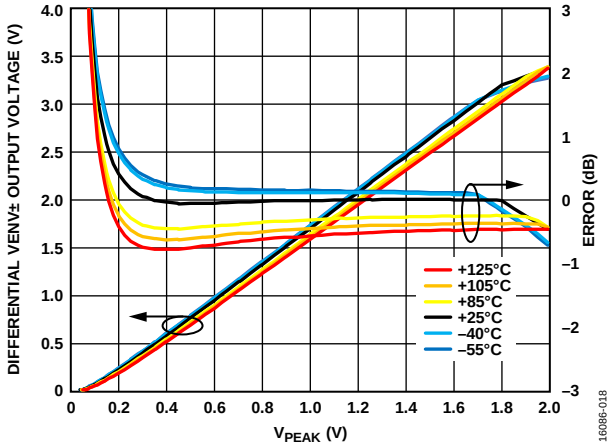


Figure 18. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 28 GHz

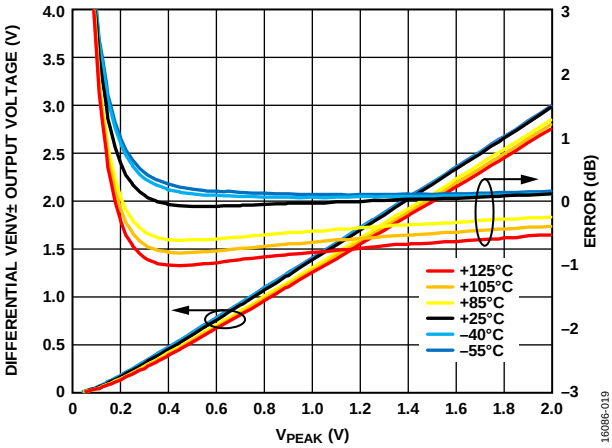


Figure 19. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 38 GHz

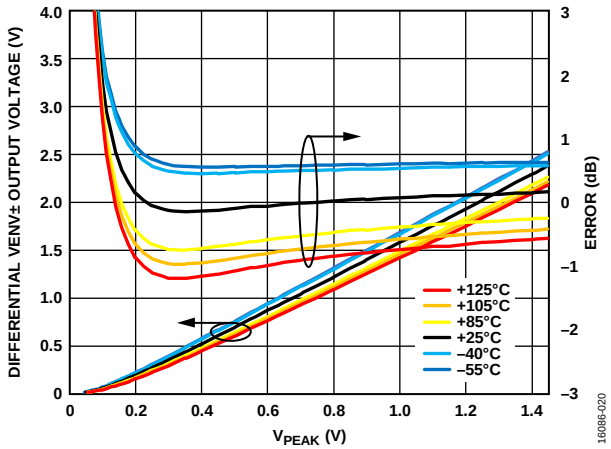


Figure 20. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 40 GHz

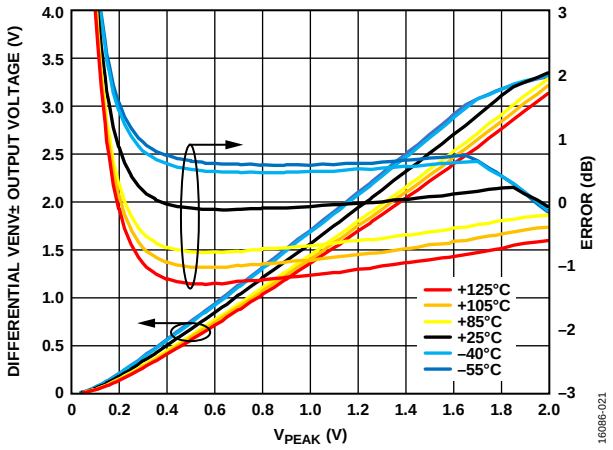


Figure 21. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 43.5 GHz

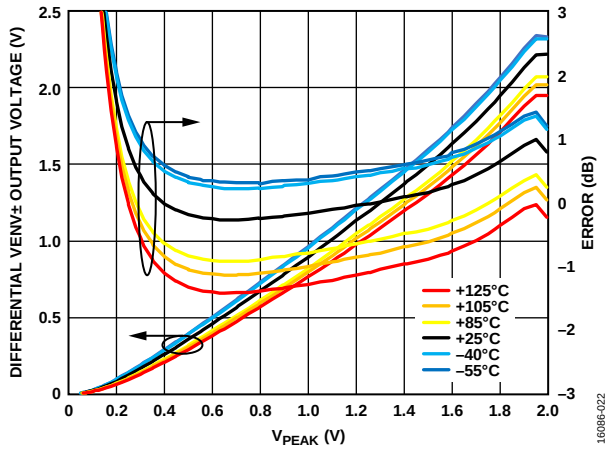


Figure 22. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 52 GHz

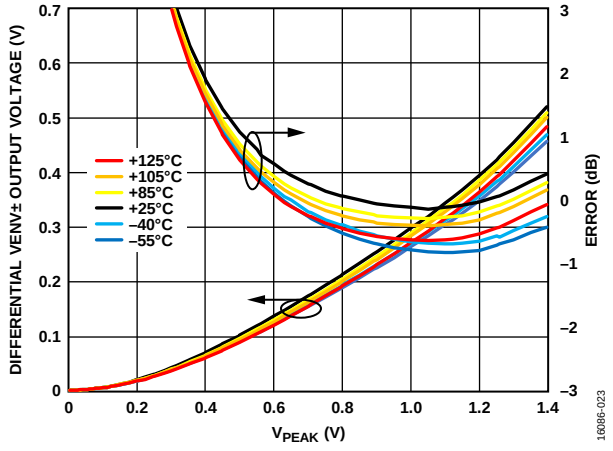


Figure 23. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 60 GHz

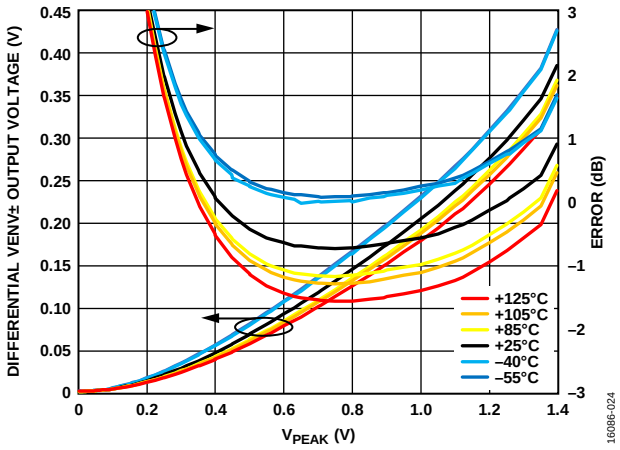


Figure 24. Differential VENV± Output Voltage and Error vs. V_{PEAK} for Various Temperatures at 67 GHz

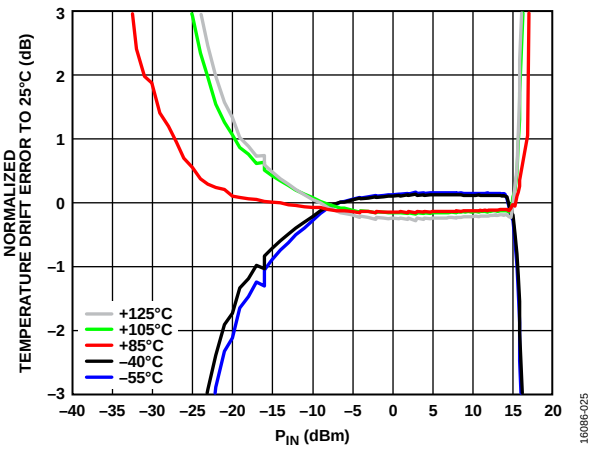


Figure 25. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 2 GHz

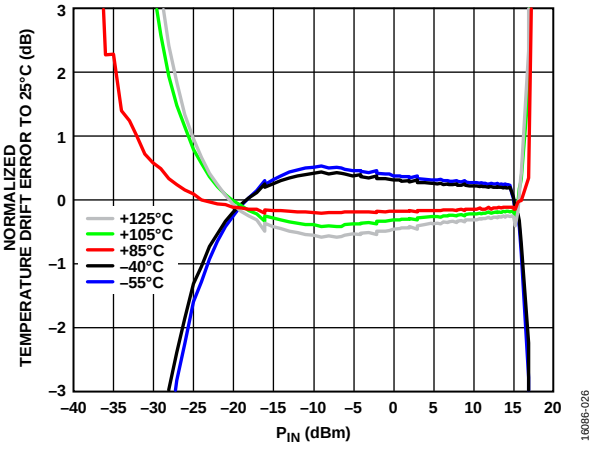


Figure 26. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 5.8 GHz

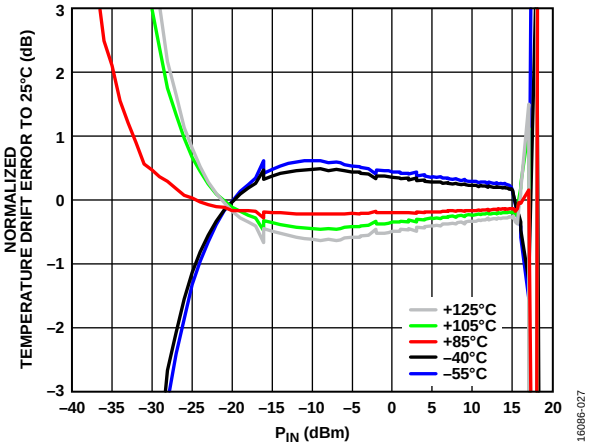


Figure 27. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 10 GHz

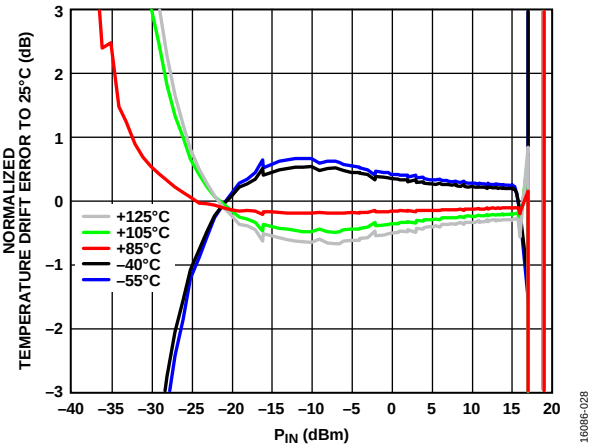


Figure 28. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 18 GHz

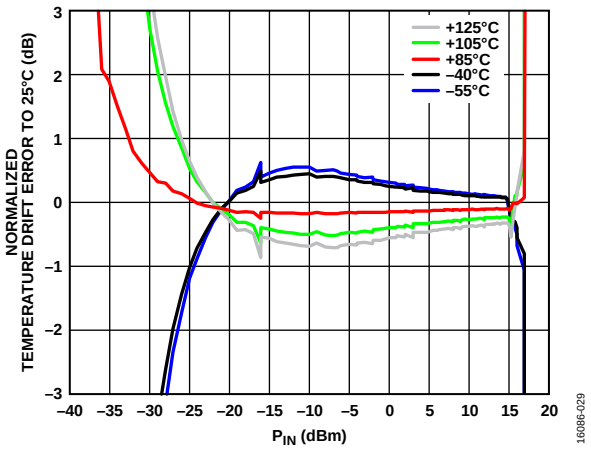


Figure 29. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 28 GHz

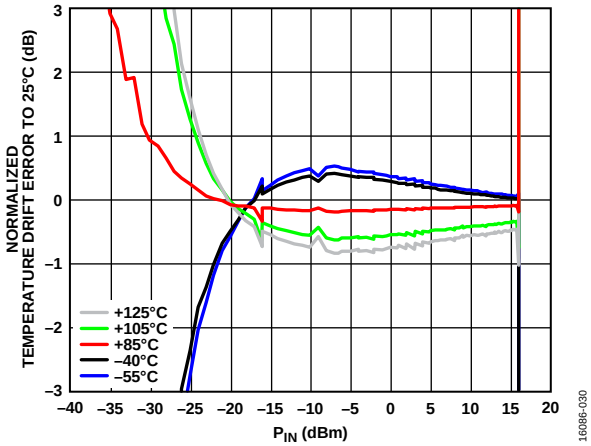


Figure 30. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 38 GHz

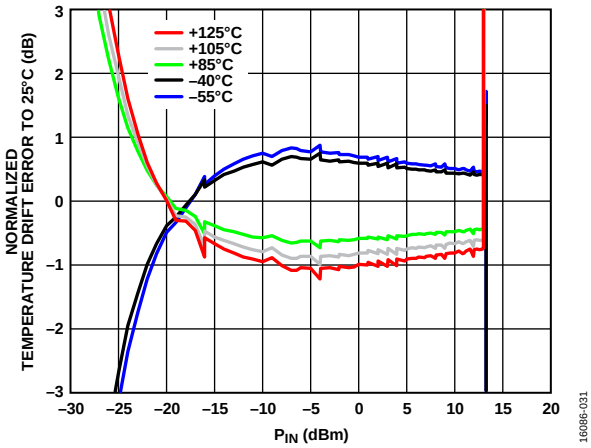


Figure 31. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 40 GHz

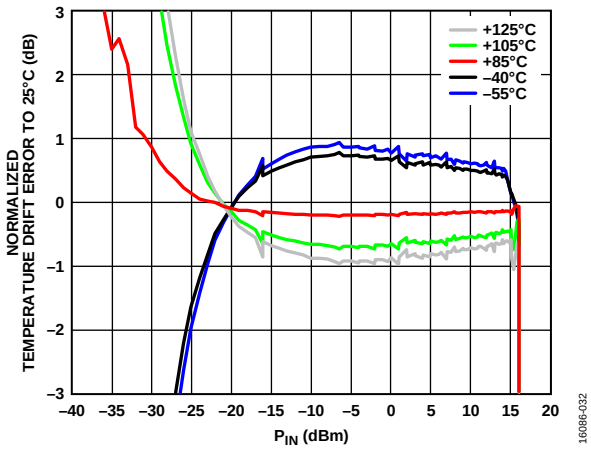


Figure 32. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 43.5 GHz

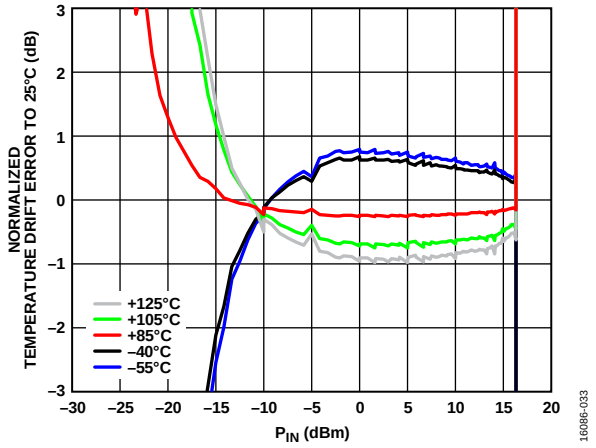


Figure 33. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 52 GHz

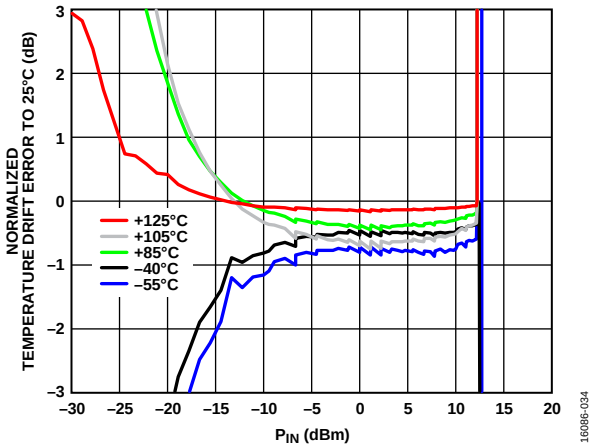


Figure 34. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 60 GHz

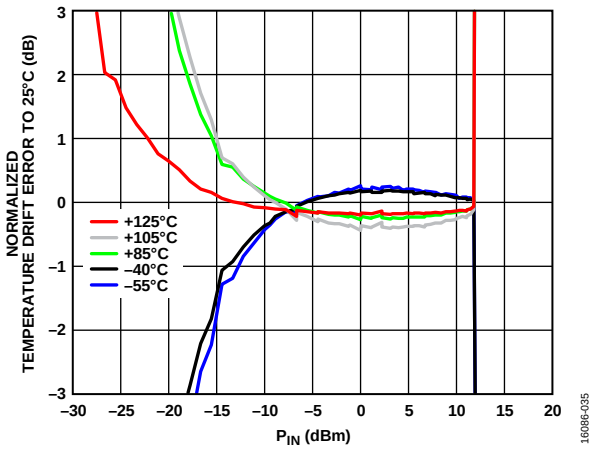


Figure 35. Normalized Temperature Drift Error to 25°C vs. P_{IN} for Various Temperatures at 67 GHz

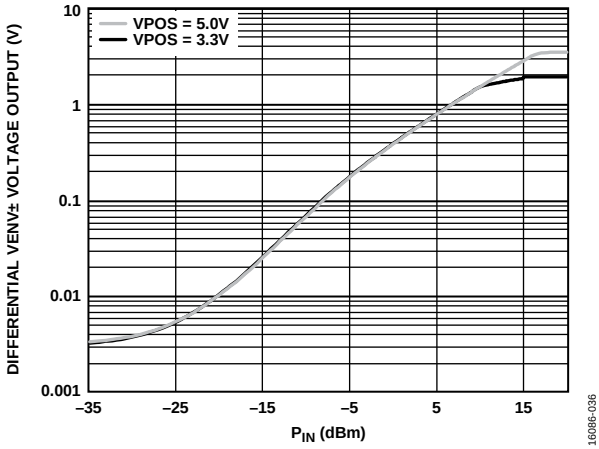


Figure 36. Differential VENV± Output Voltage vs. P_{IN} for Various Supply Voltages

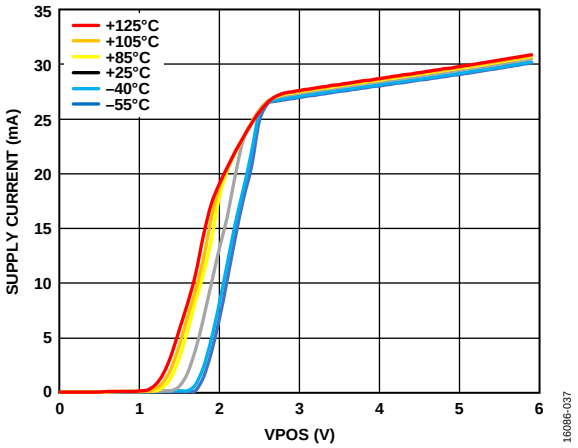


Figure 37. Supply Current vs. VPOS for Various Temperatures

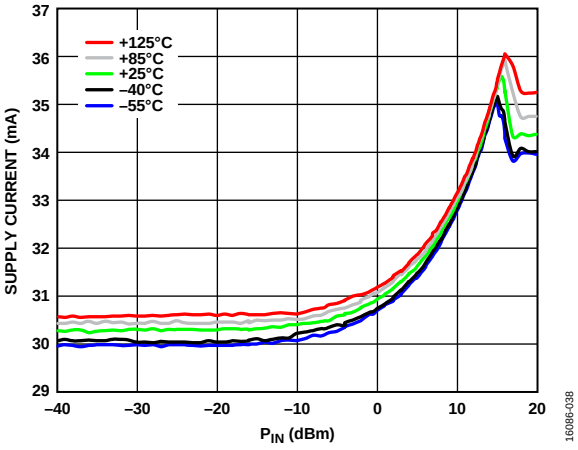


Figure 38. Supply Current vs. P_{IN} for Various Temperatures at18 GHz

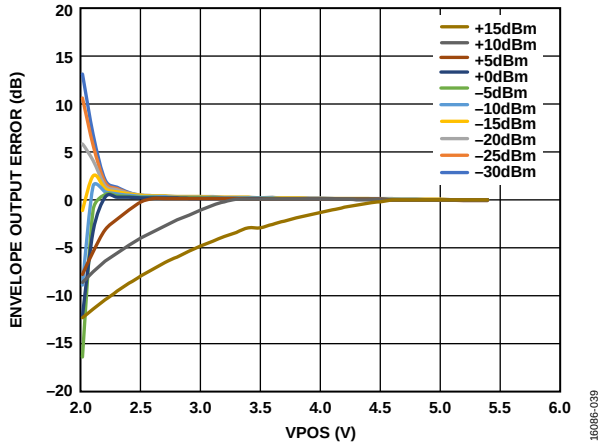


Figure 39. Envelope Output Error vs. VPOS at Different RF Input Power Levels

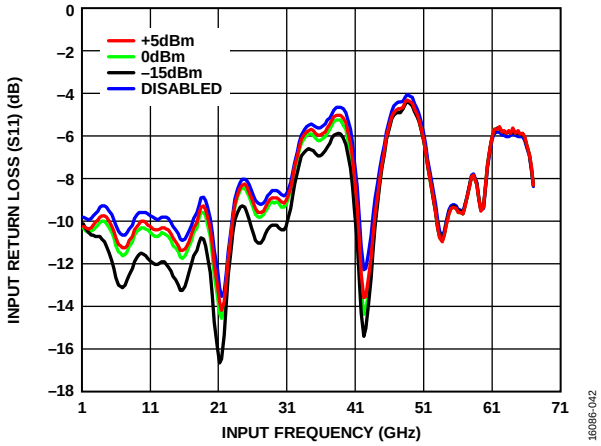


Figure 42. Input Return Loss (S11) vs. Input Frequency with Input Connector and PCB Trace Embedded

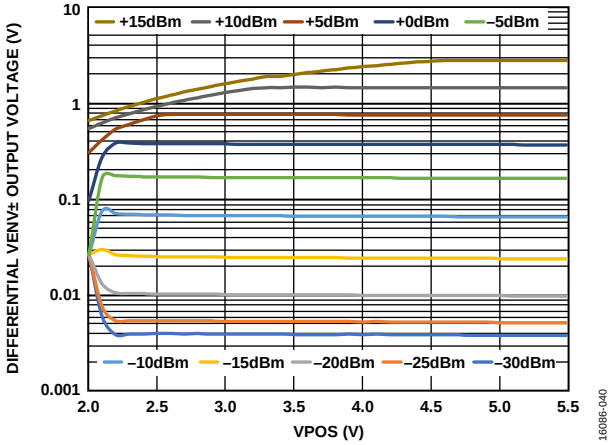


Figure 40. Differential VENV± Output vs. VPOS at Different RF Input Power Levels

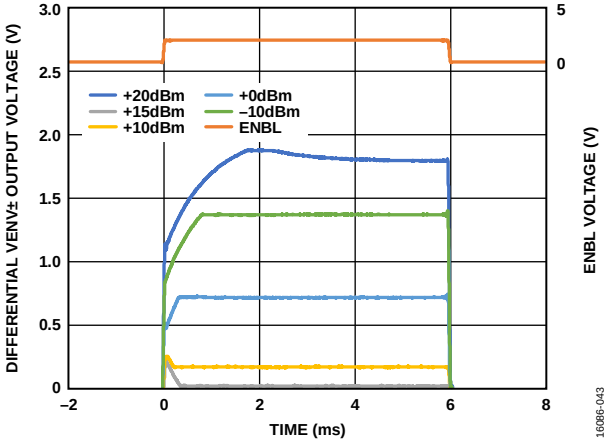


Figure 43. ENBL Pulse Response at Different RF Input Power Levels

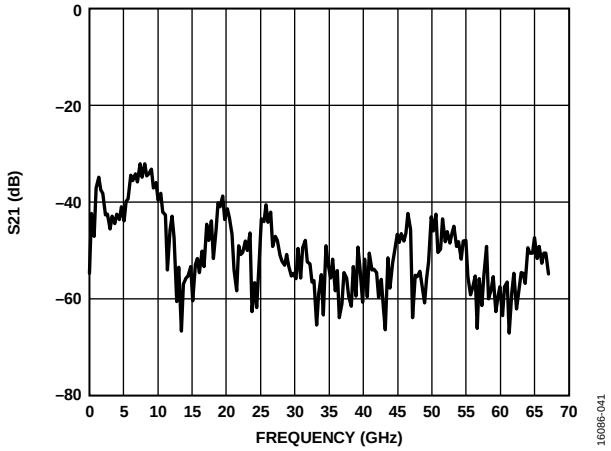


Figure 41. RF Feedthrough Insertion Loss (S21) from RFIN to VENV±

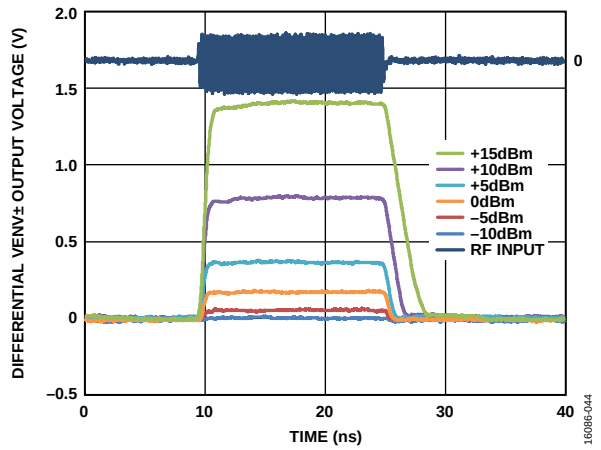


Figure 44. RF Input Pulse Response, Carrier = 4 GHz

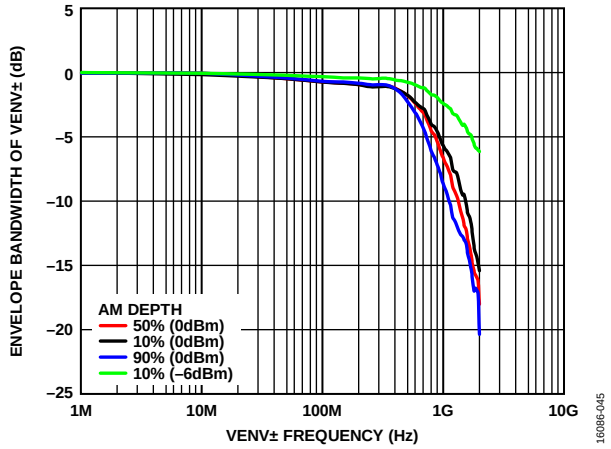


Figure 45. Envelope Bandwidth of VENV± vs. VENV± Frequency and Amplitude Modulation (AM) Depth

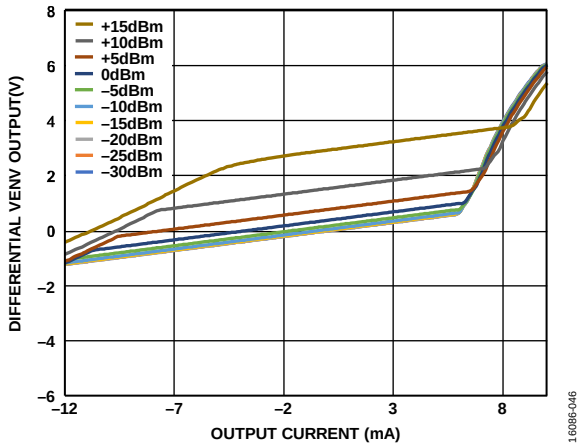


Figure 46. Differential VENV± Output Voltage vs. Output Current for Different RF Input Power Levels

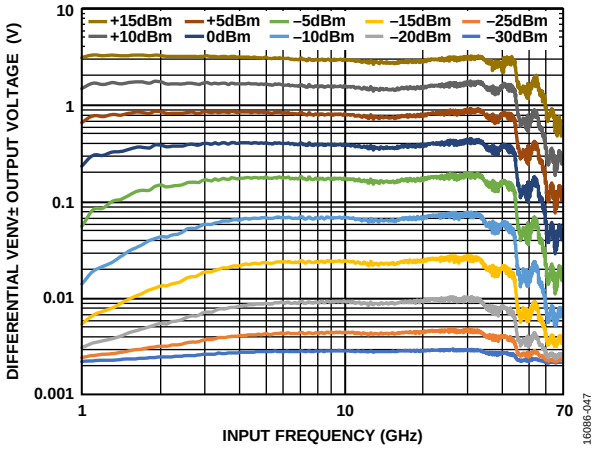


Figure 47. Differential VENV±-Output Voltage vs. Input Frequency at Different RF Input Power Levels

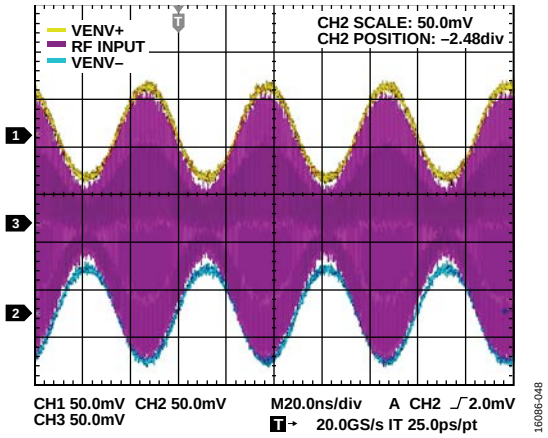


Figure 48. AM Response on VENV± Outputs, Carrier = 4 GHz, Envelope = 20 MHz

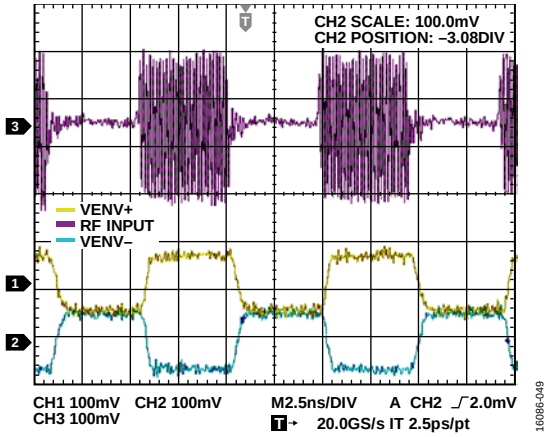


Figure 49. Pulse Response on VENV± Outputs, Carrier = 5.8 GHz

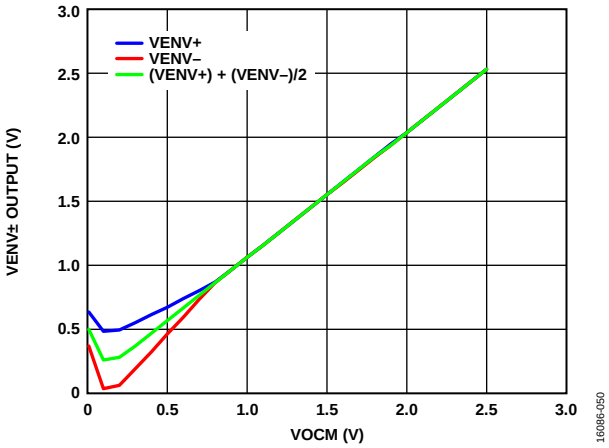


Figure 50. VENV± Output vs. VOCM, No RF Input

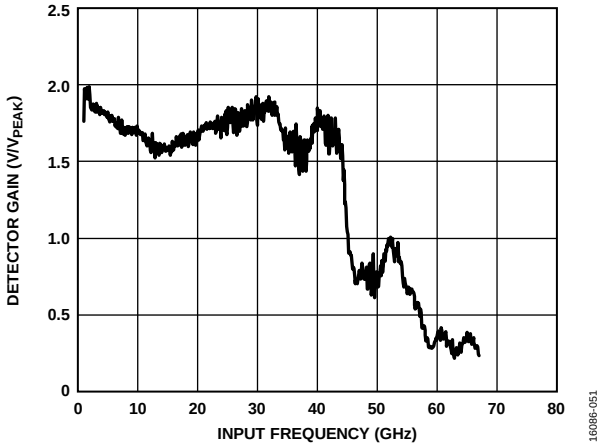


Figure 51. Detector Gain vs. Input Frequency

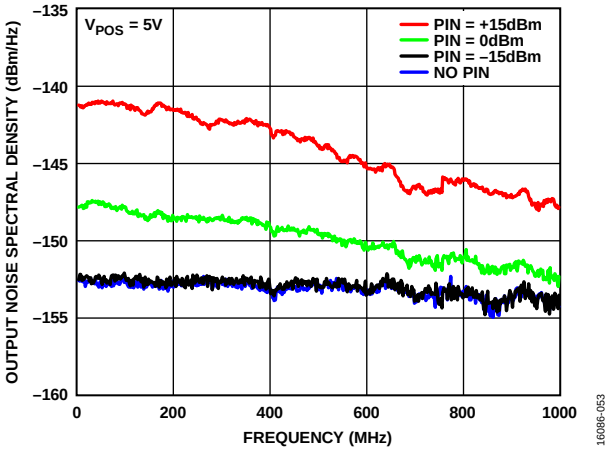


Figure 53. Output Spectral Noise Density vs. Frequency, RFIN = 3 GHz

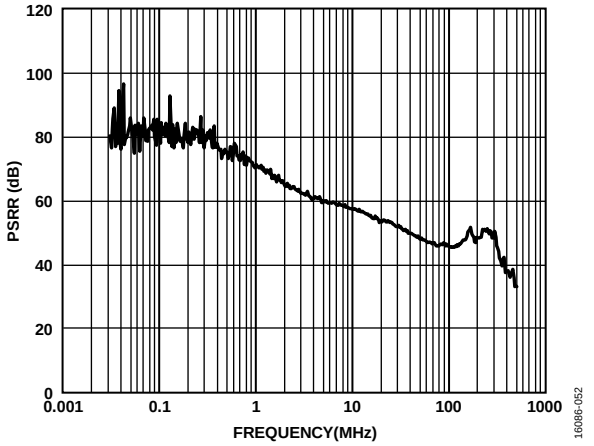


Figure 52. Power Supply Rejection Ratio (PSRR) vs. Frequency, 200 mV p-p at the VPOS Pin (See Figure 58 for the PSRR Measurement Setup)

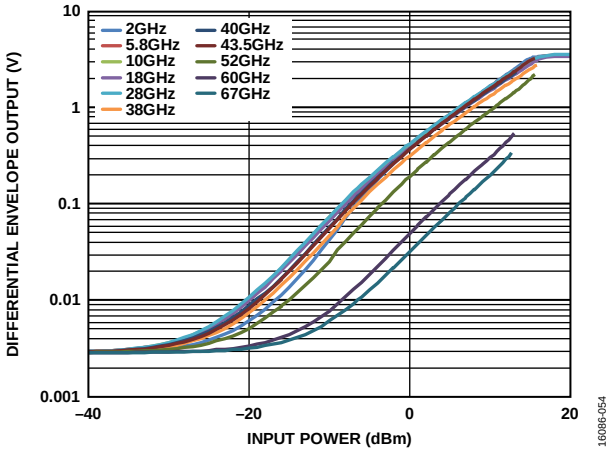


Figure 54. Differential Envelope Output vs. Input Power at Various Frequencies at 25°C

MEASUREMENT SETUPS

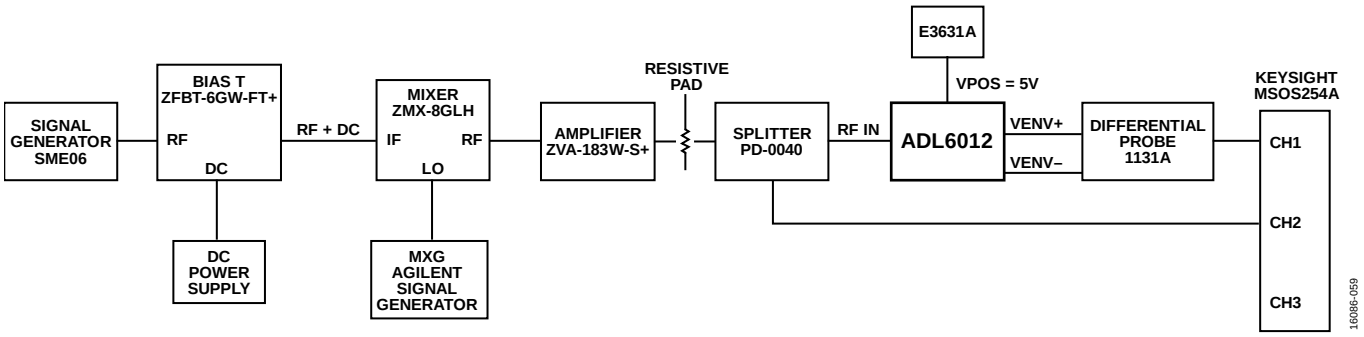


Figure 55. Amplitude Modulation Envelope Bandwidth Measurement Setup

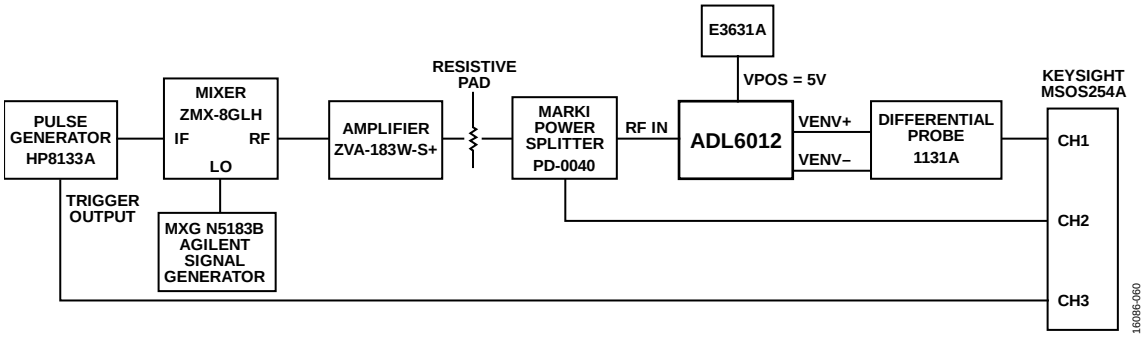


Figure 56. Test Setup for Pulse Response

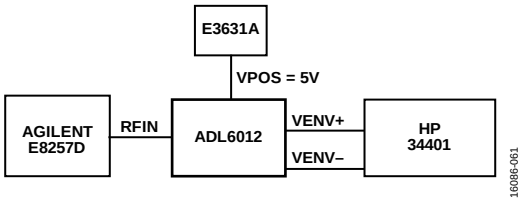


Figure 57. Setup to Measure Differential Envelope Output Voltage vs. Input Power

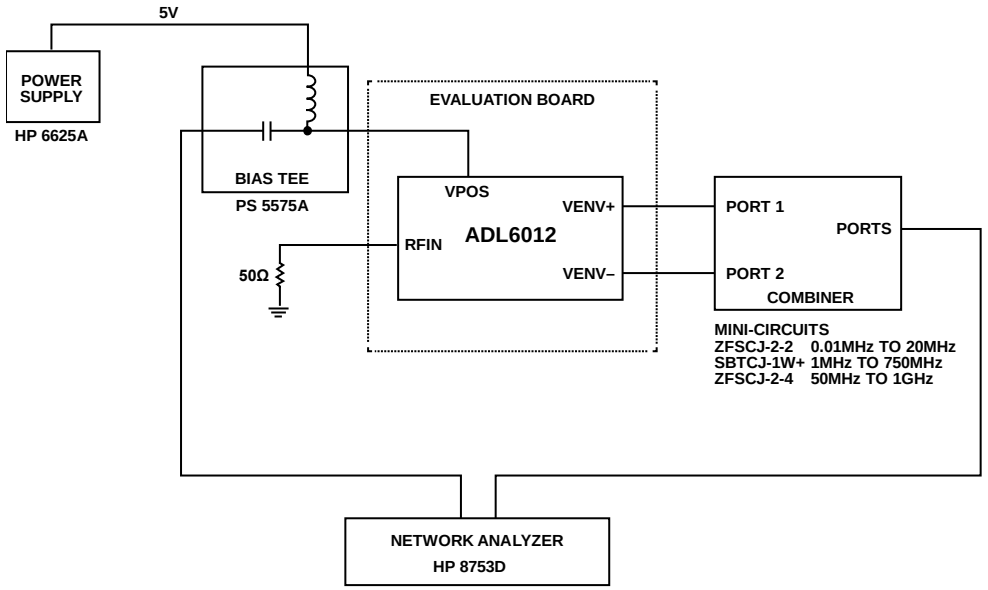


Figure 58. Setup for PSRR Measurement

THEORY OF OPERATION

The ADL6012 uses Schottky diodes in a two path detector topology. One path responds during the positive half cycles of the input, and the other responds during the negative half cycles of the input, achieving full wave signal detection. This arrangement presents a constant input impedance throughout the full RF cycle, preventing the reflection of even order harmonic distortion components back toward the source. This reflection is a well known phenomenon of widely used, traditional, single-Schottky diode detectors. Detector response time at lower RF frequencies is also improved with symmetrical detection.

The diodes are arranged on the chip to minimize the effect of chip stresses and temperature variations. The diodes are biased by small, keep alive currents chosen in a trade-off between the inherently low sensitivity of a diode detector and the need to preserve envelope bandwidth. Therefore, the corner frequency of the front-end, low-pass filtering is a weak function of the input level. At low input levels, the −3 dB corner frequency is at approximately 2 GHz.

DC voltages at the RFIN pin (Pin 3) are blocked by an on-chip capacitor. The two RFCM ground pins, Pin 2 and Pin 4, on either side of RFIN form part of an RF coplanar waveguide (CPWG) launch into the detector. The RFCM pins must be connected to the signal ground. Give careful attention to the design of the PCB in this area.

The output stage impedance is 100 Ω differential with propagation delay under 1 ns, and an envelope bandwidth over 500 MHz. The differential outputs, VENV+ and VENV− (Pin 8 and Pin 9, respectively) provide the high speed envelope information for both the positive and negative cycles of the RF input signal.

BASIC CONNECTIONS

The basic connections are shown in Figure 59. A dc supply of nominally 3.3 V to 5 V is required. The bypass capacitors (C2 and C3) provide supply decoupling for the device. Place these capacitors as close as possible to VPOS (Pin 5). The exposed pad is internally connected to the IC ground and must be soldered down to a low impedance ground on the PCB. OCOM (Pin 6) is the output common. Connect OCOM to a low impedance ground plane together with the exposed pad. DCPL (Pin 10) is connected to an internal bias node. Place a 0.1 µF capacitor to ground for the best common-mode noise rejection.

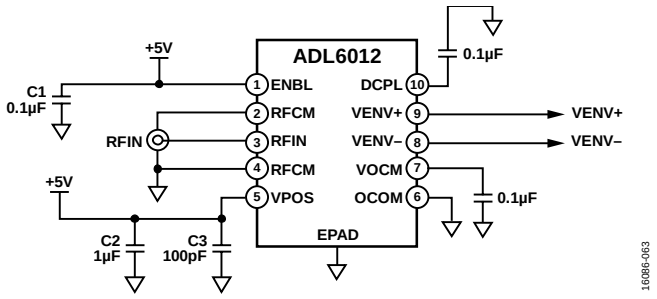


Figure 59. Basic Connections

RF INPUT

The RFIN single-ended input is internally terminated and internally ac-coupled. No external matching is required up to 67 GHz. The simplified input stage is shown in Figure 60. The input trace can be directly routed with CPWG with ground on both sides of the signal trace shown in Figure 65 and Figure 66. Broadband response is achieved with small vias on both sides of the signal trace and microwave dielectric material. The trace width, gap, and dielectric thickness for the CPWG is designed to the characteristic impedance of 50 Ω to ensure the broadband matching is achieved for the best frequency flatness.

The RFCM pins are the ground return to the RF input. It is critical that these pins are connected to the low impedance ground plane, and serve as ground for the CPWG.

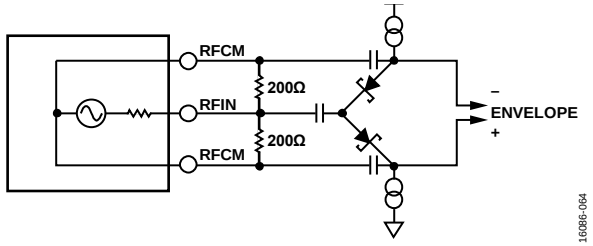


Figure 60. Input Stage

ENVELOPE OUTPUT INTERFACE

The differential envelope outputs, VENV+ and VENV−, provide the envelope information of the input signal. The ADL6012 is designed to drive 100 Ω differential or a 50 Ω load on each VENV± output when ac-coupled. It is important that the VENV± outputs are not dc-coupled to 50 Ω load referenced to ground, which results in excessive dc current flow to the load that may exceed the output drive capability, depending on the output common-mode voltage level. The ADL6012 is suitable for AM and pulse modulation detection. See Figure 48 and Figure 49 for the typical AM and pulse output response, respectively. The device features an extremely fast response time of approximately 1 ns or less.

For applications that require fast response to RF input levels or pulsed RF detection, connect the envelope outputs to transmission lines with a differential characteristic impedance of 100 Ω, terminated with a 100 Ω differential load, so that the outputs are impedance matched with no reflections from the load. Figure 61 shows the simplified ADL6012 output stage interfaced to a 100 Ω load with impedance controlled transmission lines.

The output impedance of the ADL6012 drives a differential 100 Ω load. The differential VENV± output dc voltage is divided down by the ratio of the load and output impedance. For example, with a differential 100 Ω output load, the differential output voltage is halved from the open load voltage. See Figure 62 for the differential envelope output voltage vs. the input power with various output loads.

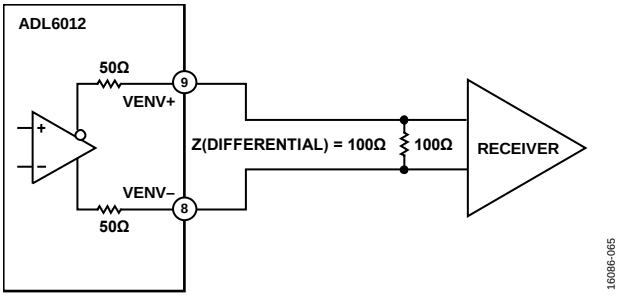


Figure 61. Simplified ADL6012 Output Interface

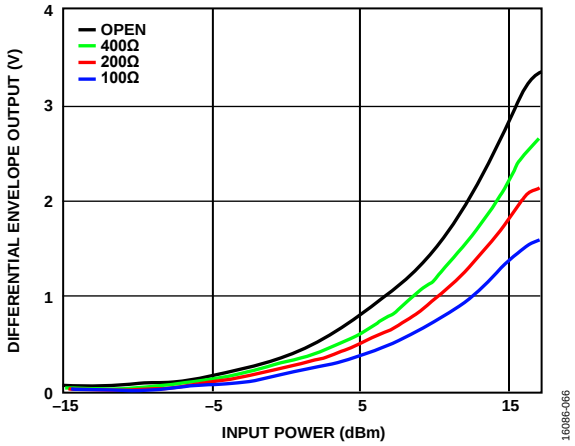


Figure 62. Differential Envelope Output vs. Input Power for Different Output Loads

The ADL6012 envelope outputs can also be ac-coupled for pulsed detection applications, as shown in Figure 63. AC coupling allows different common-mode voltages to be interfaced to the ADC. For example, the VENV+ and VENV− outputs can be used to detect pulses in radar applications. See Figure 49 for the typical envelope pulse response.

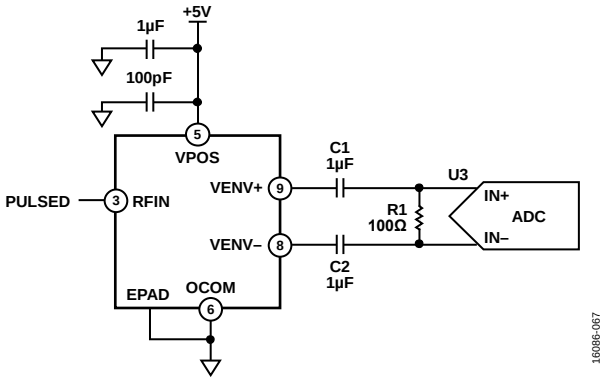


Figure 63. Simplified Pulsed Measurement Application

COMMON-MODE VOLTAGE INTERFACE

VOCM (Pin 7) is the input that controls the common-mode voltage output to the VENV± pins. VOCM sets the output common-mode voltage and is internally biased to VPOS/2. An external voltage source can be used for setting a different output common-mode voltage to accommodate the next stage input common-mode voltage range, as shown in Figure 64. The reference voltage from the ADC is used as the voltage source to accurately drive the VOCM pin. The range for VOCM is 0.9 V to VPOS/2. In addition, this pin is used to level shift the VENV± outputs so that both the positive and negative envelope information is accurately represented.

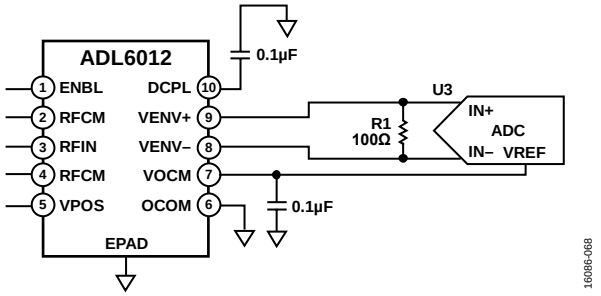


Figure 64. External Voltage Source Setting VOCM

Differential envelope outputs provide the lowest distortion and lower noise. The advantages of differential outputs include lower offset error, faster output response, higher common-mode noise rejection, and less feedthrough. Place a 0.1 µF bypass capacitor from VOCM to GND to minimize common-mode noise.

ENABLE INTERFACE

ENBL (Pin 1) provides the ability to enable or disable the device to conserve power. Connect ENBL to VPOS or above 1.5 V to enable the device. Connect ENBL to ground or below 0.5 V to disable the device. Do not exceed VPOS by 0.3 V or below ground by more than 0.3 V. Leaving the ENBL pin open turns off the device.

Faster turn on time can be achieved using a smaller capacitor value on the VOCM pin. The capacitor must be large enough to minimize the common-mode noise.

DECOUPLING INTERFACE

DCPL (Pin 10) is connected to the internal bias node. DCPL provides the stable output common-mode voltage. Connect a 0.1 µF capacitor from the DCPL pin to ground for the best common-mode noise performance.

PCB LAYOUT RECOMMENDATIONS

Parasitic elements of the PCB, such as coupling and radiation, limit accuracy at very high frequencies. Ensure low loss power transmission from the connector to the internal circuit of the ADL6012. Microstrip and CPWG are popular forms of transmission lines because of their ease of fabrication and low cost (see Figure 65 and Figure 66). In the ADL6012 evaluation board (ADL6012-EVALZ), a grounded CPWG (GCPWG) minimizes radiation effects and provides the maximum bandwidth by using two rows of grounding vias on both sides of the signal trace.

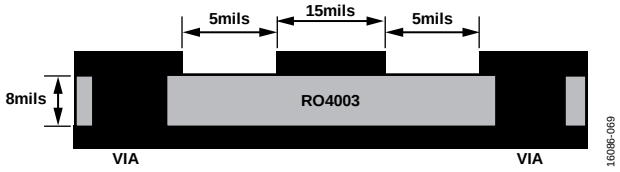


Figure 65. CPWG Interface Design to RFIN for RO4003 Material (Not to Scale)

Figure 66 shows the CPWG structure of the PCB layout. Microwave material RO4003 with 8 mil thickness is used in the ADL6012-EVALZ between the RF signal and ground layer.

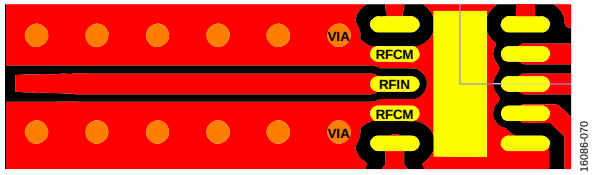


Figure 66. Suggested RF Input Layout

SYSTEM CALIBRATION AND MEASUREMENT ERROR

To achieve the highest detection accuracy, perform calibration at the board level because output voltages vary from device to device. Each device can be calibrated with two or more points in the linear region of the transfer function by applying CW input at different levels. The slope and intercept can be calculated as described in this section. Linear regression over the calibration range is recommended for best accuracy.

Board level calibration is a simple method to improve the accuracy of the envelope detection. With a minimum of two point or more calibration, the entire detection range of the device can be calibrated to the highest accuracy possible.

The measured ADL6012 transfer function at 18 GHz is shown in Figure 67 and the envelope output and linearity conformance error vs. the input peak voltage at various temperatures from −40°C to +125°C. Error over temperature is relative to the room 25°C curve.

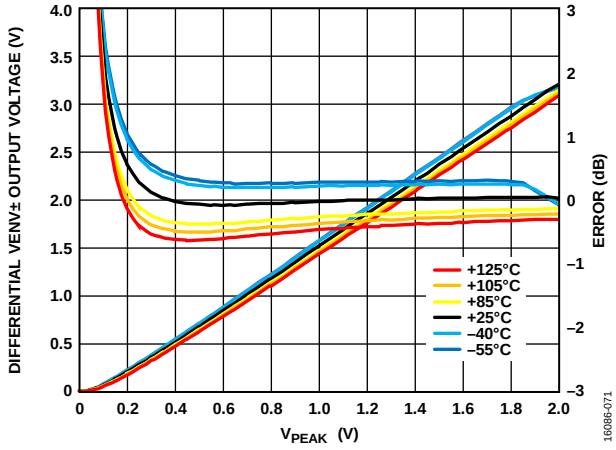


Figure 67. Differential VENV± Output Voltage and Error vs. Input Peak Voltage at 18 GHz

The following equations are used to calculate the slope and intercept of each device, which is used in calibration to improve the detection accuracy:

$$Slope = (V_{OUT2} - V_{OUT1})/(V_{PEAK2} - V_{PEAK1}) \quad (1)$$

$$Intercept = V_{OUT1} - (Slope \times V_{PEAK1}) \quad (2)$$

The error conformance is calculated as follows:

$$Error = 20 \times \log((V_{OUT} - Intercept)/(Slope \times V_{PEAK})) \quad (3)$$

where:
V_{OUT2} is the output voltage with V_{PEAK2} input.
V_{OUT1} is the output voltage with V_{PEAK1} input.
V_{OUT} is the differential envelope output voltage at different input levels.
V_{PEAK1} and V_{PEAK2} are input peak voltages at two different input levels.
V_{PEAK} is the peak voltage input.

The ADL6012 offers extremely stable temperature performance across frequencies. See Figure 25 to Figure 35 for the temperature drift error from −55°C to +125°C. The typical temperature drift is less than 1 dB of error over the entire detection range of the device from 2 GHz to 67 GHz. This makes the device well suited for applications operating over a wide temperature range. Temperature drift error relative to 25°C is calculated as follows:

$$Temperature\ Drift\ Error\ (\text{dB}) = (V_{OUT\ (TEMPERATURE)} - V_{OUT\ (AT\ 25°C)})/(dV_{OUT}/dP_{IN}) \quad (4)$$

where:
V_{OUT} is the differential envelope output.
dV_{OUT}/dP_{IN} is the derivative of the transfer function of the differential VENV± output at 25°C vs. the input power.

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADL6012-EVALZ is a fully populated, 4-layer, Rogers 4003A and FR4-based evaluation board. For normal operation, the board requires a 3.3 V to 5 V power supply. Connect the power supply to the VPOS and GND test loops. Apply the RF input to RFIN at the 1.85 mm connector. The differential envelope output signal is ac-coupled and is available on the connectors labelled VENV+ and VENV−. The dc envelope output voltage and the output common-mode voltage can be measured at the test points labeled VENV+_TP and VENV-TP. The output common-mode voltage can be set externally by the VOCM turret. See the ADL6012-EVALZ user guide for additional information on the eval board.

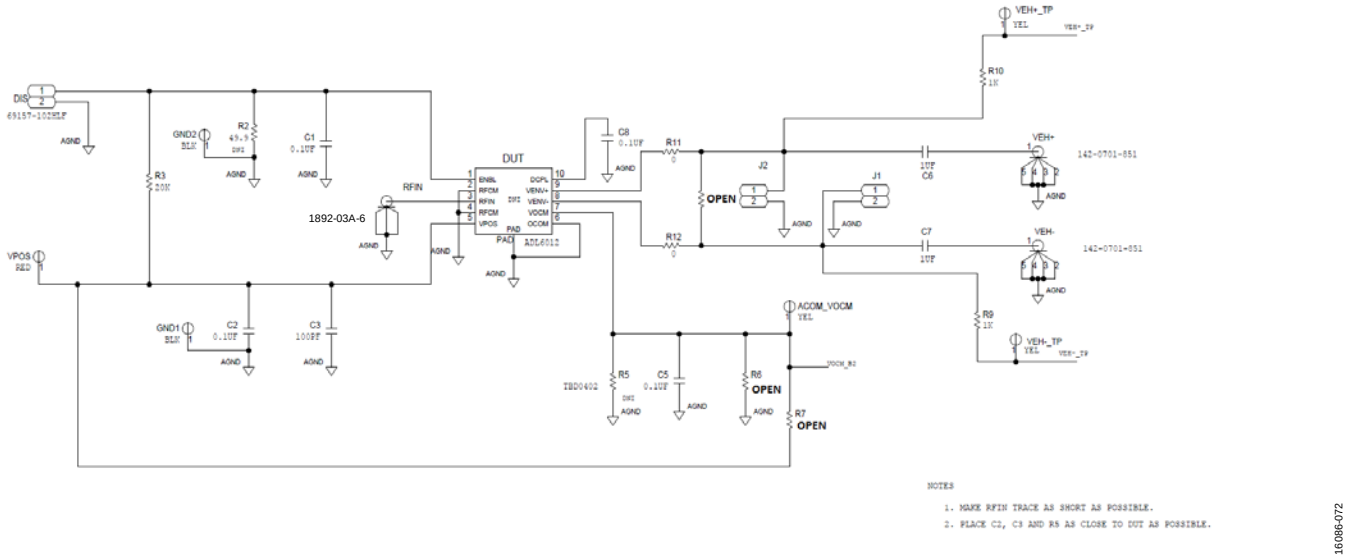
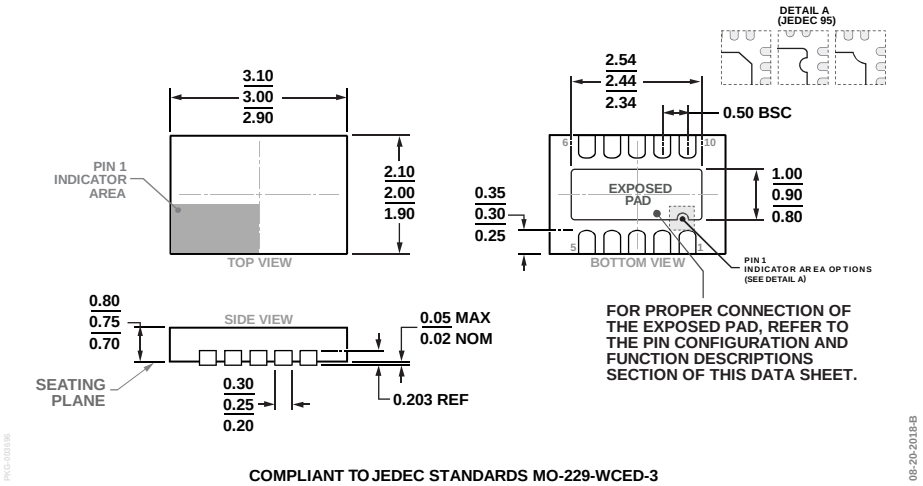


Figure 68. Evaluation Board Schematic (Rev. C)

Table 5. Evaluation Board Components

Component	Function/Comments	Default Value
C1	Bypass capacitor for the ENBL pin	0.1 µF
C2	Supply bypass capacitor. Place this capacitor as close to the VPOS pin as possible. Use microwave grade, PPI, 0402BB104KW500 material.	0.1 µF
C3	Supply bypass capacitor. Place this capacitor as close to the VPOS pin as possible. Use microwave grade material.	100 pF
C5, C8	Bypass capacitors for the output common-mode voltage. Place these capacitors as close to the IC as possible.	0.1 µF
C6, C7	Envelope output ac coupling capacitors.	1 µF
R2	ENBL termination resistor.	Open
R3	ENBL pull-up resistor.	20 kΩ
R4	Output load resistor.	Open
R5	Optional VOCM resistor.	Open
R6, R7	VOCM resistor divider network.	Open
R9, R10	Series resistors for measuring the dc envelope outputs.	1 kΩ
R11, R12	Series VENV± resistors.	0 Ω
RFIN connector	1.85 mm, edge mount. Southwest,1892-03A-6.	1892-03A-6

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-WCED-3

Figure 69. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 2 mm Body and 0.75 mm Package Height
(CP-10-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Marking Code
ADL6012ACPZN	−40°C to +105°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-12	1	C9Y
ADL6012ACPZN-R2	−40°C to +105°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-12	100	C9Y
ADL6012ACPZN-R7	−40°C to +105°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-12	1000	C9Y
ADL6012SCPZN	−55°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-12	1	CAL
ADL6012SCPZN-R2	−55°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-12	100	CAL
ADL6012-EVALZ		Evaluation Board		1	

[1] Z = RoHS Compliant Part.

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