DATA SHEET

AU5790
Single wire CAN transceiver

Product data
Supersedes data of 2001 Jan 31
IC18 Data Handbook

2001 May 18

Philips
Semiconductors

PHILIPS

Single wire CAN transceiver AU5790

FEATURES

- Supports in-vehicle class B multiplexing via a single bus line with ground return
- 33 kbps CAN bus speed with loading as per J2411
- 83 kbps high-speed transmission mode
- Low RFI due to output waveshaping
- Direct battery operation with protection against load dump, jump start and transients
- Bus terminal protected against short-circuits and transients in the automotive environment
- Built-in loss of ground protection
- Thermal overload protection
- Supports communication between control units even when network in low-power state
- 70 µA typical power consumption in sleep mode
- 8- and 14-pin small outline packages
- ±8 kV ESD protection on bus and battery pins

DESCRIPTION

The AU5790 is a line transceiver, primarily intended for in-vehicle multiplex applications. The device provides an interface between a CAN data link controller and a single wire physical bus line. The achievable bus speed is primarily a function of the network time constant and bit timing, e.g., up to 33.3 kbps with a network including 32 bus nodes. The AU5790 provides advanced sleep/wake-up functions to minimize power consumption when a vehicle is parked, while offering the desired control functions of the network at the same time. Fast transfer of larger blocks of data is supported using the high-speed data transmission mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BAT}	Operating supply voltage		5.3	13	27	V
T_{amb}	Operating ambient temperature range		–40		+125	°C
V_{BATld}	Battery voltage	load dump; 1s			+40	V
V_{CANHN}	Bus output voltage		3.65		4.55	V
V_T	Bus input threshold		1.8		2.2	V
t_{TrN}	Bus output delay, rising edge		3		6.3	µs
t_{TfN}	Bus output delay, falling edge		3		9	µs
t_{DN}	Bus input delay		0.3		1	µs
I_{BATS}	Sleep mode supply current			70	100	µA

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
SO8: 8-pin plastic small outline package	–40 °C to +125 °C	AU5790D	SOT96–1
SO14: 14-pin plastic small outline package	–40 °C to +125 °C	AU5790D14	SOT108–1

BLOCK DIAGRAM

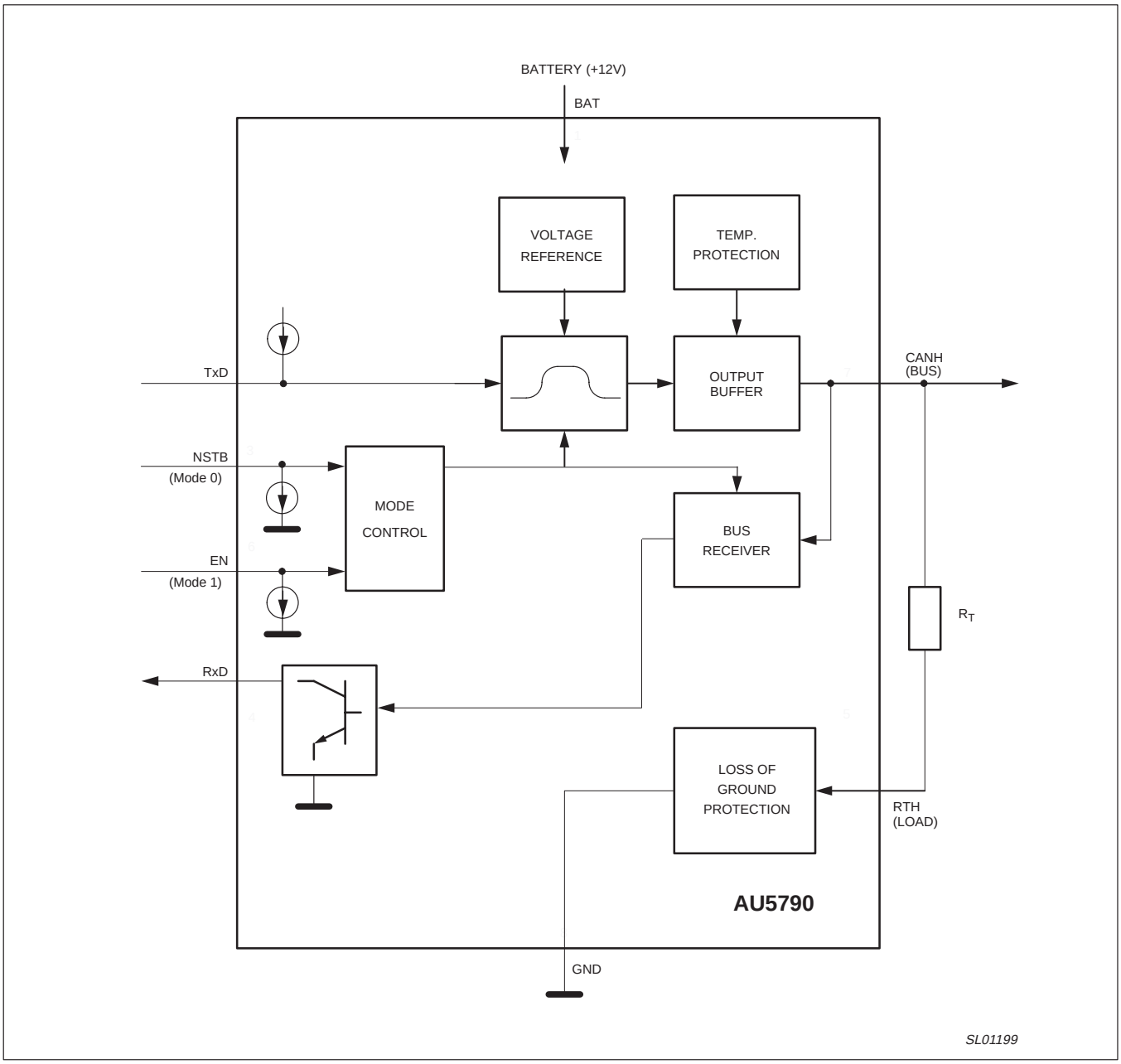
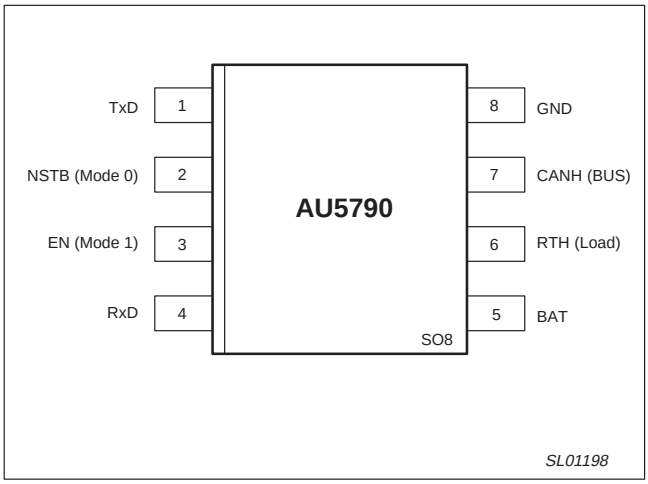


Figure 1. Block Diagram

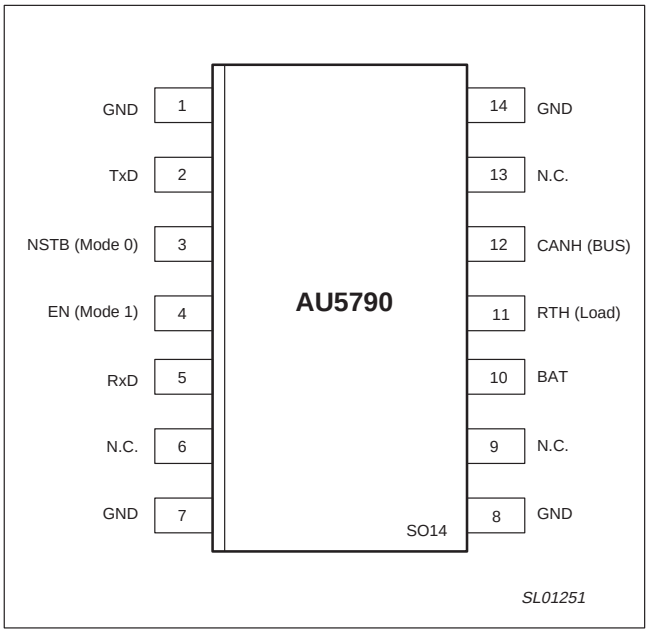
SO8 PIN CONFIGURATION



SO8 PIN DESCRIPTION

SYM-BOL	PIN	DESCRIPTION
TxD	1	**Transmit data input:** high = transmitter passive; low = transmitter active
NSTB (Mode 0)	2	**Stand-by control:** high = normal and high-speed mode; low = sleep and wake-up mode
EN (Mode 1)	3	**Enable control:** high = normal and wake-up mode; low = sleep and high-speed mode
RxD	4	**Receive data output:** low = active bus condition detected; float/high = passive bus condition detected
BAT	5	**Battery supply input** (12 V nom.)
RTH (LOAD)	6	**Switched ground pin:** pulls the load to ground, except in case the module ground is disconnected
CANH (BUS)	7	**Bus line transmit input/output**
GND	8	**Ground**

SO14 PIN CONFIGURATION



SO14 PIN DESCRIPTION

SYM-BOL	PIN	DESCRIPTION
GND	1	**Ground**
TxD	2	**Transmit data input:** high = transmitter passive; low = transmitter active
NSTB (Mode 0)	3	**Stand-by control:** high = normal and high-speed mode; low = sleep and wake-up mode
EN (Mode 1)	4	**Enable control:** high = normal and wake-up mode; low = sleep and high-speed mode
RxD	5	**Receive data output:** low = active bus condition detected; float/high = passive bus condition detected
N.C.	6	**No connection**
GND	7	**Ground**
GND	8	**Ground**
N.C.	9	**No connection**
BAT	10	**Battery supply input** (12 V nom.)
RTH (LOAD)	11	**Switched ground pin:** pulls the load to ground, except in case the module ground is disconnected
CANH (BUS)	12	**Bus line transmit input/output**
N.C.	13	**No connection**
GND	14	**Ground**

FUNCTIONAL DESCRIPTION

The AU5790 is an integrated line transceiver IC that interfaces a CAN protocol controller to the vehicle's multiplexed bus line. It is primarily intended for automotive "Class B" multiplexing applications in passenger cars using a single wire bus line with ground return. The achievable bit rate is primarily a function of the network time constant and the bit timing parameters. For example, the maximum bus speed is 33 kpbs with bus loading as specified in J2411 for a full 32 node bus, while 41.6 kbps at is possible with modified bus loading. The AU5790 also supports low-power sleep mode to help meet ignition-off current draw requirements.

The protocol controller feeds the transmit data stream to the transceiver's TxD input. The AU5790 transceiver converts the TxD data input to a bus signal with controlled slew rate and waveshaping to minimize emissions. The bus output signal is transmitted via the CANH in/output, connected to the physical bus line. If TxD is low, then a typical voltage of 4 V is output at the CANH pin. If TxD is high then the CANH output is pulled passive low via the local bus load resistance R_T. To provide protection against a disconnection of the module ground, the resistor R_T is connected to the RTH pin of the AU5790. By providing this switched ground pin, no current can flow from the floating module ground to the bus. The bus receiver detects the data stream on the bus line. The data signal is output at the RxD pin being connected to a CAN controller. The AU5790 provides appropriate filtering to ensure low susceptibility against electromagnetic interference. Further enhancement is possible with applying an external capacitor between CANH and ground potential. The device features low bus output leakage current at power supply failure situations.

If the NSTB and EN control inputs are pulled low or floating, the AU5790 enters a low-power or "sleep" mode. This mode is dedicated to minimizing ignition-off current drain, to enhance system efficiency. In sleep mode, the bus transmit function is disabled, e.g. the CANH output is inactive even when TxD is pulled low. An internal network active detector monitors the bus for any occurrence of signal edges on the bus line. If such edges are detected, this will be signalled to the CAN controller via the RxD output. Normal transmission mode will be entered again upon a high level being applied to the NSTB and EN control inputs. These signals are typically being provided by a controller device.

Sleeping bus nodes will generally ignore normal communication on the bus. They should be activated using the dedicated wake-up mode. When NSTB is low and EN is high the AU5790 enters wake-up mode i.e. it sends data with an increased signal level. This will result in an activation of other bus nodes being attached to the network.

The AU5790 also provides a high-speed transmission mode supporting bit rates up to 100 kbps. If the NSTB input is pulled high and the EN input is low, then the internal waveshaping function is disabled, i.e. the bus driver is turned on and off as fast as possible to support high-speed transmission of data. Consequently, the EMC performance is degraded in this mode compared to the normal transmission mode. In high-speed transmission mode the AU5790 supports the same bus signal level as specified for the CANH output in normal mode.

The AU5790 features special robustness at its BAT and CANH pins. Hence the device is well suited for applications in the automotive environment. The BAT input is protected against 40 V load dump and jump start condition. The CANH output is protected against wiring fault conditions, e.g., short circuit to ground or battery voltage, as well as typical automotive transients. In addition, an over-temperature shutdown function with hysteresis is incorporated protecting the device under system fault conditions. In case of the chip temperature reaching the trip point, the AU5790 will latch-off the transmit function. The transmit function is available again after a small decrease of the chip temperature. The AU5790 contains a power-on reset circuit. For $V_{bat} < 2.5$ V, the CANH output drive will be turned off, the output will be passive, and RxD will be high. For $2.5\ V < V_{bat} < 5.3$ V, the CANH output drive may operate normally or be turned off.

Table 1. Control Input Summary

NSTB	EN	TxD	Description	CANH	RxD
0	0	Don't Care	Sleep mode	0 V	float (high)
0	1	Tx-data	Wake-up transmission mode	0 V, 12 V	bus state[1]
1	0	Tx-data	High-speed transmission mode	0 V, 4 V	bus state[1]
1	1	Tx-data	Normal transmission mode	0 V, 4 V	bus state[1]

NOTE:

1. RxD outputs the bus state. If the bus level is below the receiver threshold (i.e., all transmitters passive), then RxD will be floating (i.e., high, considering external pull-up resistance). Otherwise, if the bus level is above the receiver threshold (i.e., at least one transmitter is active), then RxD will be low.

ABSOLUTE MAXIMUM RATINGS

According to the IEC 134 Absolute Maximum System: operation is not guaranteed under these conditions; all voltages are referenced to pin 8 (GND); positive currents flow into the IC, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT}	Supply voltage	Steady state	–0.3	+27	V
V_{BATld}	Short-term supply voltage	Load dump; ISO7637/1 test pulse 5 (SAE J1113, test pulse 5), T < 1s		+40	V
V_{BATtr2}	Transient supply voltage	ISO 7637/1 test pulse 2 (SAE J1113, test pulse 2), with series diode and bypass cap of 100 nF between BAT and GND pins, Note 2.		+100	V
V_{BATtr3}	Transient supply voltage	ISO 7637/1 pulses 3a and 3b (SAE J1113 test pulse 3a and 3b), Note 2.	–150	+100	V
V_{CANH_1}	CANH voltage	V_{BAT} > 2 V	–10	+18	V
V_{CANH_0}	CANH voltage	V_{BAT} < 2 V	–16	+18	V
$V_{CANHtr1}$	Transient bus voltage	ISO 7637/1 test pulse 1, Notes 1 and 2	–100		V
$V_{CANHtr2}$	Transient bus voltage	ISO 7637/1 test pulse 2, Notes 1 and 2		+100	V
$V_{CANHtr3}$	Transient bus voltage	ISO 7637/1 test pulses 3a, 3b, Notes 1 and 2	–150	+100	V
V_{RTH1}	Pin RTH voltage	V_{BAT} > 2 V, voltage applied to pin RTH via a 2 kΩ series resistor	–10	+18	V
V_{RTH0}	Pin RTH voltage	V_{BAT} < 2 V, voltage applied to pin RTH via a 2 kΩ series resistor	–16	+18	V
V_I	DC voltage on pins TxD, EN, RxD, NSTB		–0.3	+7	V
ESD_{BAHB}	ESD capability of pin BAT	Direct contact discharge, R=1.5 kΩ, C=100 pF	–8	+8	kV
ESD_{CHHB}	ESD capability of pin CANH	Direct contact discharge, R=1.5 kΩ, C=100 pF	–8	+8	kV
ESD_{RTHB}	ESD capability of pin RTH	Direct contact discharge, R=1.5 kΩ + 3 kΩ, C=100 pF	–8	+8	kV
ESD_{LGHB}	ESD capability of pins TxD, NSTB, EN, RxD, and RTH	Direct contact discharge, R=1.5 kΩ , C=100 pF	–2	+2	kV
R_{Tmin}	Bus load resistance R_T being connected to pin RTH		2		kΩ
T_{amb}	Operating ambient temperature		–40	+125	°C
T_{stg}	Storage temperature		–40	+150	°C
T_{vj}	Junction temperature		–40	+150	°C

NOTES:
1. Test pulses are coupled to CANH through a series capacitance of 1 nF.
2. Rise time for test pulse 1: t_r < 1 µs; pulse 2: t_r < 100 ns; pulses 3a/3b: t_r < 5 ns.

DC CHARACTERISTICS

$-40\ °C < T_{amb} < +125\ °C$; $5.5\ V < V_{BAT} < 16\ V$; $-0.3\ V < V_{TxD} < 5.5\ V$; $-0.3\ V < V_{NSTB} < 5.5\ V$; $-0.3\ V < V_{EN} < 5.5\ V$; $-0.3\ V < V_{RxD} < 5.5\ V$; $-1\ V < V_{CANH} < +16\ V$; bus load resistor at pin RTH: $2\ k\Omega < R_T < 9.2\ k\Omega$; total bus load resistance $270\ \Omega < R_L < 9.2\ k\Omega$; $C_L < 13.7\ nF$; $1\mu s < R_L * C_L < 4\mu s$; RxD pull-up resistor $2.2\ k\Omega < R_d < 3.0\ k\Omega$; RxD: loaded with $C_{LR} < 30pF$ to GND; all voltages are referenced to pin 8 (GND); positive currents flow into the IC; typical values reflect the approximate average value at $V_{BAT} = 13\ V$ and $T_{amb} = 25\ °C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin BAT						
V_{BAT}	Operating supply voltage	Note 1	5.3	13	27	V
V_{BATL}	Low battery state	Part functional or in undervoltage lockout state	2.5		5.3	V
V_{BATLO}	Supply undervoltage lockout state	TxD = 1 or 0; check CANH and RxD are floating			2.5	V
I_{BATPN}	Passive state supply current in normal mode	NSTB = 5 V, EN = 5 V, TxD = 5 V			2	mA
I_{BATPW}	Passive state supply current in wake-up mode	NSTB = 0 V, EN = 5 V, TxD = 5 V, Note 2			3	mA
I_{BATPH}	Passive state supply current in high speed mode	NSTB = 5 V, EN = 0 V, TxD = 5 V, Note 2			4	mA
I_{BATN}	Active state supply current in normal mode	NSTB = 5 V, EN = 5 V, TxD = 0 V, $R_L = 270\ \Omega$, $T_{amb} = 125\ °C$			35	mA
		$T_{amb} = 25\ °C, -40\ °C$			40	mA
I_{BATW}	Active state supply current in wake-up mode	NSTB = 0 V, EN = 5 V, TxD = 0 V, $R_L = 270\ \Omega$, Note 2, $T_{amb} = 125\ °C$			70	mA
		$T_{amb} = 25\ °C, -40\ °C$, Note 2			90	mA
I_{BATH}	Active state supply current in high speed mode	NSTB = 5 V, EN = 0 V, TxD = 0 V, $R_L = 100\ \Omega$, Note 2, $T_{amb} = 125\ °C$			70	mA
		$T_{amb} = 25\ °C, -40\ °C$, Note 2			85	mA
I_{BATS}	Sleep mode supply current	NSTB = 0 V, EN = 0 V, TxD = 5 V, RxD = 5 V, $-1\ V < V_{CANH} < +1\ V$, $5.5\ V < V_{BAT} < 14\ V$, $-40\ °C < T_j < 125\ °C$		70	100	µA
Pin CANH						
V_{CANHN}	Bus output voltage in normal mode	NSTB = 5 V, EN = 5 V, $R_L > 270\Omega$; $5.5\ V < V_{BAT} < 27\ V$	3.65	4.1	4.55	V
V_{CANHW}	Bus output voltage in wake-up mode	NSTB = 0 V, EN = 5 V, $R_L > 270\Omega$; $11.3\ V < V_{BAT} < 16\ V$	9.80		min (V_{BAT}, 13)	V
V_{CANHWL}	Bus output voltage in wake-up mode, low battery	NSTB = 0 V, EN = 5 V, $R_L > 270\Omega$; $5.5\ V < V_{BAT} < 11.3\ V$	$V_{BAT} - 1.45$		V_{BAT}	V
V_{CANHH}	Bus output voltage in high-speed transmission mode	NSTB = 5 V, EN = 0 V, $R_L > 100\Omega$; $8\ V < V_{BAT} < 16\ V$	3.65		4.55	V
I_{CANHRR}	Recessive state output current, bus recessive	Recessive state or sleep mode, $V_{CANH} = -1\ V$; $0\ V < V_{BAT} < 27\ V$	–10		10	µA
I_{CANHRD}	Recessive state output current, bus dominant	Recessive state or sleep mode, $V_{CANH} = 10\ V$; $0\ V < V_{BAT} < 16\ V$	–20		100	µA
I_{CANHDD}	Dominant state output current, bus dominant	TxD = 0 V, normal mode, high-speed mode and sleep mode; $V_{CANH} = 10\ V$; $0\ V < V_{BAT} < 16\ V$	–20		100	µA
$-I_{CANH_N}$	Bus short circuit current, normal mode	$V_{CANH} = -1\ V$, TxD = 0 V; NSTB = 5 V; EN = 5 V	30		150	mA
$-I_{CANHW}$	Bus short circuit current, wake-up mode	$V_{CANH} = -1\ V$, TxD = 0 V; NSTB = 0 V; EN = 5 V	60		190	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin CANH (continued)						
$-I_{CANHH}$	Bus short circuit current in high-speed mode	V_{CANH} = –1 V, TxD = 0 V; NSTB = 5 V; EN = 0 V; 8 V < V_{BAT} < 16 V	50		190	mA
I_{CANLG}	Bus leakage current at loss of ground (I_CAN_LG = I_CANH + I_RTH)	0 V < V_{BAT} < 16 V; see Figure 3 in the test circuits section	–50		50	µA
T_{sd}	Thermal shutdown	Note 2	155		190	°C
T_{hys}	Thermal shutdown hysteresis	Note 2	5		15	°C
V_T	Bus input threshold	5.8 V < V_{BAT} < 27 V, all modes except sleep mode	1.8		2.2	V
V_{TL}	Bus input threshold, low battery	5.5 V < V_{BAT} < 5.8 V, all modes except sleep mode	1.5		2.2	V
V_{TS}	Bus input threshold in sleep mode	NSTB = 0 V, EN = 0 V, V_{BAT} > 11.3 V	6.15		8.1	V
V_{TSL}	Bus input threshold in sleep mode, low battery	NSTB = 0 V, EN = 0 V, 5.5 V < V_{BAT} < 11.3 V	V_{BAT} – 4.3		V_{BAT} – 3.25	V
Pin RTH						
V_{RTH1}	Voltage on switched ground pin	I_{RTH} = 1 mA			0.1	V
V_{RTH2}	Voltage on switched ground pin	I_{RTH} = 6 mA			1	V
Pins NSTB, EN						
V_{ih}	High level input voltage	5.5 V < V_{BAT} < 27 V	3			V
V_{il}	Low level input voltage	5.5 V < V_{BAT} < 27 V			1	V
I_i	Input current	V_i = 1 V and V_i = 5 V	15		50	µA
Pin TxD						
V_{itxd}	TxD input threshold	5.5 V < V_{BAT} < 27 V	1		3	V
$-I_{iltxd}$	TxD low level input current in normal mode	NSTB = 5 V, EN = 5 V, V_{TxD} = 0 V	50		180	µA
$-I_{ihtxd}$	TxD high level input current in sleep mode	NSTB = 0 V, EN = 0 V, V_{TxD} = 5 V	–5		10	µA
Pin RxD						
V_{olrxd}	RxD low level output voltage	I_{RxD} = 2.2 mA; V_{CANH} = 10 V, all modes			0.45	V
I_{olrxd}	RxD low level output current	V_{RxD} = 5 V; V_{CANH} = 10 V	3		35	mA
I_{ohrxd}	RxD high level leakage	V_{RxD} = 5 V; V_{CANH} = 0 V, all modes	–10		+10	µA

NOTES:

1. Operation at battery voltages down to 5.3 volts is guaranteed by design. Operation higher than 18 volts (18 V < V_{BAT} < 27 V) for up to two minutes is permitted if the thermal design of the board prevents reaching the thermal protection temperature limit, T_{sd}, otherwise the device will self protect. Typically these requirements will be encountered during jump start operation at T_{amb} 85 °C and V_{BAT} < 27 V. Refer to the “Thermal Characteristics” section of this data sheet, or application note AN2005 for guidance.
2. This parameter is characterized but not subject to production test.

Dynamic (AC) CHARACTERISTICS for 33 kbps operation

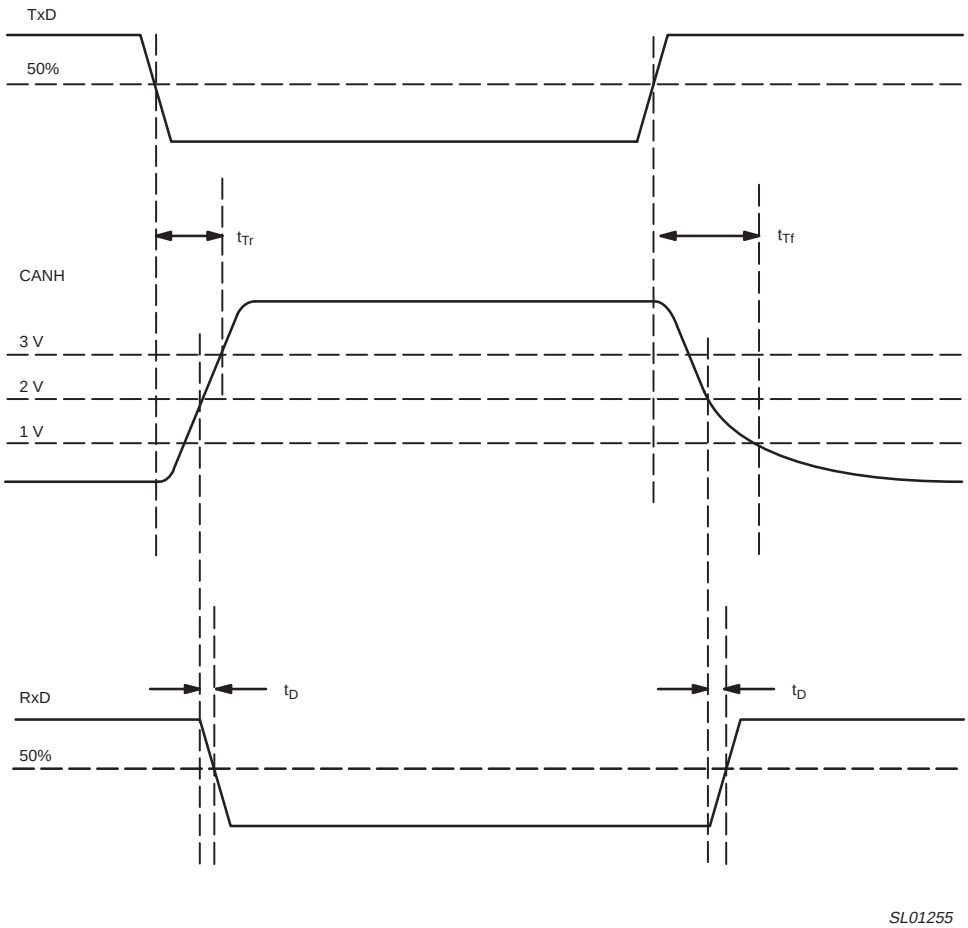
$-40\ °C < T_{amb} < +125\ °C$; $5.5\ V < V_{BAT} < 16\ V$; $-0.3\ V < V_{TxD} < 5.5\ V$; $-0.3\ V < V_{NSTB} < 5.5\ V$; $-0.3\ V < V_{EN} < 5.5\ V$; $-0.3\ V < V_{RxD} < 5.5\ V$; $-1\ V < V_{CANH} < +16\ V$; bus load resistor at pin RTH: $2\ k\Omega < R_T < 9.2\ k\Omega$; total bus load resistance $270\ \Omega < R_L < 9.2\ k\Omega$; $C_L < 13.7\ nF$; $1\mu s < R_L * C_L < 4\mu s$; RxD pull-up resistor $2.2\ k\Omega < R_d < 3.0\ k\Omega$; RxD: loaded with $C_{LR} < 30pF$ to GND; all voltages are referenced to pin 8 (GND); positive currents flow into the IC; typical values reflect the approximate average value at $V_{BAT} = 13\ V$ and $T_{amb} = 25\ °C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin CANH						
V_{dBAMN}	CANH harmonic content in normal mode	NSTB = 5 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $f_{TxD} = 20\ kHz$, 50% duty cycle; $8\ V < V_{BAT} < 16\ V$; $0.53\ MHz < f < 1.7\ MHz$, Note 2			70	dBµV
V_{dBAMW}	CANH harmonic content in wake-up mode	NSTB = 5 V, EN = 0 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $f_{TxD} = 20\ kHz$, 50% duty cycle; $8\ V < V_{BAT} < 16\ V$; $0.53\ MHz < f < 1.7\ MHz$, Note 2			80	dBµV
Pins NSTB, EN						
t_{NH}	Normal mode to high-speed mode delay				30	µs
t_{HN}	High-speed mode to normal mode delay				30	µs
t_{WN}	Wake-up mode to normal mode delay	$8\ V < V_{BAT} < 16\ V$			30	µs
t_{NS}	Normal mode to sleep mode delay				500	µs
t_{SN}	Sleep mode to normal mode delay				50	µs
Pin TxD						
t_{TrN}	Transmit delay in normal mode, bus rising edge	NSTB = 5 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $5.5\ V < V_{BAT} < 27\ V$; measured from the falling edge on TxD to $V_{CANH} = 3.0\ V$	3		6.3	µs
t_{TfN}	Transmit delay in normal mode, bus falling edge	NSTB = 5 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $5.5\ V < V_{BAT} < 27\ V$; measured from the rising edge on TxD to $V_{CANH} = 1.0\ V$	3		9	µs
t_{TrW}	Transmit delay in wake-up mode, bus rising edge to normal levels	NSTB = 0 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $5.5\ V < V_{BAT} < 27\ V$; measured from the falling edge on TxD to $V_{CANH} = 3.0\ V$	3		6.3	µs
t_{TrW-S}	Transmit delay in wake-up mode, bus rising edge to wake-up level	NSTB = 0 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $11.3\ V < V_{BAT} < 27\ V$; measured from the falling edge on TxD to $V_{CANH} = 8.9\ V$	3		18	µs
$t_{TfW-3.6}$	Transmit delay in wake-up mode, bus falling edge with 3.6 µs time constant	NSTB = 0 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 13.3\ nF$; $5.5\ V < V_{BAT} < 27\ V$; measured from the rising edge on TxD to $V_{CANH} = 1\ V$, Note 2	3		12.7	µs
$t_{TfW-4.0}$	Transmit delay in wake-up mode, bus falling edge with 4.0 µs time constant	NSTB = 0 V, EN = 5 V; $R_L = 270\ \Omega$, $C_L = 15\ nF$; $5.5\ V < V_{BAT} < 27\ V$; measured from the rising edge on TxD to $V_{CANH} = 1\ V$	3		13.7	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin TxD (continued)						
t_{TrHS}	Transmit delay in high-speed mode, bus rising edge	NSTB = 5 V, EN = 0 V; R_L = 100 Ω, C_L = 15 nF; 8 V < V_{BAT} < 16 V; measured from the falling edge on TxD to V_{CANH} = 3.0 V	0.1		1.5	µs
t_{TfHS}	Transmit delay in high-speed mode, bus falling edge	NSTB = 5 V, EN = 0 V; R_L = 100 Ω, C_L = 15 nF; 8 V < V_{BAT} < 16 V; measured from the rising edge on TxD to V_{CANH} = 1.0 V	0.2		3	µs
Pin RxD						
t_{DN}	Receive delay in normal mode, bus rising and falling edge	NSTB = 5 V, EN = 5 V; 5.5 V < V_{BAT} < 27 V; CANH to RxD time measured from V_{CANH} = 2.0 V to V_{RxD} = 2.5 V	0.3		1	µs
t_{DW}	Receive delay in wake-up mode, bus rising and falling edge	NSTB = 0 V, EN = 5 V; 5.5 V < V_{BAT} < 27 V; CANH to RxD time measured from V_{CANH} = 2.0 V to V_{RxD} = 2.5 V	0.3		1	µs
t_{DHS}	Receive delay in high-speed mode, bus rising and falling edge	NSTB = 5 V, EN = 0 V; 8 V < V_{BAT} < 16 V; CANH to RxD time measured from V_{CANH} = 2.0 V to V_{RxD} = 2.5 V	0.3		1	µs
t_{DS}	Receive delay in sleep mode, bus rising edge	NSTB = 0 V, EN = 0 V; CANH to RxD time, measured from V_{CANH} = min {(V_{BAT} – 3.78 V), 7.13 V} to V_{RxD} = 2.5 V	10		70	µs

NOTES:

1. Operation at battery voltages down to 5.3 volts is guaranteed by design. Operation higher than 18 volts (18 V < V_{BAT} < 27 V) for up to two minutes is permitted if the thermal design of the board prevents reaching the thermal protection temperature limit, T_{sd}, otherwise the device will self protect. Typically these requirements will be encountered during jump start operation at T_{amb} 85 °C and V_{BAT} < 27 V. Refer to the “Thermal Characteristics” section of this data sheet, or application note AN2005 for guidance.
2. This parameter is characterized but not subject to production test.



NOTE:

1. When AU5790 is in normal, high-speed, or wake-up mode, the transmit delay in rising edge t_{Tr} may be expressed as t_{TrN}, t_{TrHS}, or t_{TrW}, respectively; the transmit delay in falling edge t_{Tf} may be expressed as t_{TfN}, t_{TfHS}, or t_{TfW}, respectively; and the receive delay t_D as t_{DN}, t_{DHS}, or t_{DW}, respectively.

Figure 2. Timing Diagrams: Pin TxD, CANH, and RxD

TEST CIRCUITS

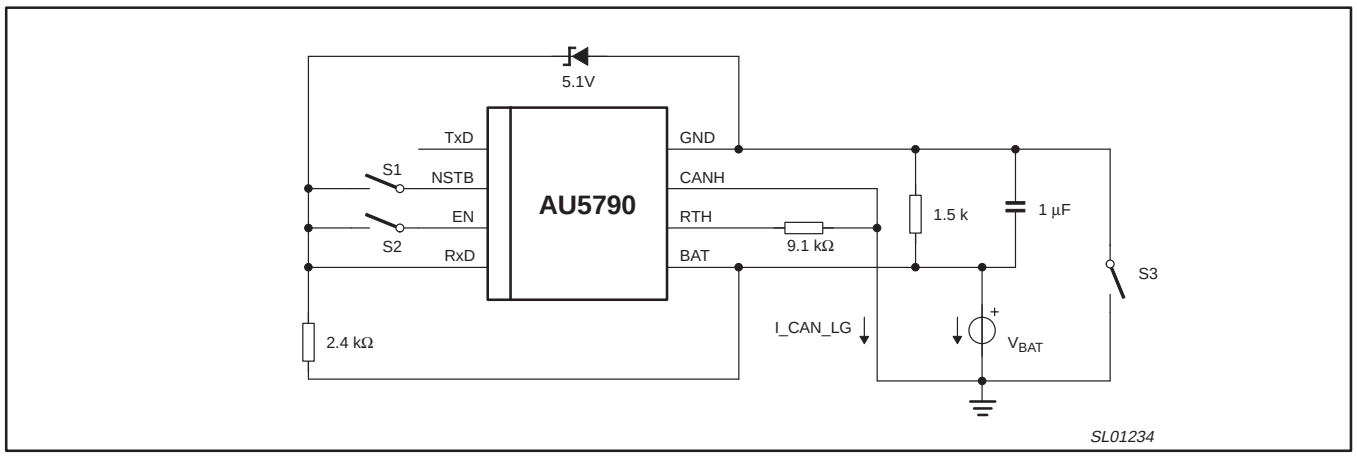
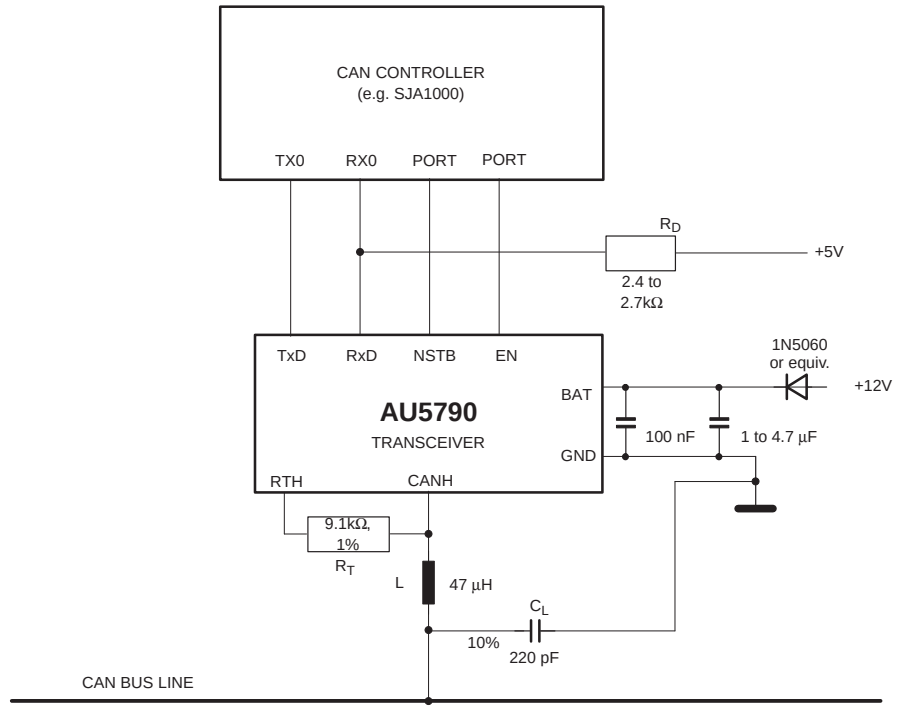


Figure 3. Loss of ground test circuit

NOTES:
Opening S3 simulates loss of module ground.
Check I_CAN_LG with the following switch positions to simulate loss of ground in all modes:
1. S1 = open = S2
2. S1 = open, S2 = closed
3. S1 = closed, S2 = open
4. S1 = closed = S2

APPLICATION INFORMATION

The information in this section is not part of the IC specification, but is presented for information purposes only. Additional information on single wire CAN networks, application circuits, and thermal management are included in application note AN2005.



Note 1 TX0 should be configured to push-pull operation, active low; e.g., Output Control Register = 1E hex.
Note 2 Recommended range for the load resistor is $3k < R_T < 11k$.

SL01200

Figure 4. Application circuit example for the AU5790

AU5790 transceivers may require additional PCB surface at ground pin(s) as heat conductor(s) in order to meet thermal requirements. See thermal characteristics section for details.

Table 2. Maximum CAN Bit Rate

MODE	MAXIMUM BIT RATE AT 0.35% CLOCK ACCURACY
Normal transmission	33.3 kbps
High-speed transmission	83.3 kbps
Sample point as % of bit time	85%
Bus Time constant, normal mode	1.0 to 4.0 µs

THERMAL CHARACTERISTICS

The AU5790 provides protection from thermal overload. When the IC junction temperature reaches the threshold (≈155 °C), the AU5790 will disable the transmitter drivers, reducing power dissipation to protect the device. The transmit function will become available again after the junction temperature drops. The thermal shutdown hysteresis is about 5 °C.

In order to avoid this transmit function shutdown, care must be taken to not overheat the IC during application. The relationships between junction temperature, ambient temperature, dissipated power, and thermal resistance can be expressed as:

$T_j = T_a + P_d * \theta_{ja}$

where: T_j is junction temperature (°C);
T_a is ambient temperature (°C);
P_d is dissipated power (W);
θ_{ja} is thermal resistance (°C/W).

Thermal Resistance

Thermal resistance is the ability of a packaged IC to dissipate heat to its environment. In semiconductor applications, it is highly dependant on the IC package, PCBs, and airflow. Thermal resistance also varies slightly with input power, the difference between ambient and junction temperatures, and soldering material.

Figures 5 and 6 show the thermal resistance as the function of the IC package and the PCB configuration, assuming no airflow.

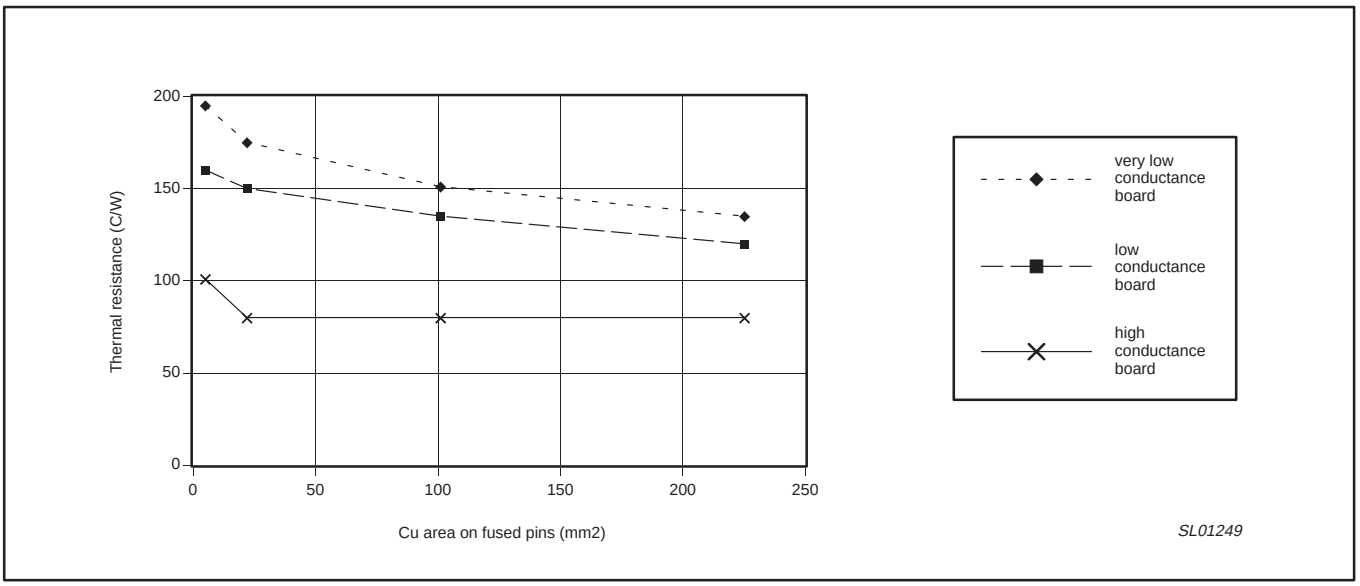


Figure 5. SO-8 Thermal Resistance vs. PCB Configuration, Note 1, 2, 3

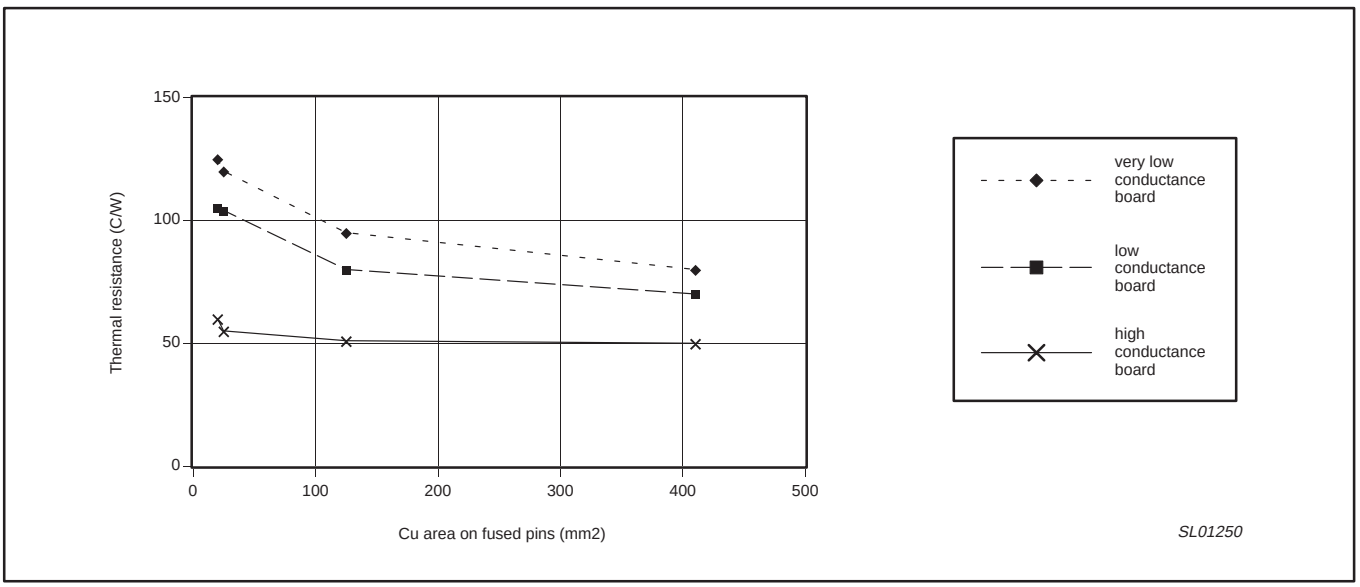


Figure 6. SO-14 Thermal Resistance vs. PCB Configuration, Note 1, 2, 3

Table 3 shows the maximum power dissipation of an AU5790 without tripping the thermal overload protection, for specified combinations of package, board configuration, and ambient temperature.

Table 3. Maximum power dissipation

Board Type	Additional Foil Area for Heat Dissipation	Θ_{JA}	P_{tot}	
			Power Dissipation Max.	
		Thermal Resistance	T_a= 85 °C	T_a= 125 °C
		K/W	mW	mW
SO-8 on High Conductance Board	Normal traces	103	631	243
	225 Sq. mm of copper foil attached to pin 8.	82	793	305
SO-8 on Low Conductance Board	Normal traces	163	399	153
	225 Sq. mm of copper attached to pin 8.	119	546	210
SO-8 on Very Low Conductance Board	Normal traces	194	335	129
	225 Sq. mm of copper attached to pin 8.	135	481	185
SO-14 on High Conductance Board	Normal traces	63	1032	397
	105 Sq. mm of copper attached to each of pins 1, 7, 8, & 14.	50	1300	500
SO-14 on Low Conductance Board	Normal traces	103	631	243
	105 Sq. mm of copper attached to each of pins 1, 7, 8, & 14.	70	929	357
SO-14 on Very Low Conductance Board	Normal traces	126	516	198
	105 Sq. mm of copper attached to each of pins 1, 7, 8, & 14.	82	793	305

NOTES:
1. The High Conductance board is based on modeling done to EIA/JEDEC Standard JESD51-7. The board emulated contains two one ounce thick copper ground planes, and top surface copper conductor traces of two ounce (0.071 mm thickness of copper).
2. The Low Conductance board is based on modeling done to EIA/JEDEC Standard EIA/JESD51-3. The board does not contain any ground planes, and the top surface copper conductor traces of two ounce (0.071 mm thickness of copper).
3. The Very Low Conductance board is based on the EIA/JESD51-3, however the thickness of the surface conductors has been reduced to 0.035 mm (also referred to as 1.0 Ounce copper).
4. The above mentioned JEDEC specifications are available from: **http://www.jedec.org/**

Power Dissipation

Power dissipation of an IC is the major factor determining junction temperature. AU5790 power dissipation in active and passive states are different. The average power dissipation is:

$$P_{tot} = P_{INT}*Dy + P_{PNINT} * (1-Dy)$$

where: P_{tot} is total dissipation power;

P_{INT} is dissipation power in an active state;

P_{PNINT} is dissipation power in a passive state;

Dy is duty cycle, which is the percentage of time that TxD is in an active state during any given time duration.

At passive state there is no current going into the load. So all of the supply current is dissipated inside the IC.

$$P_{PNINT} = V_{BAT} * I_{BATPN}$$

where: V_{BAT} is the battery voltage;

I_{BATPN} is the passive state supply current in normal mode.

In an active state, part of the supply current goes to the load, and only part of the supply current dissipates inside the IC, causing an incremental increase in junction temperature.

$$P_{INT} = P_{BATAN} – P_{LOADN}$$

where: P_{BATAN} is active state battery supply power in normal mode;

$$P_{BATAN} = V_{BAT} * I_{BATAN}$$

P_{LOADN} is load power consumption in normal mode.

$$P_{LOADN} = V_{CANHN} * I_{LOADN}$$

where: I_{BATAN} is active state supply current in normal mode;

V_{CANHN} is bus output voltage in normal mode;

I_{LOADN} is current going through load in normal mode.

$$I_{LOAD} = V_{CANHN}/R_{LOAD}$$

$$I_{BATN} = I_{LOAD} + I_{INT}$$

where: I_{INT} is an active state current dissipated within the IC in normal mode.

I_{INT} will decrease slightly when the node number decreases. To simplify this analysis, we will assume I_{INT} is fixed.

$$I_{INT} = I_{BATN} \text{ (32 nodes)} – I_{LOAD} \text{ (32 nodes)}$$

I_{BATN} (32 nodes) may be found in the DC Characteristics table.

A power dissipation example follows. The assumed values are chosen from specification and typical applications.

Assumptions:

V_{BAT} = 13.4 V
R_T = 9.1 kΩ
32 nodes
I_{BATPN} = 2 mA
I_{BATN} (32 nodes) = 35 mA
V_{CANHN} = 4.55 V
Duty cycle = 50%

Computations:

R_{LOAD} = 9.1 kΩ / 32 = 284.4 Ω
P_{PNINT} = 13.4 V × 2 mA = 26.8 mW
I_{LOAD} = 4.55 V / 284.4 Ω = 16mA
P_{LOADN} = 4.55 V × 16 mA = 72.8 mW
I_{INT} = 35 mA - 16 mA = 19 mA
P_{BATAN} = 13.4 V × 35 mA = 469 mW
P_{INT} = 469 mW - 72.8 mW = 396.2 mW
P_{tot} = 396.2 mW × 50% + 26.8 mW × (1-50%) = 211.5 mW

Additional examples with various node counts are shown in Table 4.

Table 4. Representative Power Dissipation Analyses

Nodes	R_{LOAD} (Ω)	V_{BAT} (V)	I_{BATPN} (mA)	P_{PNINT} (mW)	V_{CANHN} (V)	I_{LOAD} (mA)	I_{BATN} (mA)	I_{INT} (mA)	P_{INT} (mW)	Dcycle	P_{tot} (mW)
2	4550	**13.4**	2	26.8	4.55	1	20	19	263.5	0.5	145.1
10	910	**13.4**	2	26.8	4.55	5	24	19	298.9	0.5	162.8
20	455	**13.4**	2	26.8	4.55	10	29	19	343.1	0.5	184.9
32	284.4	**13.4**	2	26.8	4.55	16	35	19	396.2	0.5	211.5
2	4550	**26.5**	2	53	4.55	1	20	19	525.5	0.5	289.2
10	910	**26.5**	2	53	4.55	5	24	19	613.3	0.5	333.1
20	455	**26.5**	2	53	4.55	10	29	19	723	0.5	388
32	284.4	**26.5**	2	53	4.55	16	35	19	854.7	0.5	453.8

By knowing the maximum power dissipation, and the operation ambient temperature, the required thermal resistance without tripping the thermal protection can be calculated, as shown in Figure 7. Then from Figure 5 or 6, a suitable PCB can be selected.

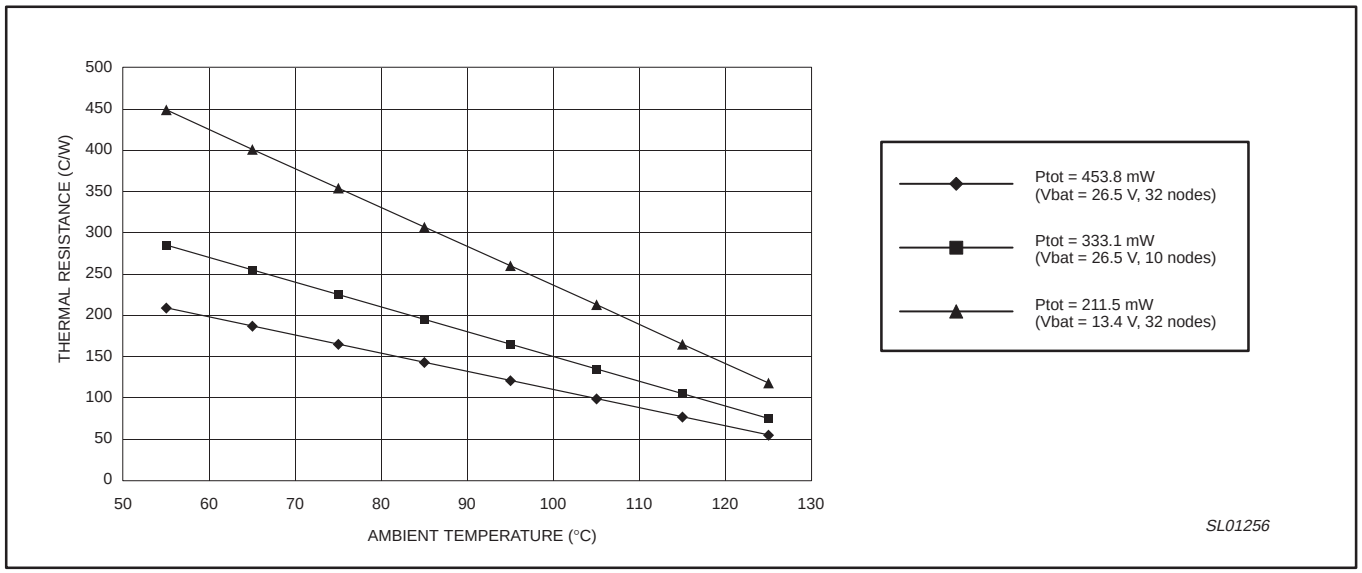
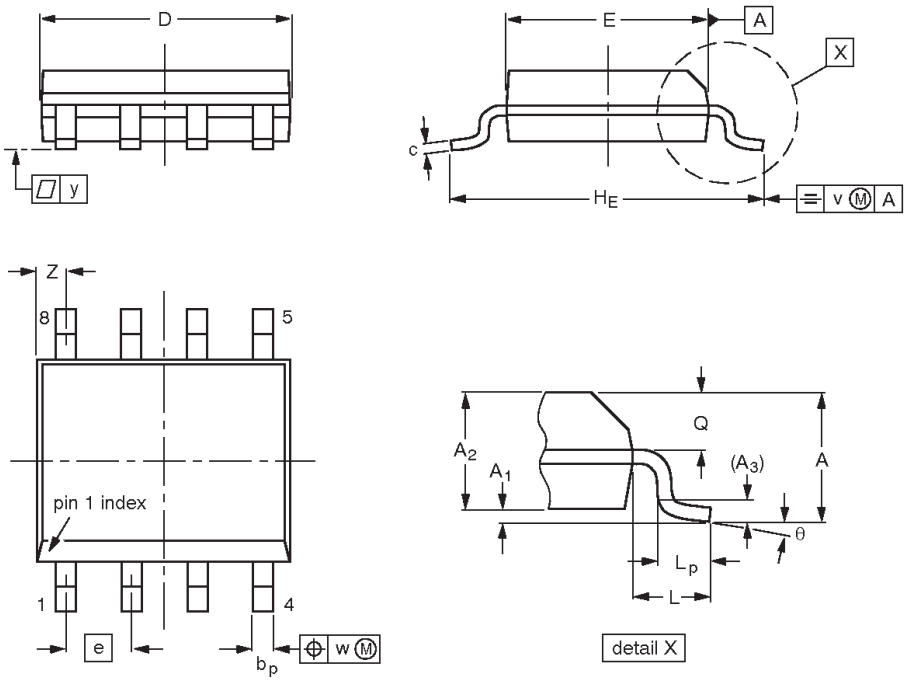
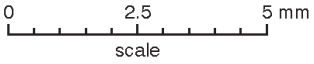


Figure 7. Required Thermal Resistance vs. Ambient Temperature and Power Dissipation

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

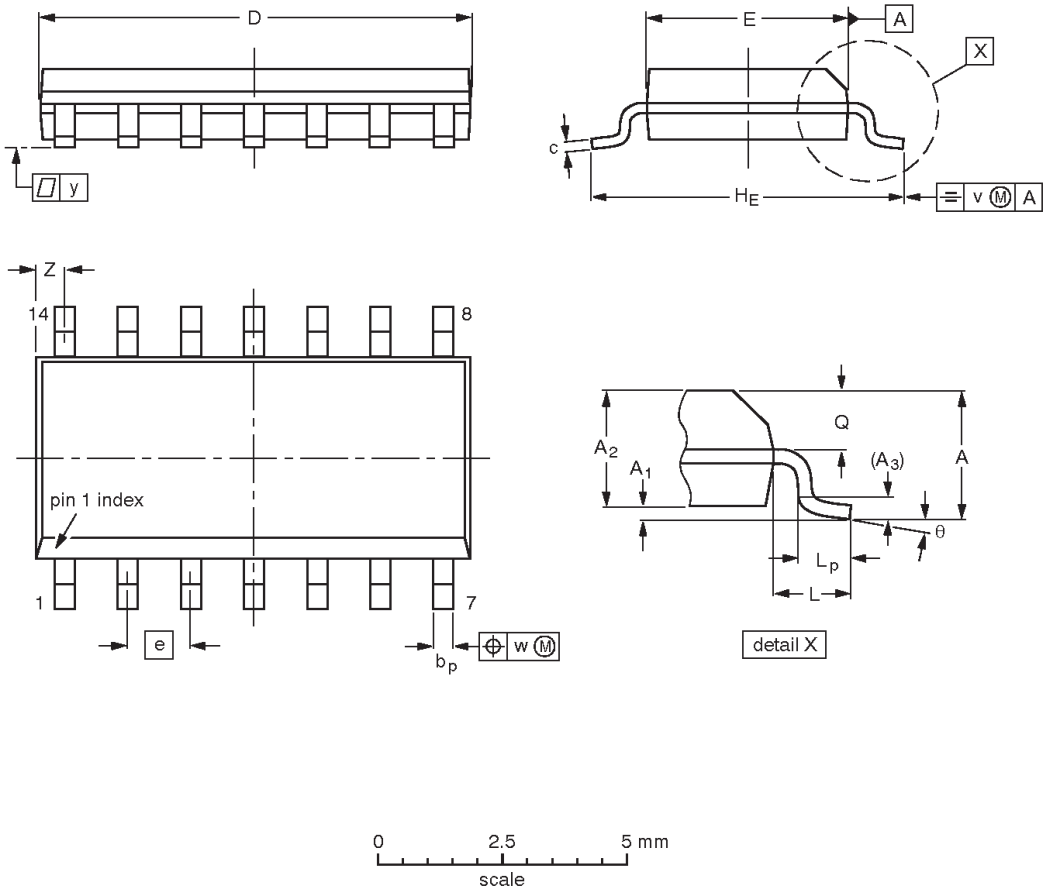
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

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