SMP4050-12UTG

Technical Data
Data Sheet N1737 Rev.-

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Description

The SMP4050 integrates low capacitance diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb up to 20A per IEC61000-4-5 (tp=8/20μs) without performance degradation and a minimum ±30kV ESD per IEC61000-4-2 International Standard. Their low loading capacitance also makes them ideal for protecting high speed signal pins.

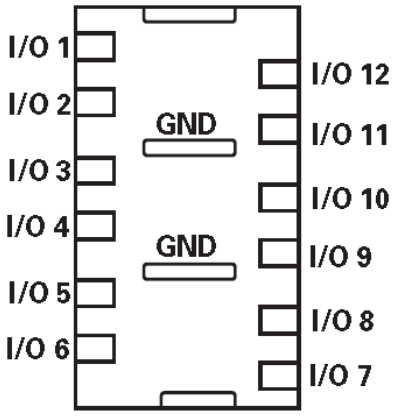
Features

- ESD protection in accordance with:
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-5 (lightning) 20A (8/20μs)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Low capacitance: 4.4pF typical per I/O
- Low leakage current of 1μA (MAX) at 2.5V

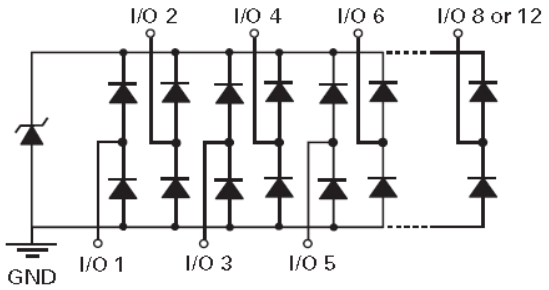
Applications

- LCD/PDP TVs
- Desktops
- Game Consoles
- Set Top Boxes
- Notebooks

Pinout



Functional Block Diagram



Note: Pinout diagrams above shown as device footprint on circuit board.

Technical Data
Data Sheet N1737 Rev.-

Green Products

Ordering Information:

Device	Package	Min. Order Qty.
SMP4050-12UTG	µDFN-12 (Pb-Free)	3000

Absolute Maximum Ratings:

Parameter	Symbol	Value	Unit
Peak Pulse Current (tp=8/20µs)	I_{PP}	20	A
Peak Pulse Power (tp=8/20µs)	P_{PK}	300	W
Operating Junction Temperature Range	T_{OP}	-40 to + 85	°C
Storage Temperature Range	T_{STOR}	-50 to + 150	°C

Thermal Information:

Parameter	Value	Unit
Storage Temperature Range	-65 to + 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature(Soldering 10s)	260	°C

Electrical Characteristics: (T_{OP}=25°C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	2.5	V
Snap Back Voltage	V_{SB}	I_{SB}=50mA	2.0	-	-	V
Reverse Leakage Current	I_{LEAK}	V_R = 2.5V, I/O to ground	-	0.5	1.0	µA
Clamping Voltage[1]	V_C	I_{PP} = 1A, tp=8/20µs, Fwd	-	4.5	-	V
		I_{PP} = 10A, tp=8/20µs, Fwd	-	8.9	-	V
		I_{PP} = 20A, tp=8/20µs, Fwd		13.2	-	V
ESD With stand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30	-	-	kV
		IEC61000-4-2 (Air)	±30	-	-	kV
Junction Capacitance[1]	$C_{I/O-GND}$	V_R = 0V, f_{SIG} = 1MHz	-	4.5	5.0	pF
Junction Capacitance[1]	$C_{I/O-I/O}$	V_R = 0V, f_{SIG} = 1MHz	-	2.2	-	pF

Note: 1. Parameter is guaranteed by design and/or device characterization.

Technical Data
Data Sheet N1737 Rev.-

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Marking Diagram

PH12

Where PH12 is SMP4050-12UTG

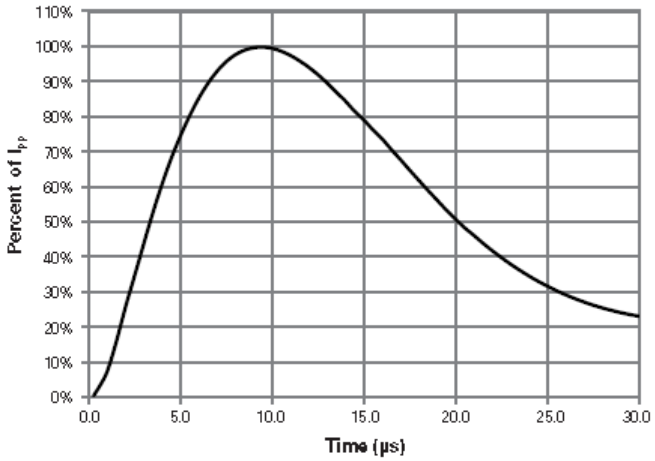
PH12 = Part Name

Part Name Information

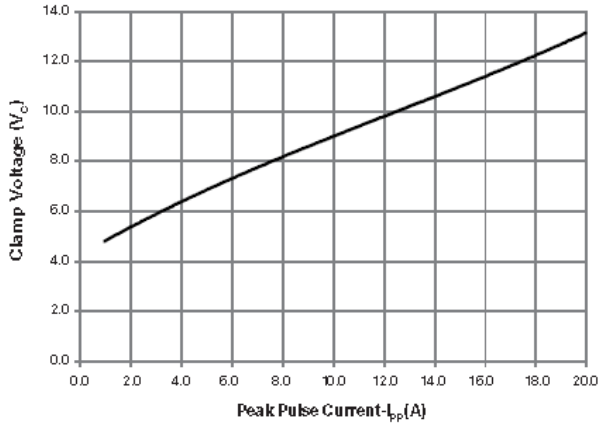
SMP 4050 – 12 U T G

- G= Green
- T= Tape & Reel
- Package U = µDFN-12
- Number of Channels
- Series
- Silicon Protection Array

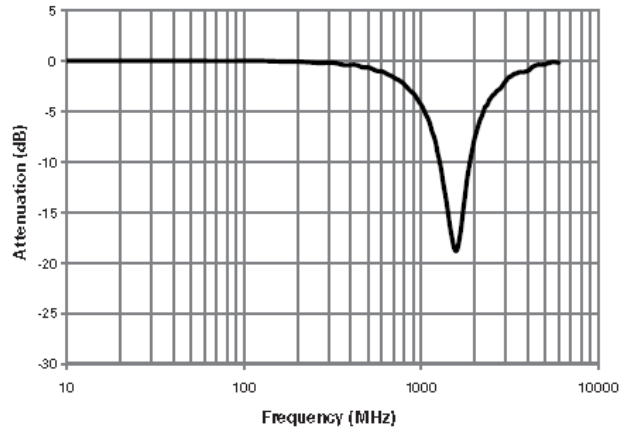
Pulse Waveform



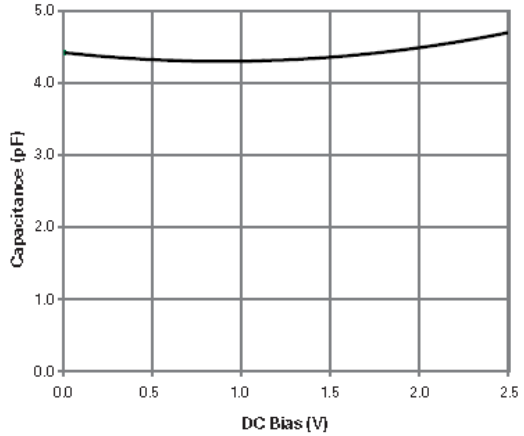
Clamping Voltage vs. I_{PP}



Insertion Loss (S21) I/O to GND



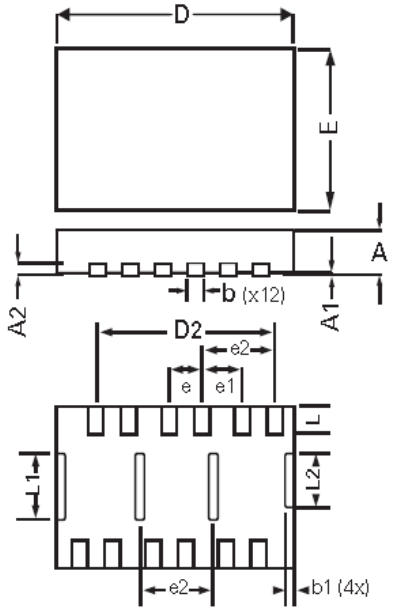
Capacitance vs. Bias



Technical Data
Data Sheet N1737 Rev.-

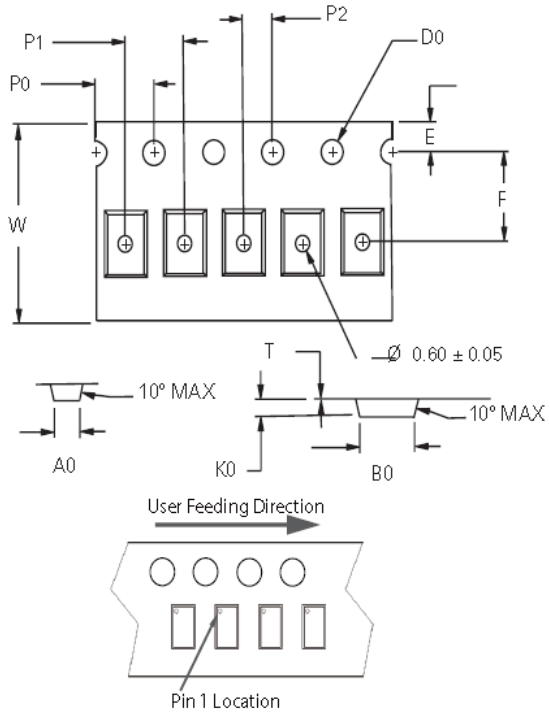
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Mechanical Dimensions (In mm/Inches):



Symbol	µDFN-12			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.65	0.020	0.026
A1	0.00	0.05	0.00	0.002
A2	0.150 REF		0.006REF	
b	0.15	0.25	0.006	0.010
b1	0.10	0.30	0.004	0.012
D	3.40	3.60	0.134	0.142
D2	2.70		0.106	
E	2.40	2.60	0.095	0.103
e	0.50 BSC		0.020 BSC	
e1	0.60 BSC		0.024 BSC	
e2	1.10 BSC		0.044 BSC	
L	0.30	0.40	0.012	0.016
L1	0.90	1.10	0.036	0.044
L2	0.70	0.90	0.028	0.036

Embossed Carrier Tape & Reel Specification µDFN-12



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A0	2.63	2.83	0.104	0.112
B0	3.63	3.83	0.143	0.151
D0	1.40	1.60	0.055	0.063
E	1.65	1.85	0.065	0.073
F	5.45	5.55	0.215	0.219
K0	0.85	1.05	0.033	0.041
P0	3.90	4.10	0.154	0.161
P1	3.90	4.10	0.154	0.161
P2	1.95	2.05	0.077	0.081
T	0.18	0.22	0.007	0.009
W	11.90	12.30	0.469	0.484

Technical Data ***Green Products***
Data Sheet N1737 Rev.-

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