

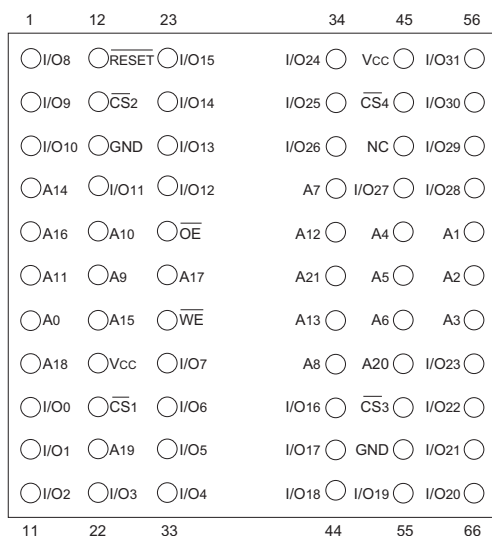
**4MX32 5V FLASH MODULE, SMD 5962-97612 (pending)** PRELIMINARY***FEATURES**

- Access Times of 100, 120, 150ns
- Packaging:
 - 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).
 - 68 lead, 40mm Low Profile CQFP (Package 502), 3.5mm (0.140") height.
 - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990CQFJ footprint (Fig. 3)
- Sector Architecture
 - 32 equal size sectors of 64KBytes per each 2Mx8 chip
 - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 4Mx32
- User configurable as 8Mx16 or 16Mx8 in HIP and G4T packages.
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V $\pm$ 10% Supply.
- Low Power CMOS
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET pin resets internal state machine to the read mode.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity

**This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

Note:

For programming information refer to Flash Programming 16M5 Application Note.

FIG. 1 PIN CONFIGURATION FOR WF4M32-XH2X5**TOP VIEW****PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-21	Address Inputs
WE	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
RESET	Reset

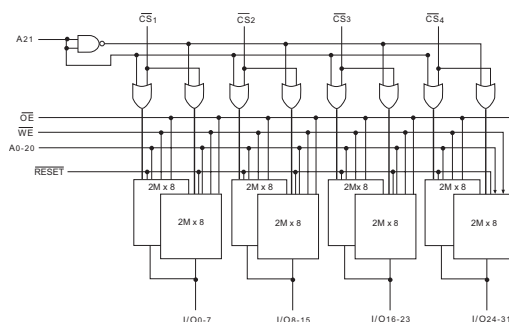
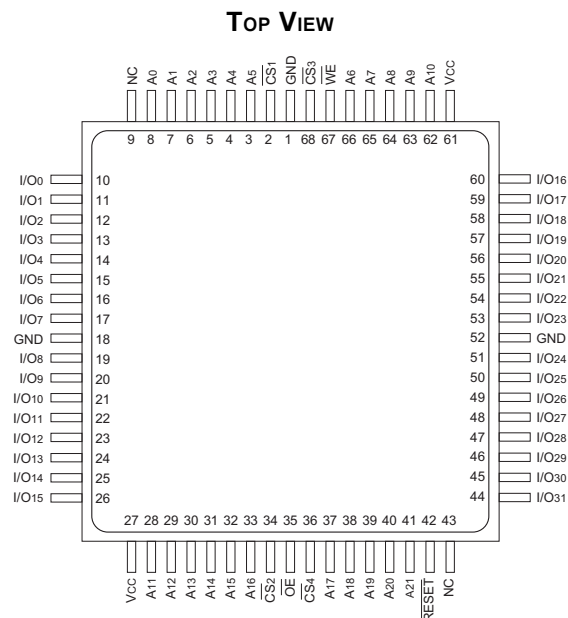
BLOCK DIAGRAM



FIG. 2 PIN CONFIGURATION FOR WF4M32-XG4TX5



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-21	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
RESET	Reset
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

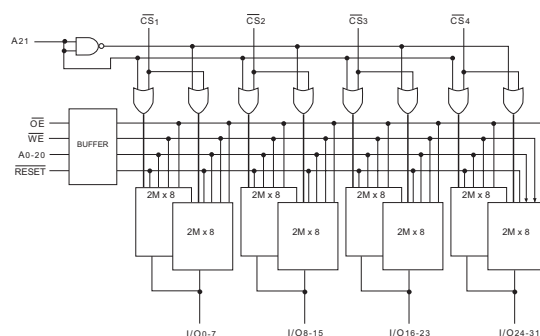
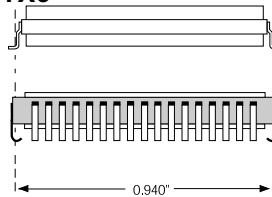
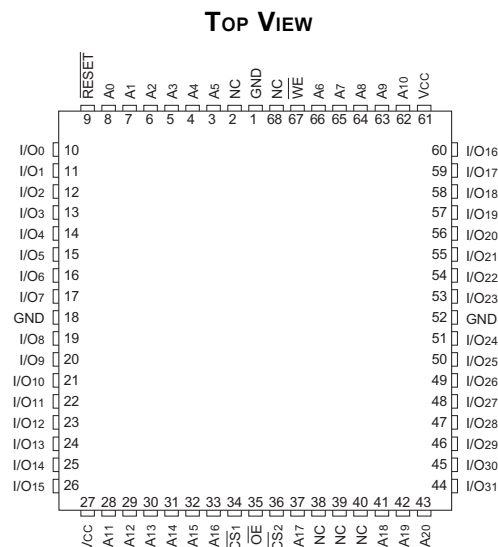


FIG. 3 PIN CONFIGURATION FOR WF4M32-XG2TX5

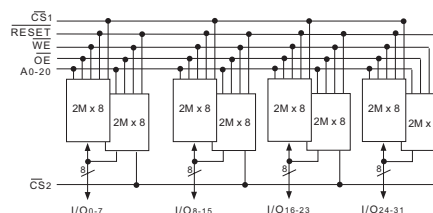


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS1-2}$	Banks Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
RESET	Reset

BLOCK DIAGRAM



Note: $\overline{CS1}$ & $\overline{CS2}$ are used as bank select



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _I	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{stg}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE (pF)

(TA = +25°C, V_{IN} = 0V, F = 1.0MHz)

Parameter	Symbol	HIP (H2)	CQFP (G2T)	CQFP (G4T)
OE capacitance	C _{OE}	75	75	20
WE capacitance	C _{WE}	75	75	20
CS capacitance	C _{CS}	20	50	20
Data I/O capacitance	C _{IO}	30	30	30
Address input capacitance	C _{AD}	75	75	20

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C

DC CHARACTERISTICS - CMOS COMPATIBLE (V_{CC} = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Symbol	Conditions	HIP		G2T		G4T		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _I	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		320		215		345	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		420		295		445	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, CS = V _{IH} , f = 5MHz, RESET = $\overline{V_{IH}}$		20		2.0		95	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45		0.45		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		0.85 x V _{CC}		0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	3.2	4.2	3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

HIP = 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).

G2T = 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square. Designed to fit JEDEC 68 lead 0.990" CQFP footprint (Fig. 3) (Package 509)

G4T = 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140") (Package 502)



AC CHARACTERISTICS FOR G2T PACKAGE – WRITE/ERASE/PROGRAM OPERATIONS - WE CONTROLLED (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	100		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		ns
Write Enable Pulse Width	tWLWH	tWP	45		50		50		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
Data Setup Time	tDVWH	tDS	45		50		50		ns
Data Hold Time	tWHDx	tDH	0		0		0		ns
Address Hold Time	tWLAX	tAH	45		50		50		ns
Write Enable Pulse Width High	tWHWL	tWPH	20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300	μs
Sector Erase (2)	tWHWH2			15		15		15	sec
Read Recovery Time before Write	tGHWL		0		0		0		μs
Vcc Setup Time	tVCS		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		tOEH	10		10		10		ns
RESET Pulse Width		tRP	500		500		500		ns

NOTES:

1. Typical value for tWHWH1 is 7μs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS FOR G2T PACKAGE – READ-ONLY OPERATIONS (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	100		120		150		ns
Address Access Time	tAVQV	tACC		100		120		150	ns
Chip Select Access Time	tELQV	tCE		100		120		150	ns
Output Enable to Output Valid	tGLQV	tOE		40		50		55	ns
Chip Select High to Output High Z (1)	tEHQZ	tDF		20		30		35	ns
Output Enable High to Output High Z (1)	tGHQZ	tDF		20		30		35	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	tAXQX	tOH	0		0		0		ns
RST Low to Read Mode (1)		tready		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS FOR G2T PACKAGE – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED (VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	100		120		150		ns
Write Enable Setup Time	tWLEL	tWS	0		0		0		ns
Chip Select Pulse Width	tLELH	tCP	45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		ns
Data Setup Time	tDVEH	tDS	45		50		50		ns
Data Hold Time	tEHDX	tDH	0		0		0		ns
Address Hold Time	tELAX	tAH	45		50		50		ns
Chip Select Pulse Width High	tEHEL	tCPH	20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300	μs
Sector Erase Time (2)	tWHWH2			15		15		15	sec
Read Recovery Time	tGHEL		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		tOBH	10		10		10		ns

NOTES:

1. Typical value for tWHWH1 is 7μs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.



AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	100		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		ns
Write Enable Pulse Width	tWLWH	tWP	45		50		50		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
Data Setup Time	tDVWH	tDS	45		50		50		ns
Data Hold Time	tWHDH	tDH	15		15		15		ns
Address Hold Time (1)	tWLAX	tAH	45		50		50		ns
Write Enable Pulse Width High (2)	tWHWL	tWPH	20		20		20		ns
Duration of Byte Programming Operation (3)	tWHWH1			300		300		300	μs
Sector Erase (4)	tWHWH2			15		15		15	sec
Read Recovery Time before Write	tGHWL		0		0		0		μs
VCC Setup Time	tVCS		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (5)				256		256		256	sec
Output Enable Hold Time (6)		tOEH	10		10		10		ns
RESET Pulse Width		tRP	500		500		500		ns

NOTES:

1. A21 must be held constant until $\overline{WE}$ or $\overline{CS}$ go high, whichever occurs first.
2. Guaranteed by design, but not tested.
3. Typical value for tWHWH1 is 7μs.
4. Typical value for tWHWH2 is 1sec.
5. Typical value for Chip Erase Time is 32sec.
6. For Toggle and Data Polling.

AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – READ-ONLY OPERATIONS (VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	100		120		150		ns
Address Access Time	tAVQV	tACC		100		120		150	ns
Chip Select Access Time	tELQV	tCE		100		120		150	ns
Output Enable to Output Valid	tGLQV	tOE		50		50		55	ns
Chip Select High to Output High Z	tEHQZ	tDF		40		45		45	ns
Output Enable High to Output High Z	tGHQZ	tDF		40		45		45	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	tAXQX	tOH	0		0		0		ns
RST Low to Read Mode		tready		20		20		20	μs



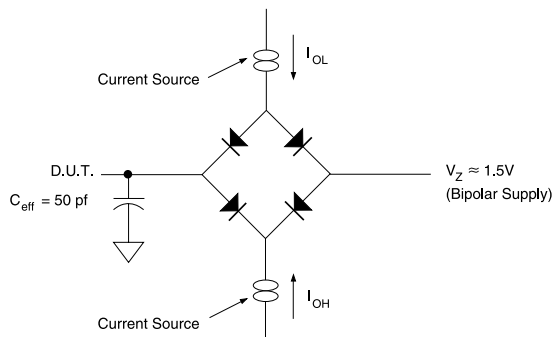
AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED (VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	100		120		150		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		ns
Chip Select Pulse Width	t _{LELH}	t _{CP}	45		50		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{EHDX}	t _{DH}	15		15		15		ns
Address Hold Time (1)	t _{ELAX}	t _{AH}	45		50		50		ns
Chip Select Pulse Width High	t _{EH}	t _{CPH}	20		20		20		ns
Duration of Byte Programming Operation (2)	t _{WHWH1}			300		300		300	μs
Sector Erase Time (3)	t _{WHWH2}			15		15		15	sec
Read Recovery Time	t _{GHEL}		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (4)				256		256		256	sec
Output Enable Hold Time (5)		t _{OBH}	10		10		10		ns

NOTES:

1. A21 must be held constant until $\overline{WE}$ or $\overline{CS}$ go high, whichever occurs first.
2. Typical value for t_{WHWH1} is 7μs.
3. Typical value for t_{WHWH2} is 1sec.
4. Typical value for Chip Erase Time is 32sec.
5. For Toggle and Data Polling.

FIG. 4 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5 RESET TIMING DIAGRAM

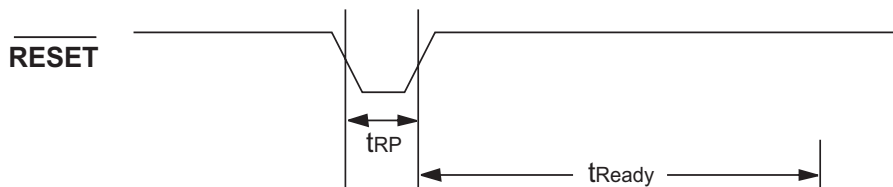
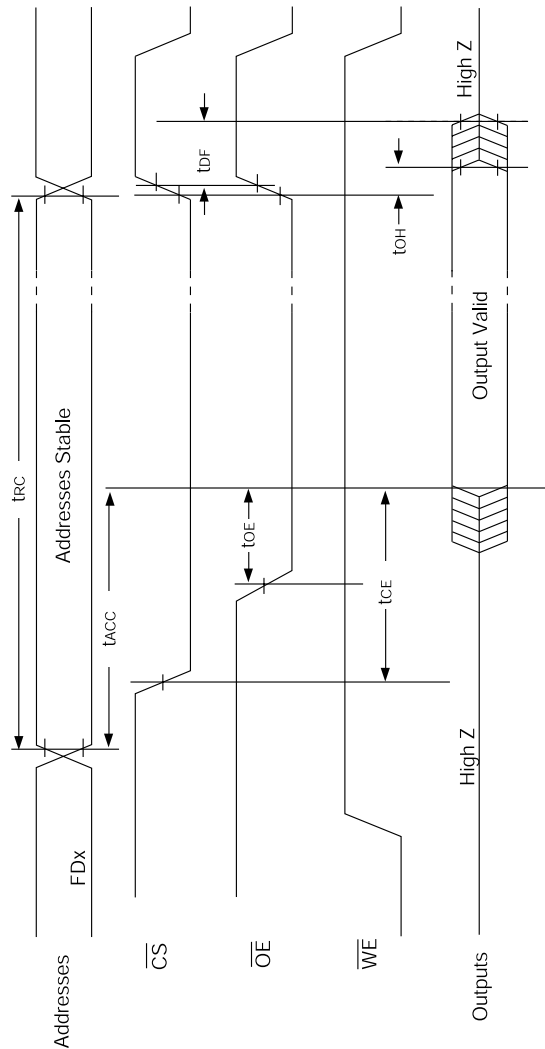
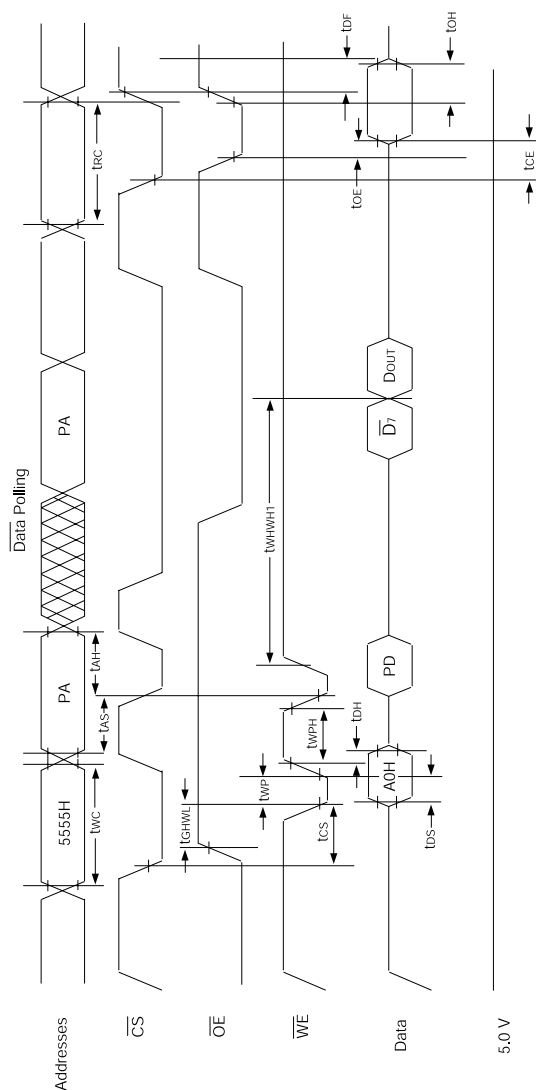




FIG. 6 AC WAVEFORMS FOR READ OPERATIONS

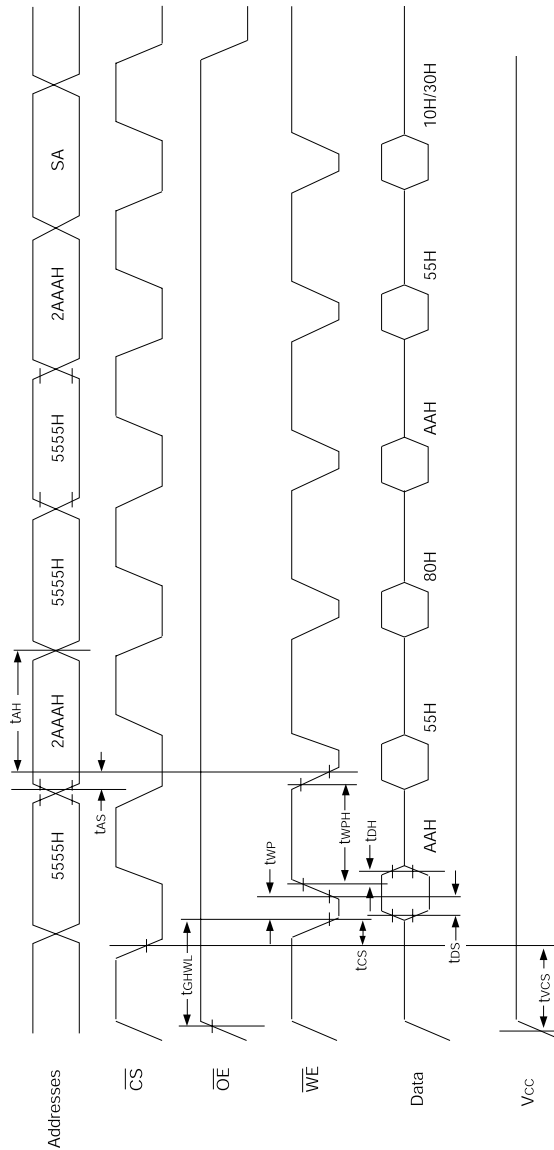




1. PA is the address of the memory location to be programmed.
2. $\overline{PD}$ is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. $Dout$ is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 8 AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:

1. SA is the sector address for Sector Erase.



FIG. 9 AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS

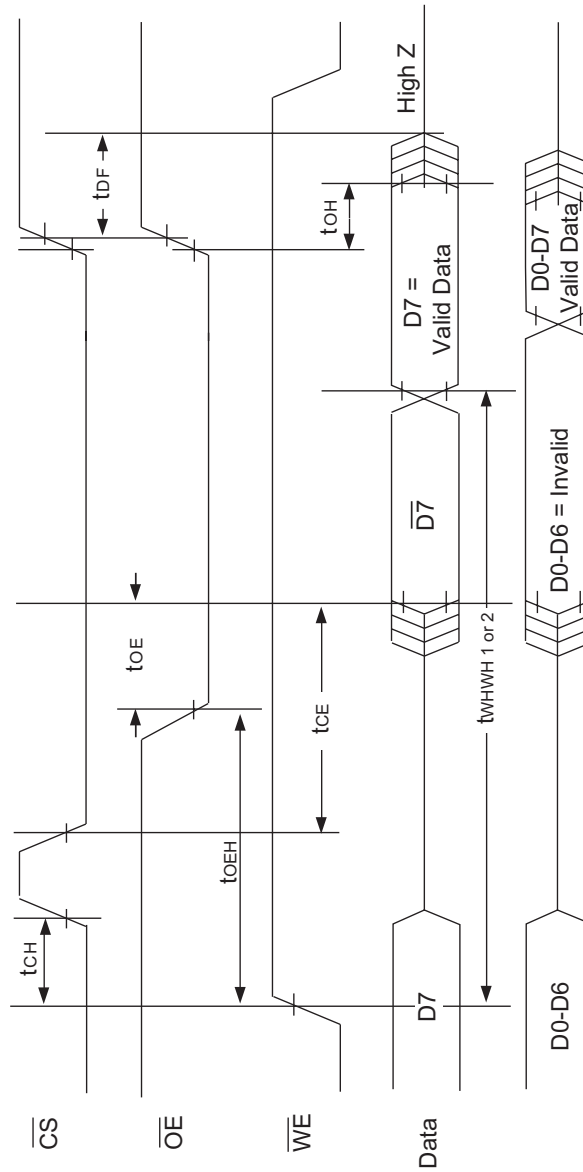
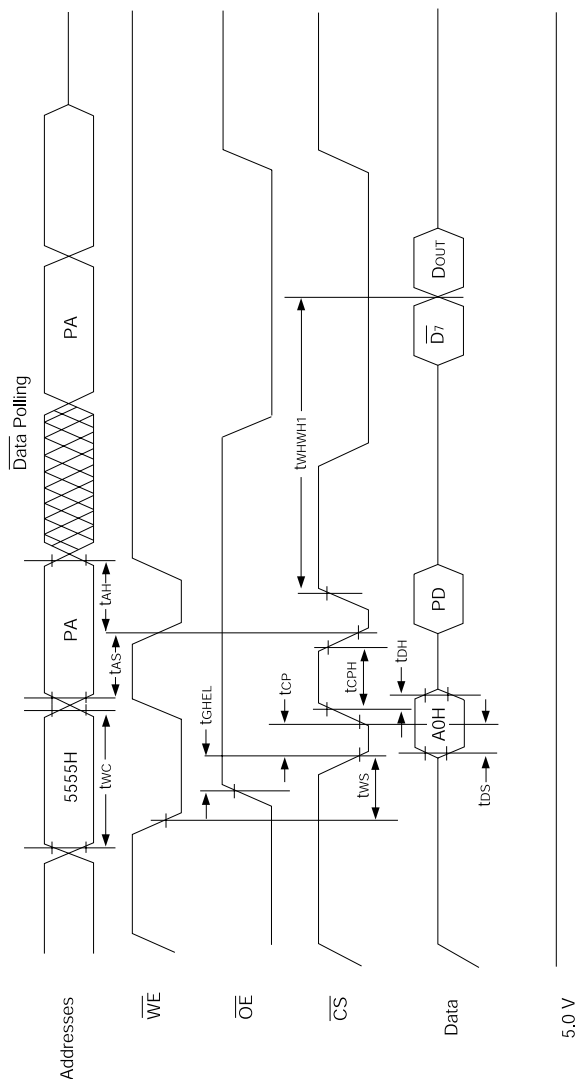




FIG. 10 ALTERNATE $\overline{\text{CS}}$ CONTROLLED PROGRAMMING OPERATION TIMINGS

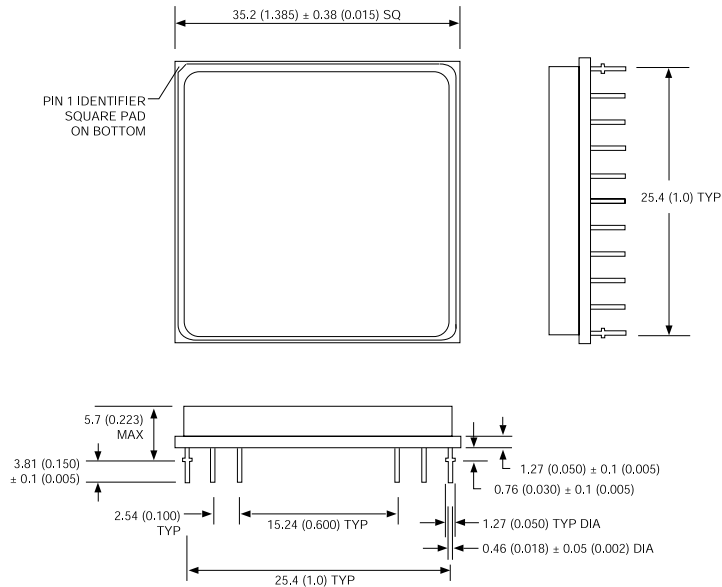


Notes:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{\text{D7}}$ is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

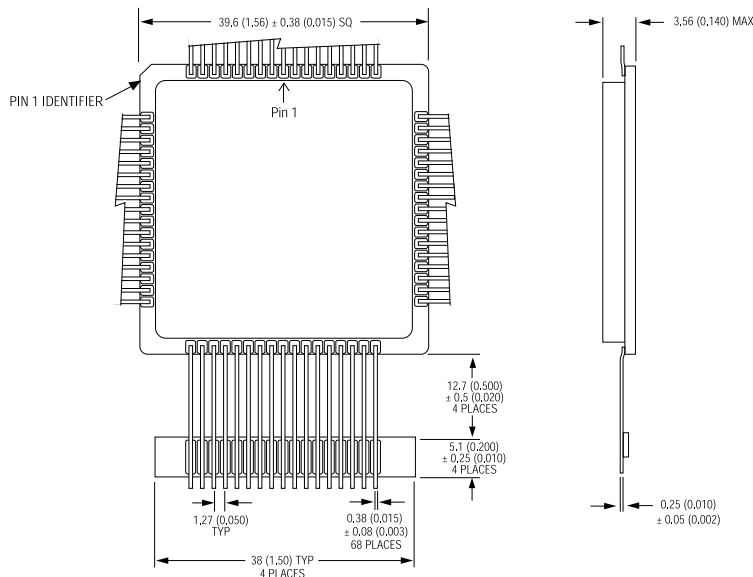


PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

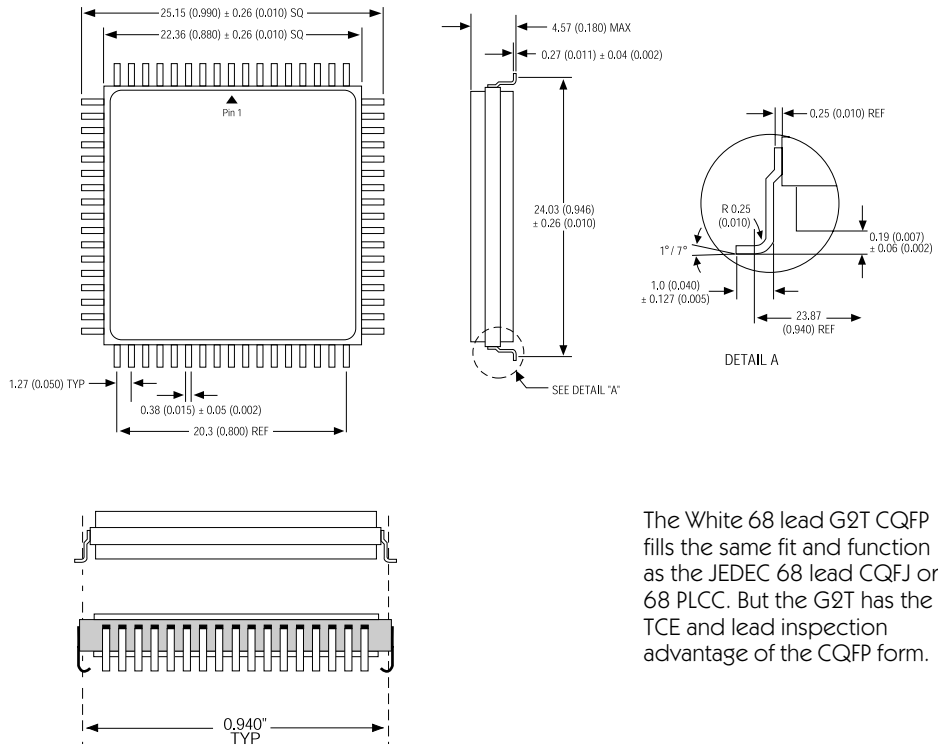
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)

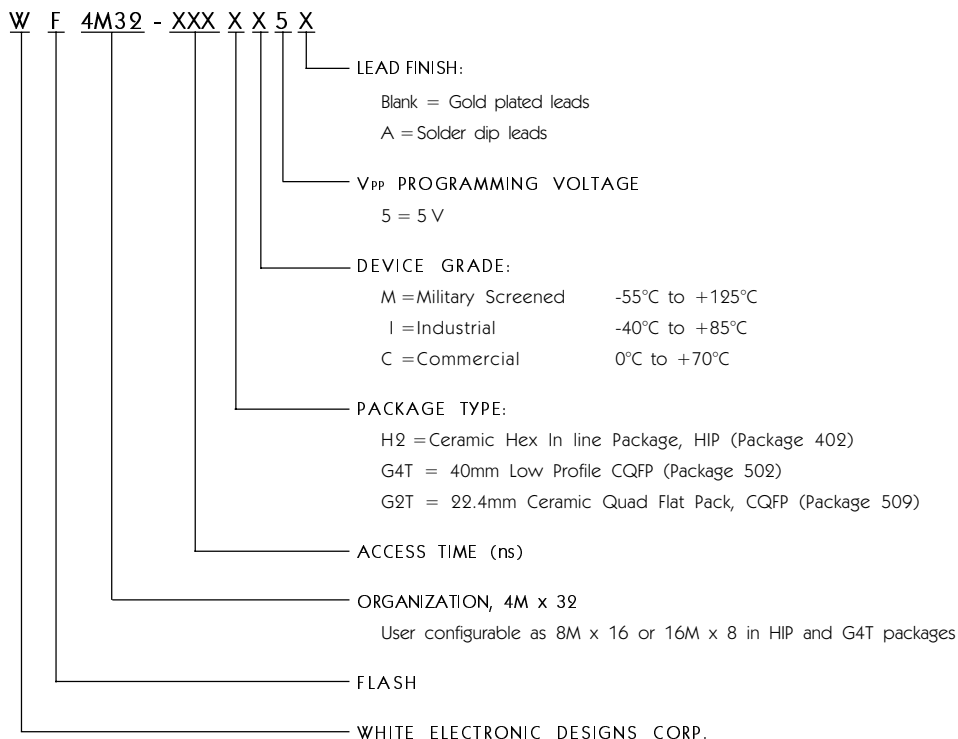


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION



DEVICE	TYPE	SECTOR	SIZE	SPEED	PACKAGE	SMD NO.
4M x 32 5V Flash Module		64KByte	150ns	66 pin HIP (H2)	5962-97612 01HXX*	
4M x 32 5V Flash Module		64KByte	120ns	66 pin HIP (H2)	5962-97612 02HXX*	
4M x 32 5V Flash Module		64KByte	100ns	66 pin HIP (H2)	5962-97612 03HXX*	
4M x 32 5V Flash Module		64KByte	150ns	68 lead CQFP Low Profile (G4T)	5962-97612 01HXX*	
4M x 32 5V Flash Module		64KByte	120ns	68 lead CQFP Low Profile (G4T)	5962-97612 02HXX*	
4M x 32 5V Flash Module		64KByte	100ns	68 lead CQFP Low Profile (G4T)	5962-97612 03HXX*	
4M x 32 5V Flash Module		64KByte	150ns	68 lead CQFP Low Profile (G2T)	5962-97612 01HXX*	
4M x 32 5V Flash Module		64KByte	120ns	68 lead CQFP Low Profile (G2T)	5962-97612 02HXX*	
4M x 32 5V Flash Module		64KByte	100ns	68 lead CQFP Low Profile (G2T)	5962-97612 03HXX*	

*Pending