JANSR2N7278

Formerly FRL234R4

June 1998

4A, 250V, 0.700 Ohm, Rad Hard, N-Channel Power MOSFET

Features

- **4A, 250V, $r_{DS(ON)}$ = 0.700Ω**
- **Total Dose**
  - **Meets Pre-RAD Specifications to 100K RAD (Si)**
- **Dose Rate**
  - **Typically Survives 3E9 RAD (Si)/s at 80% BV_{DSS}**
  - **Typically Survives 2E12 if Current Limited to I_{DM}**
- **Photo Current**
  - **4nA Per-RAD(Si)/s Typically**
- **Neutron**
  - **Maintain Pre-RAD Specifications for 1E13 Neutrons/cm^2**
  - **Usable to 1E14 Neutrons/cm^2**

Ordering Information

PART NUMBER	PACKAGE	BRAND
JANSR2N7278	TO-205AF	JANSR2N7278

Die family TA17633.

MIL-PRF-19500/604.

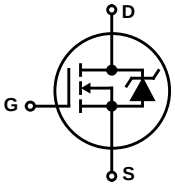
Description

The Intersil Corporation has designed a series of SECOND GENERATION hardened power MOSFETs of both N-Channel and P-Channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD (Si) and 1000K RAD (Si) with neutron hardness ranging from 1E13 for 500V product to 1E14 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (no) exposures. Design and processing efforts are also directed to enhance survival to dose rate (GAMMA DOT) exposure.

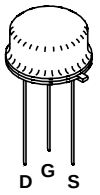
Also available at other radiation and screening levels. See us on the web, Intersil's home page: http://www.semi.harris.com. Contact your local Intersil Sales Office for additional information.

Symbol



Packaging

TO-205AF



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
http://www.intersil.com or 407-727-9207 | Copyright © Intersil Corporation 1999

File Number **4295.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		JANSR2N7278	UNITS
Drain to Source Voltage	V_{DS}	250	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	250	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	4	A
$T_C = 100^oC$	I_D	2	A
Pulsed Drain Current	I_{DM}	12	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = 25^oC$	P_T	25	W
$T_C = 100^oC$	P_T	10	W
Linear Derating Factor		0.20	$W/^oC$
Single Pulsed Avalanche Current, L = 100µH, (See Test Figure)	I_{AS}	12	A
Continuous Source Current (Body Diode)	I_S	4	A
Pulsed Source Current (Body Diode)	I_{SM}	12	A
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Lead Temperature (During Soldering) (Distance >0.063in (1.6mm) from Case, 10s Max)	T_L	300	^oC
Weight (Typical)		1.0	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA	$T_C = -55^oC$	-	-	5.0	V
			$T_C = 25^oC$	2.0	-	4.0	V
			$T_C = 125^oC$	1.0	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200V, V_{GS} = 0V	$T_C = 25^oC$	-	-	25	µA
			$T_C = 125^oC$	-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	$T_C = 25^oC$	-	-	100	nA
			$T_C = 125^oC$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	V_{GS} = 10V, I_D = 4A		-	-	2.94	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 2A, V_{GS} = 10V	$T_C = 25^oC$	-	-	0.700	Ω
			$T_C = 125^oC$	-	-	1.68	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 4A, R_L = 31.3Ω, V_{GS} = 10V, R_{GS} = 25Ω		-	-	35	ns
Rise Time	t_r			-	-	85	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	195	ns
Fall Time	t_f			-	-	75	ns
Total Gate Charge (Not on Slash Sheet)	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 125V, I_D = 4A	-	-	120	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	-	62	nC
Threshold Gate Charge (Not on Slash Sheet)	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	-	4	nC
Gate Charge Source	Q_{gs}			-	-	12	nC
Gate Charge Drain	Q_{gd}			-	-	30	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	175	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4A	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	-	800	ns

Electrical Specifications up to 100K RAD $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts	(Note 3)	BV_{DSS}	V_{GS} = 0, I_D = 1mA	250	-	V
Gate to Source Threshold Volts	(Note 3)	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 1mA	2.0	4.0	V
Gate to Body Leakage	(Notes 2, 3)	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	100	nA
Zero Gate Leakage	(Note 3)	I_{DSS}	V_{GS} = 0, V_{DS} = 200V	-	25	µA
Drain to Source On-State Volts	(Notes 1, 3)	$V_{DS(ON)}$	V_{GS} = 10V, I_D = 4A	-	2.94	V
Drain to Source On Resistance	(Notes 1, 3)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2A	-	0.700	Ω

NOTES:

1. Pulse test, 300µs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both V_{GS} = 10V, V_{DS} = 0V and V_{GS} = 0V, V_{DS} = 80% BV_{DSS}.

Typical Performance Curves Unless Otherwise Specified

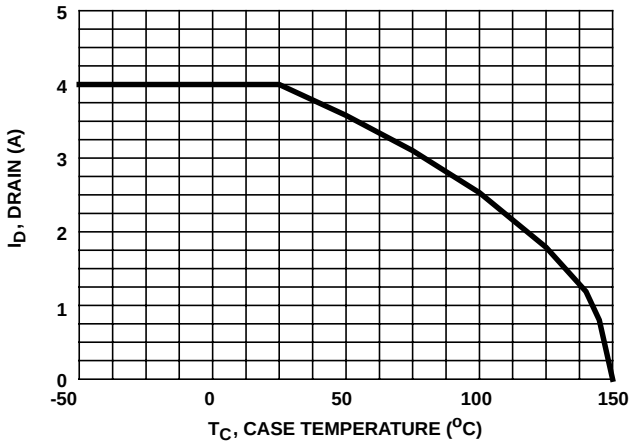


FIGURE 1. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

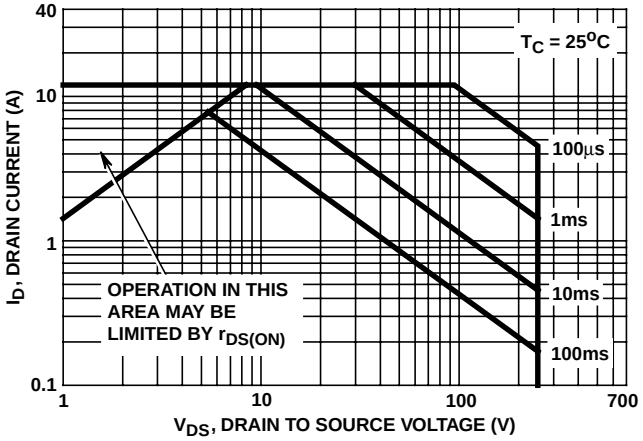


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

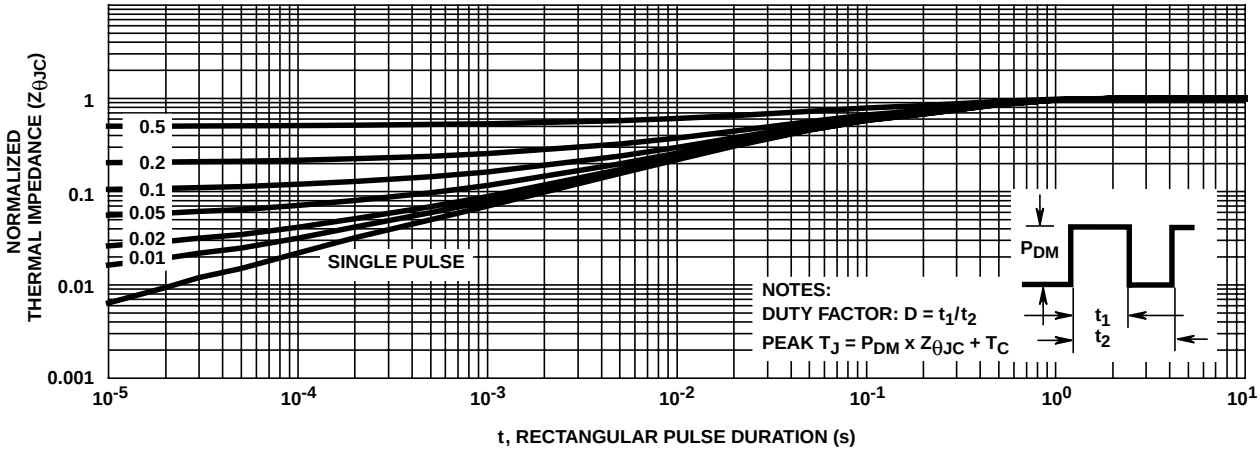


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

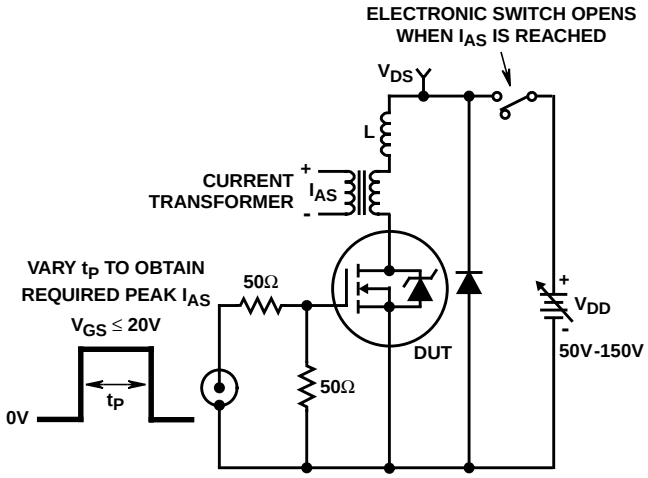


FIGURE 4. UNCLAMPED ENERGY TEST CIRCUIT

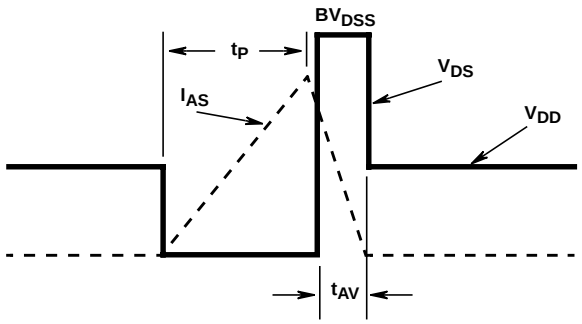


FIGURE 5. UNCLAMPED ENERGY WAVEFORMS

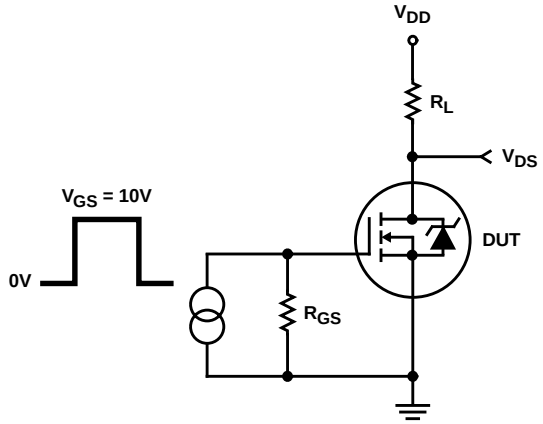


FIGURE 6. RESISTIVE SWITCHING TEST CIRCUIT

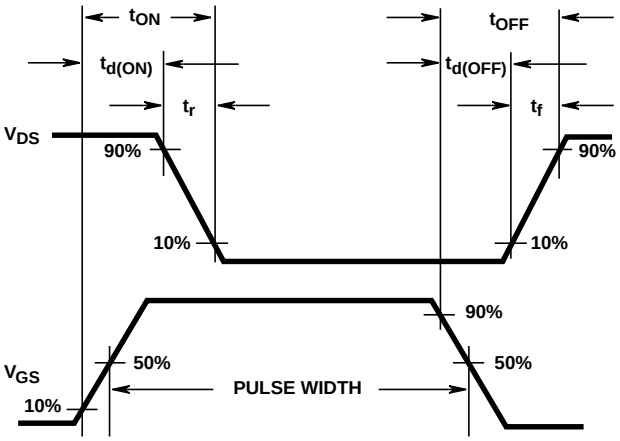


FIGURE 7. RESISTIVE SWITCHING WAVEFORMS

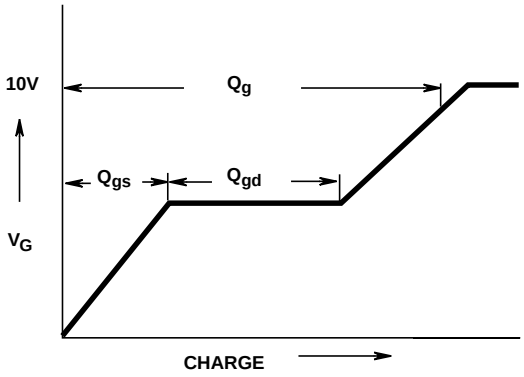


FIGURE 8. BASIC GATE CHARGE WAVEFORM

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANS) $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	±20 (Note 4)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value	±25 (Note 4)	µA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^oC$ at Rated I_D	±20% (Note 5)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1.0mA	±20% (Note 5)	V

NOTES:

4. Or 100% of Initial Reading (whichever is greater).
5. Of Initial Reading.

Screening Information

TEST	JANS
Gate Stress	V_{GS} = 30V, t = 250µs
Pind	Required
Pre Burn-In Tests (Note 6)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25^oC)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, $T_A = 150^oC$, Time = 48 hours
Interim Electrical Tests (Note 6)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, $T_A = 150^oC$, Time = 240 hours
PDA	5%
Final Electrical Tests (Note 6)	MIL-S-19500, Group A, Subgroups 2 and 3

NOTE:

6. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	V_{DS} = 200V, t = 10ms	0.50	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)}$ = 15V, L = 0.1mH	12	A
Thermal Response	ΔV_{SD}	t_H = 10ms; V_H = 25V; I_H = 2A	92	mV
Thermal Impedance	ΔV_{SD}	t_H = 500ms; V_H = 25V; I_H = 1A	190	mV

Rad Hard Data Packages - Intersil Power Transistors

1. JANS Rad Hard - Standard Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

F. Group A - Attributes Data Sheet

G. Group B - Attributes Data Sheet

H. Group C - Attributes Data Sheet

I. Group D - Attributes Data Sheet

2. JANS Rad Hard - Optional Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- X-Ray and X-Ray Report

F. Group A
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups A2, A3, A4, A5 and A7 Data

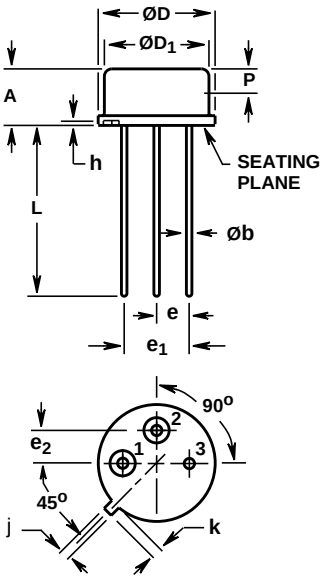
G. Group B
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups B1, B3, B4, B5 and B6 Data

H. Group C
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups C1, C2, C3 and C6 Data

I. Group D
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Pre and Post Radiation Data

TO-205AF

3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Lead no. 3 butt welded to stem base.
7. Controlling dimension: Inch.
8. Revision 3 dated 6-94.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029