Tel:886-2-66296288
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URL:http://www.princeton.com.tw

LCD Driver IC **PT6584**

DESCRIPTION

The PT6584 are 1/4 duty LCD display drivers that can directly drive up to 220 segments and can control up to four general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

FEATURES

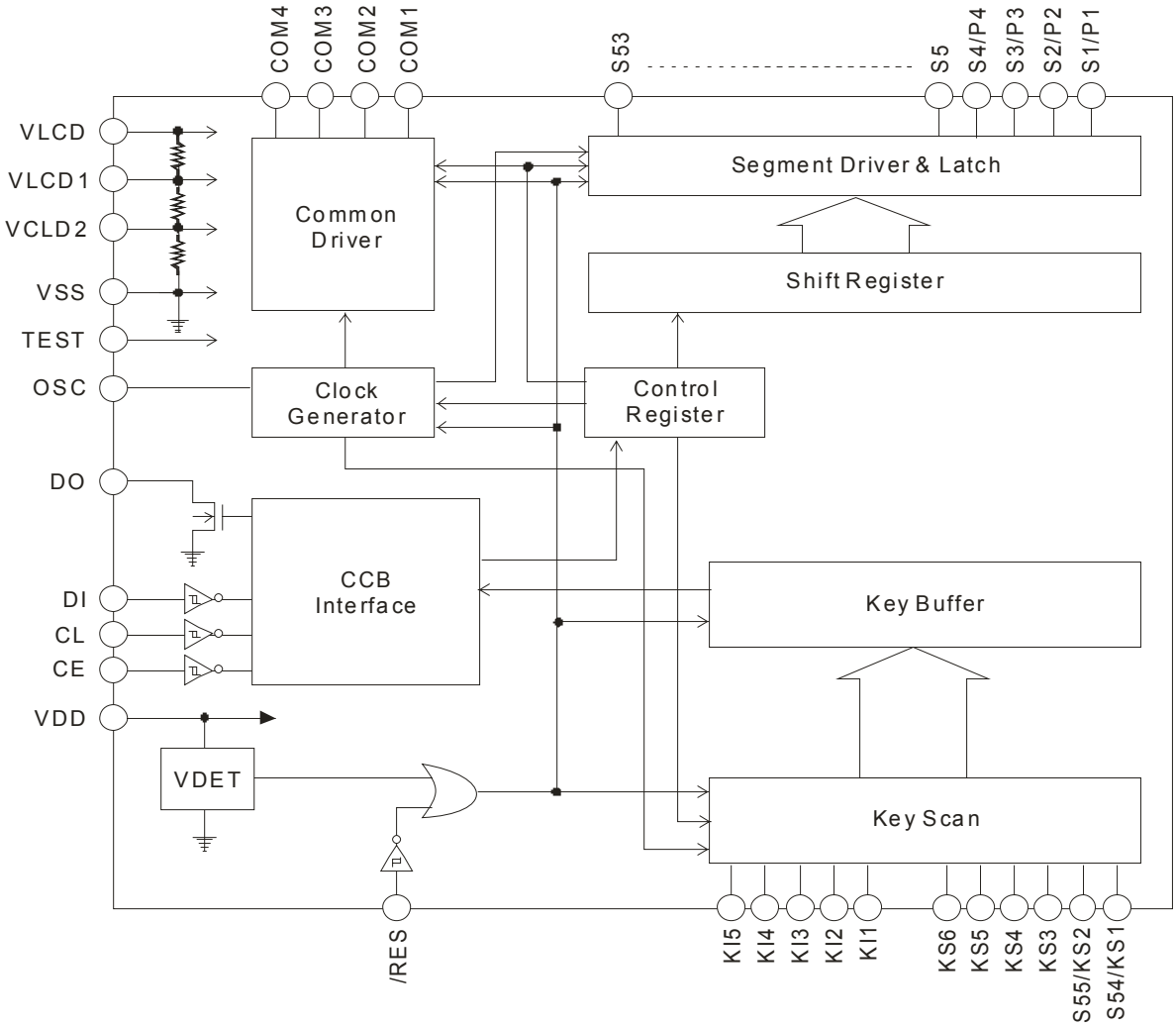
- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/4duty - 1/2bias and 1/4duty
  - 1/3bias drive schemes can be controlled from serial data (up to 220 segments).
- Sleep mode and all segments off functions that are controlled from serial data
- Segment output port/general-purpose output port function switching that is controlled from serial data
- Serial data I/O supports CCB format communication with the system controller
- Direct display of display data without the use of a decoder provides high generality
- Independent VLCD for the LCD driver block (VLCD can be set to in the range VDD-0.5 to 6.0V.)
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays
- RES pin provided for forcibly initializing the IC internal circuits
- RC oscillator circuit

APPLICATION

- Electronic Equipment with LCD Display

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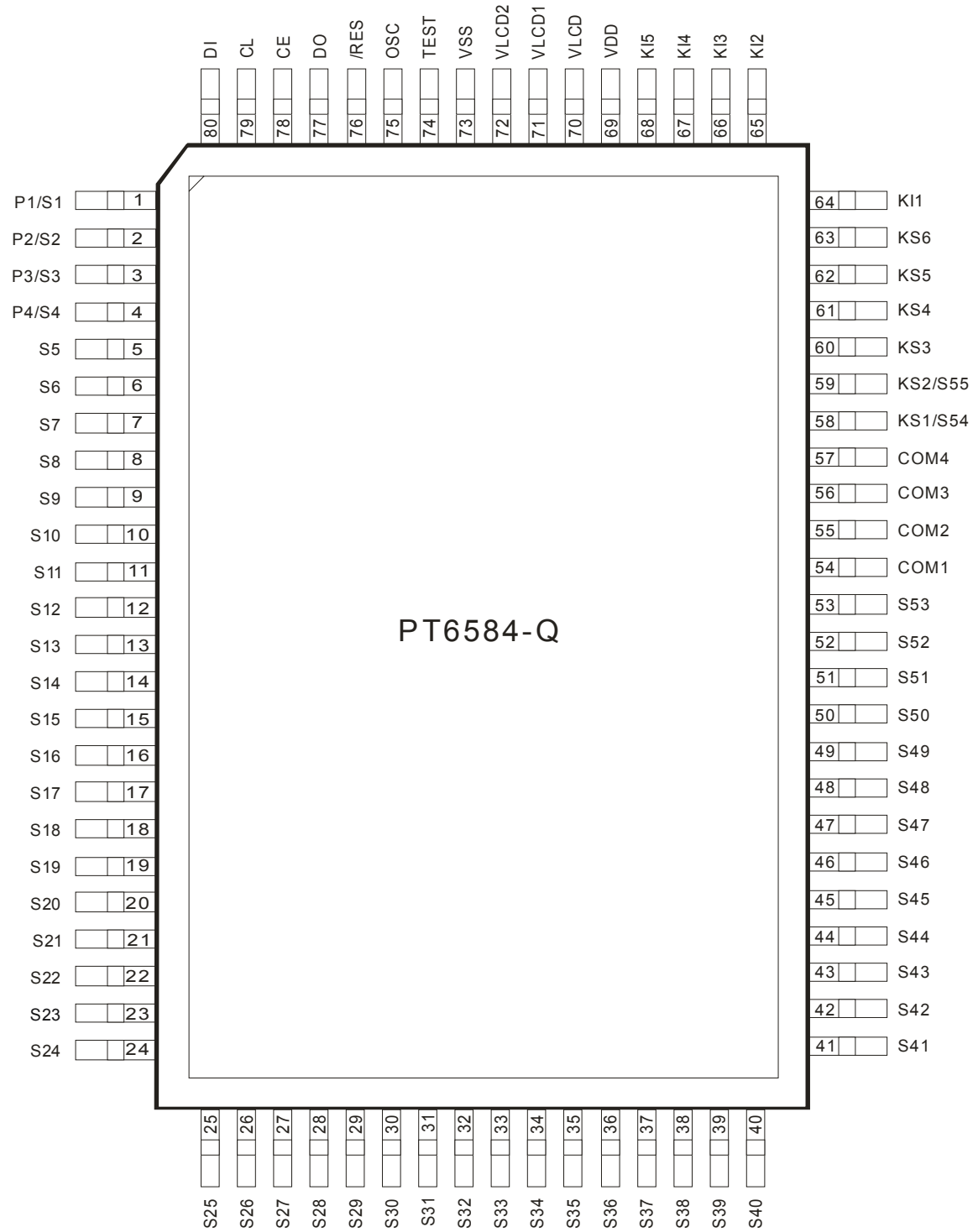
BLOCK DIAGRAM



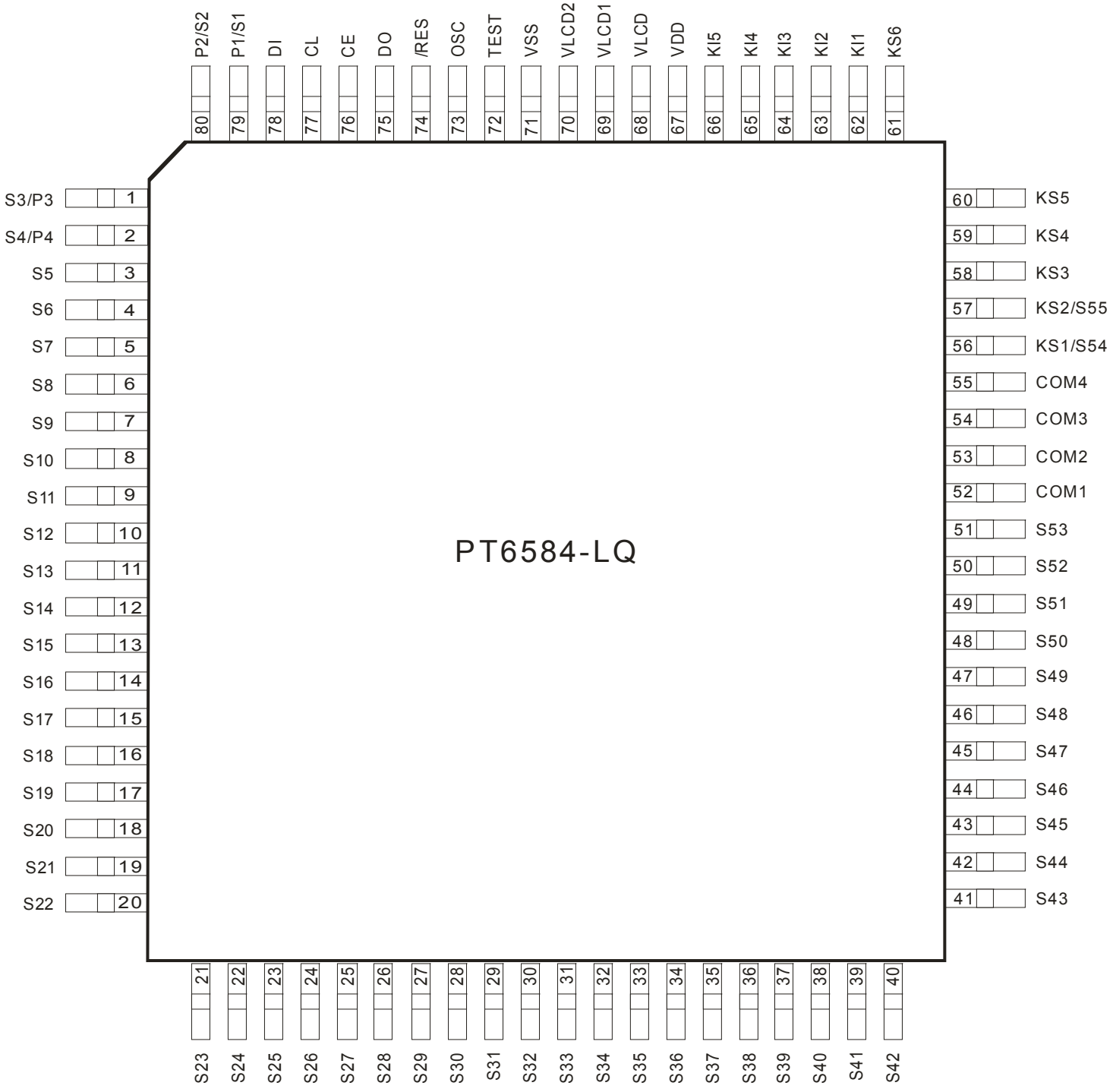
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PIN CONFIGURATION

QFP



LQFP

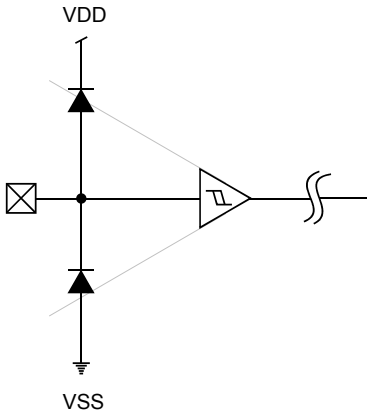

PT6584-LQ
1 S3/P3
2 S4/P4
3 S5
4 S6
5 S7
6 S8
7 S9
8 S10
9 S11
10 S12
11 S13
12 S14
13 S15
14 S16
15 S17
16 S18
17 S19
18 S20
19 S21
20 S22
21 S23
22 S24
23 S25
24 S26
25 S27
26 S28
27 S29
28 S30
29 S31
30 S32
31 S33
32 S34
33 S35
34 S36
35 S37
36 S38
37 S39
38 S40
39 S41
40 S42
41 S43
42 S44
43 S45
44 S46
45 S47
46 S48
47 S49
48 S50
49 S51
50 S52
51 S53
52 COM1
53 COM2
54 COM3
55 COM4
56 KS1/S54
57 KS2/S55
58 KS3
59 KS4
60 KS5
61 KS6
62 KI1
63 KI2
64 KI3
65 KI4
66 KI5
67 VDD
68 VLCD
69 VLCD1
70 VLCD2
71 VSS
72 TEST
73 OSC
74 /RES
75 DO
76 CE
77 CL
78 DI
79 P1/S1
80 P2/S2

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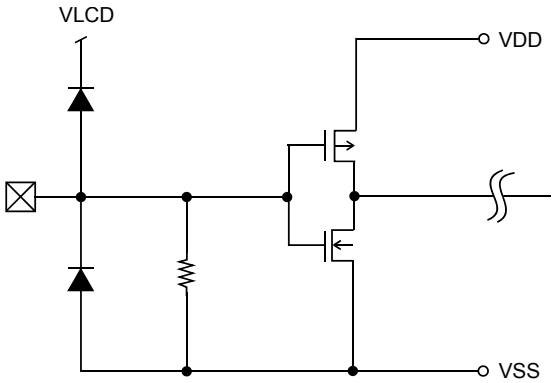
INPUT/OUPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

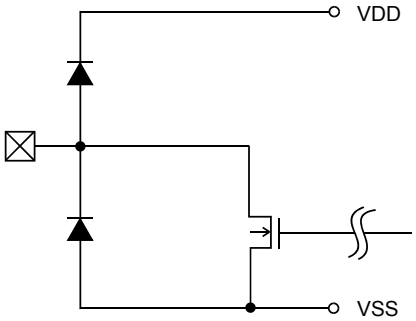
INPUT PIN: CL, CE, DI, TEST



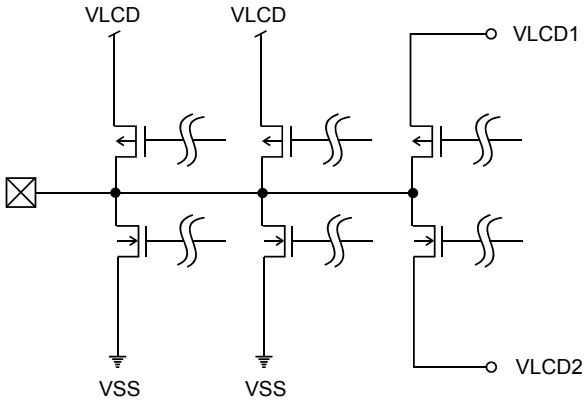
INPUT PIN: KI1 TO KI5



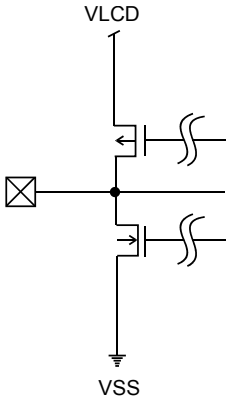
OUTPUT PIN: DO



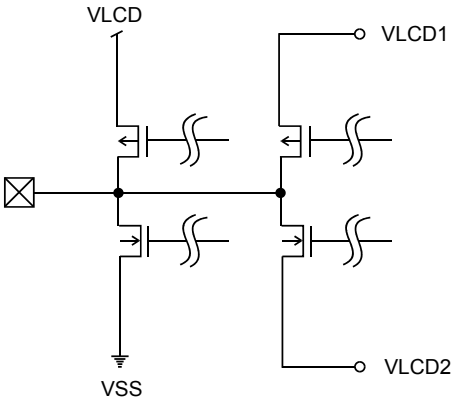
OUTPUT PIN: S1/P1 TO S4/P4, S5 TO S53, KS1/S54, KS2/S55



OUTPUT PIN: KS3 TO KS6



OUTPUT PIN: COM1 TO COM3, COM4



PIN DESCRIPTION

Pin Name	I/O	Active	Handling when unused	Description	Pin No.	
					QFP	LQFP
S1/P1 S2/P2 S3/P3 S4/P4 S4 ~ S53	O	-	OPEN	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	1 2 3 4 5 ~ 53	79 80 1 2 3 ~ 51
COM1 COM2 COM3 COM4/S74	O	-	OPEN	Common driver outputs The frame frequency fo is given by: fo = (fOSC/512)Hz.	54 55 56 57	52 53 54 55
KS1/S54 KS2/S56 KS3 ~ KS6	O	-	OPEN	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S54 and KS2/S55 pins can be used as segment outputs when so specified by the control data.	58 59 60 ~ 63	56 57 58 ~ 61
KI1 ~ KI5	I	H	GND	Key scan inputs These pins have built-in pull-down resistors.	64 ~ 68	62 ~ 66
OSC	I/O	-	VDD	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	75	73
CE	I	H	GND	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	78	76
CL	I	↑			79	77
DI	I	-			80	78
DO	O	-	OPEN		77	75
/RES	I	L	VDD	Reset signal input /RES=low ---- Display off Key scan disabled All key data is reset to low /RES=high --- Display on Key scan enabled However, serial data can be transferred when /RES is low.	76	74
TEST	I	-	-	This pin must be connected to ground	74	72
VLCD1	I	-	OPEN	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to VLCD2 when a 1/2 bias drive scheme is used.	71	69
VLCD2	I	-	OPEN	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to VLCD1 when a 1/2 bias drive scheme is used.	72	70
VDD	-	-	-	Logic block power supply connection. Provide a voltage of between 3.3 and 6.0V.	69	67
VLCD	-	-	-	LCD driver block power supply connection. Provide a voltage of between VDD-0.5 and 6.0V.	70	68
VSS	-	-	-	Power supply connection. Connect to ground.	73	71

FUNCTION DESCRIPTION

SERIAL DATA INPUT

When CL is stopped at the low level.

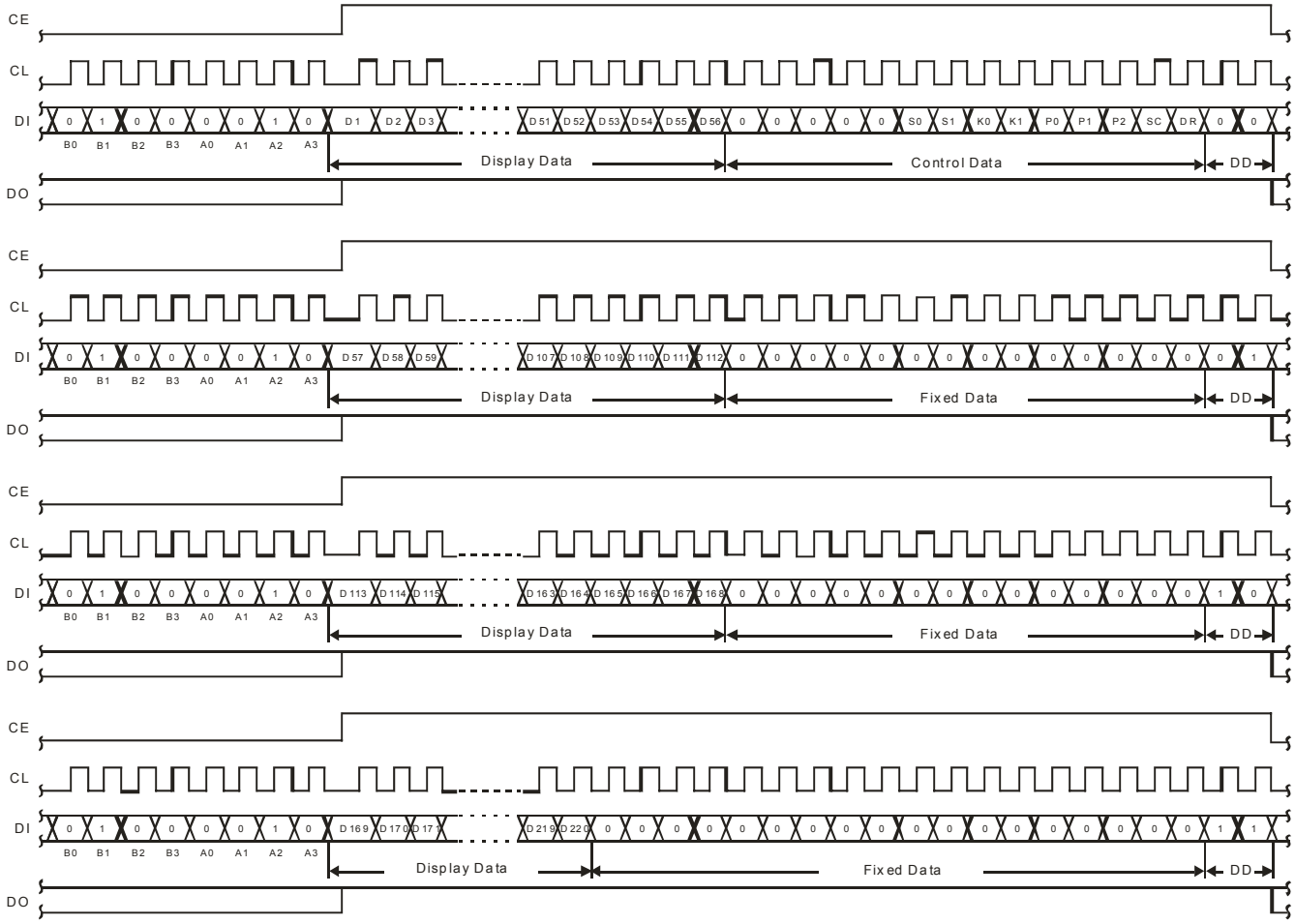


Figure 1

Notes:
1. B0 to B3, A0 to A3=CCB address.
2. D=Direction Data.

When CL is stopped at the high level.

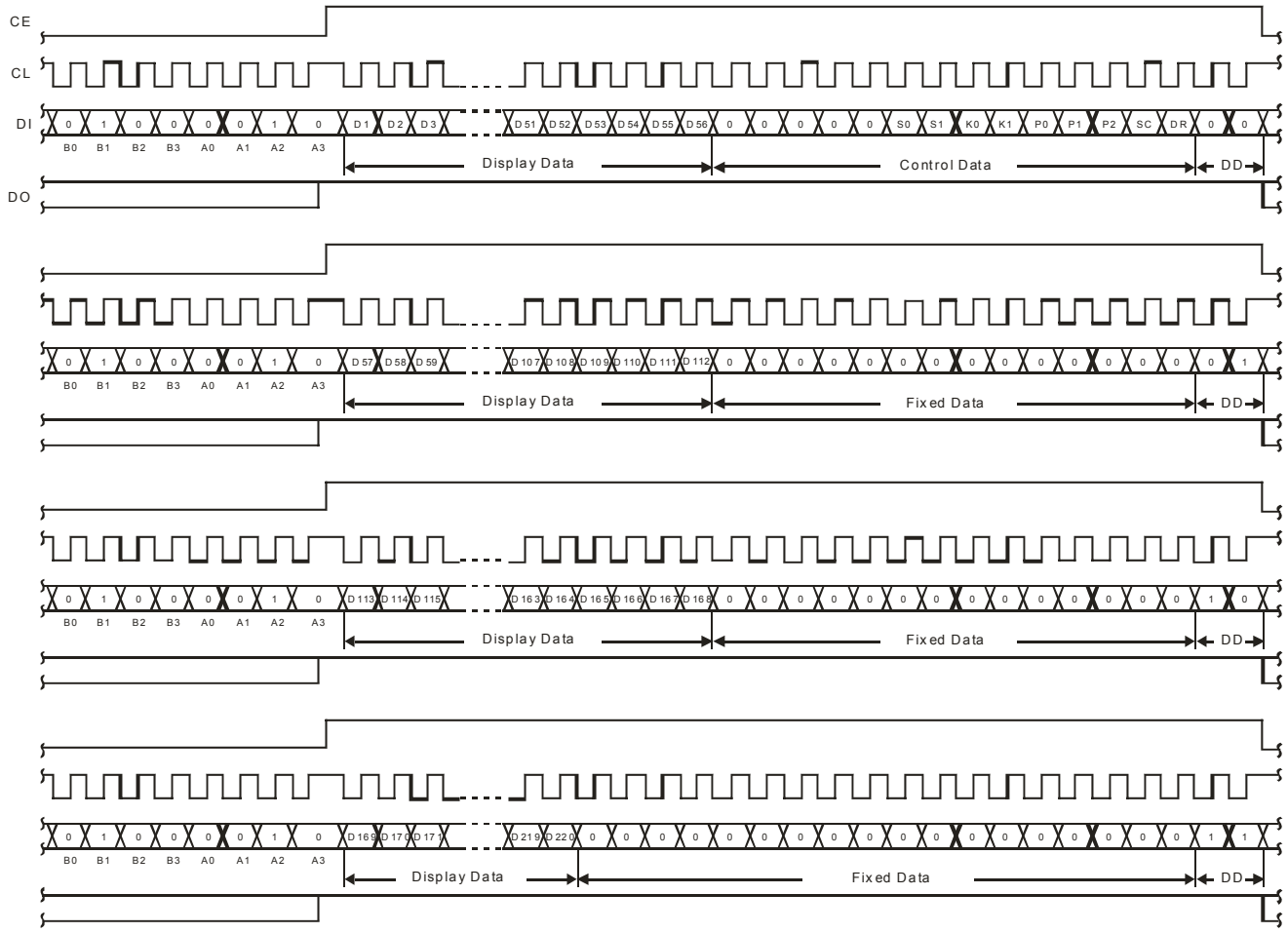


Figure 2

Notes:
1. B0 to B3, A0 to A3=CCB address.
2. DD=Direction Date.

CCB address	: 42H
D1 to D220	: Display data
S0, S1	: Sleep control data
K0, K1	: Key scan output/segment output selection data
P0 to P2	: Segment output port/general-purpose output port selection data
SC	: Segment on/off control data
DR	: 1/2 bias or 1/3 bias drive selection data

CONTROL DATA

S0, S1: SLEEP CONTROL DATA

These control data bits switch between normal mode and sleep mode and set the states of the KS1 to KS6 key scan outputs during key scan standby.

Control Data		Mode	OSC Oscillator	Segment Outputs Common Outputs	Output Pin States During Key Scan Standby					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Oscillator operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This assumes that the KS1/S54 and KS2/S55 output pins are selected for key scan output.

K0, K1: KEY SCAN OUTPUT/SEGMENT OUTPUT SELECTION DATA

These control data bits switch the functions of the KS1/S54 and KS2/S55 output pins between key scan output and segment output.

Control Data		Output Pin State		Maximum Number of Input Keys
K0	K1	KS1/S54	KS2/S55	
0	0	KS1	KS2	30
0	1	S54	KS2	25
1	X	S54	S55	20

Notes:
1. X=Don't care
2. KSn (n=1 or 2): Key scan output
3. Sn (n=54 or 55): Segment output

P0 TO P2: SEGMENT OUTPUT PORT/GENERAL-PURPOSE OUTPUT PORT SELECTION DATA

These control data bits switch the functions of the S1/P1 to S4/P4 output pins between the segment output port and the general-purpose output port.

Control Data			Output Pin State			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Notes:
1. Sn (n=1 to 4): Segment output port
2. Pn (n=1 to 4): General-purpose output port

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

Output Pin	Corresponding Display Data
S1/P1	D1
S2/P2	D5
S3/P3	D9
S4/P4	D13

For example, if the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level (V_{LCD}) when the display data D13 is 1, and will output a low level (Vss) when D13 is 0.

SC: SEGMENT ON/OFF CONTROL DATA

This control data bit controls the on/off state of the segments.

SC	Display State
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

DR: 1/2 BIAS OR 1/3 BIAS DRIVE SELECTION DATA

This control data bit switches between LCD 1/2 bias or 1/3 bias drive.

DR	Bias Drive Scheme
0	1/3 bias drive
1	1/2 bias drive

DISPLAY DATA AND OUTPUT PIN CORRESPONDENCE

Output Pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112

Output Pin	COM1	COM2	COM3	COM4
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
KS1/S54	D213	D214	D215	D216
KS2/S55	D217	D218	D219	D220

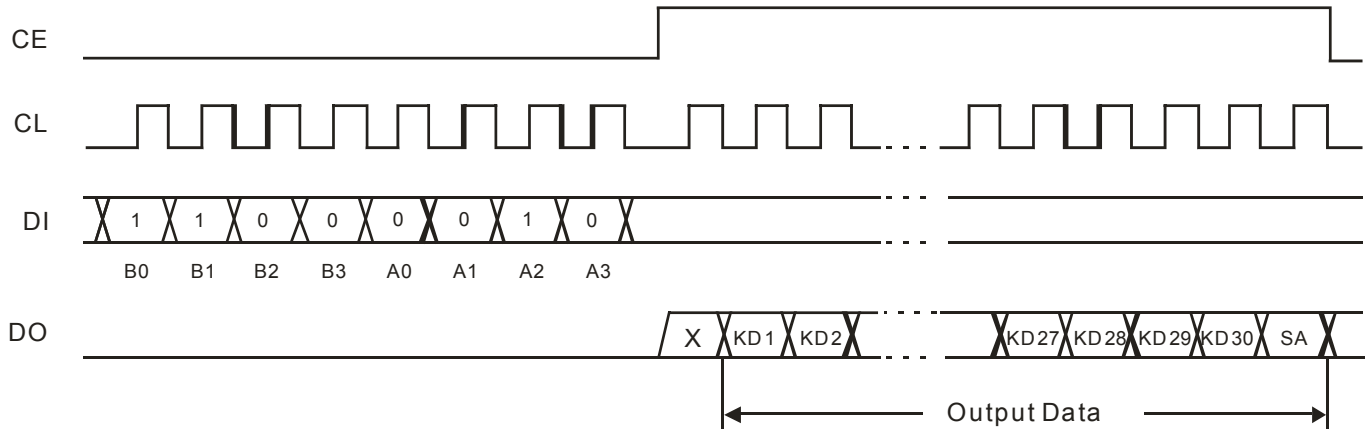
Note:
This is for the case where the output pins S1/P1 to S4/P4, KS1/S54 and KS2/S55 are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

Display Data				Output Pin State (S11)
D41	D42	D43	D44	
0	0	0	0	The LCD segment for COM1, COM2, COM3 and COM4 are off.
0	0	0	1	The LCD segment for COM4 is on.
0	0	1	0	The LCD segment for COM3 is on.
0	0	1	1	The LCD segments for COM3 and COM4 are on.
0	1	0	0	The LCD segment for COM2 is on.
0	1	0	1	The LCD segments for COM2 and COM4 are on.
0	1	1	0	The LCD segments for COM2 and COM3 are on.
0	1	1	1	The LCD segments for COM2, COM3 and COM4 are on.
1	0	0	0	The LCD segment for COM1 is on.
1	0	0	1	The LCD segments for COM1 and COM4 are on.
1	0	1	0	The LCD segments for COM1 and COM3 are on.
1	0	1	1	The LCD segments for COM1, COM3 and COM4 are on.
1	1	0	0	The LCD segments for COM1 and COM2 are on.
1	1	0	1	The LCD segments for COM1, COM2 and COM4 are on.
1	1	1	0	The LCD segments for COM1, COM2 and COM3 are on.
1	1	1	1	The LCD segments for COM1, COM2, COM3 and COM4 are on.

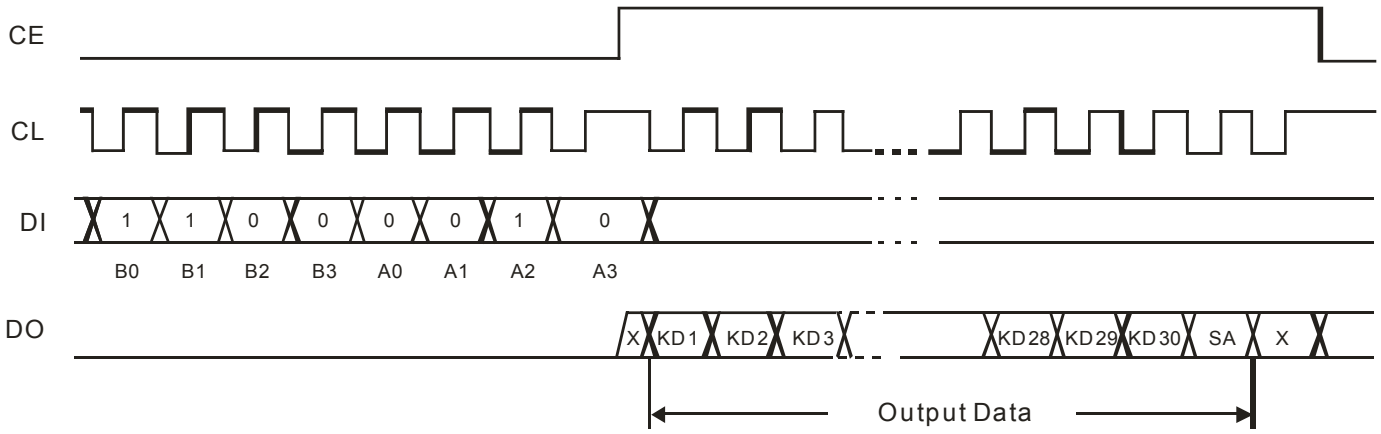
SERIAL DATA OUTPUT

When CL is stopped at the low level.



Notes:
1. X=Don't care
2. B0 to B3, A0 to A3: CCB address

When CL is stopped at the high level.



Notes:
1. X=Don't care
2. B0 to B3, A0 to A3: CCB address
3. CCD address: 43H
4. KD1 to KD30: Key data
5. SA: Sleep acknowledge data
6. If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

OUTPUT DATA

KD1 TO KD30: KEY DATA

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

Item	KI1	KI2	KI3	KI4	KI5
KS1/S54	KD1	KD2	KD3	KD4	KD5
KS2/S55	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

When the KS1/S54 and KS2/S55 output pins are selected to be segment outputs by control data bits K0 and K1 and a key matrix of up to 20 keys is formed using the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

SA: SLEEP ACKNOWLEDGE DATA

This output data is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in the sleep mode and 0 in the normal mode.

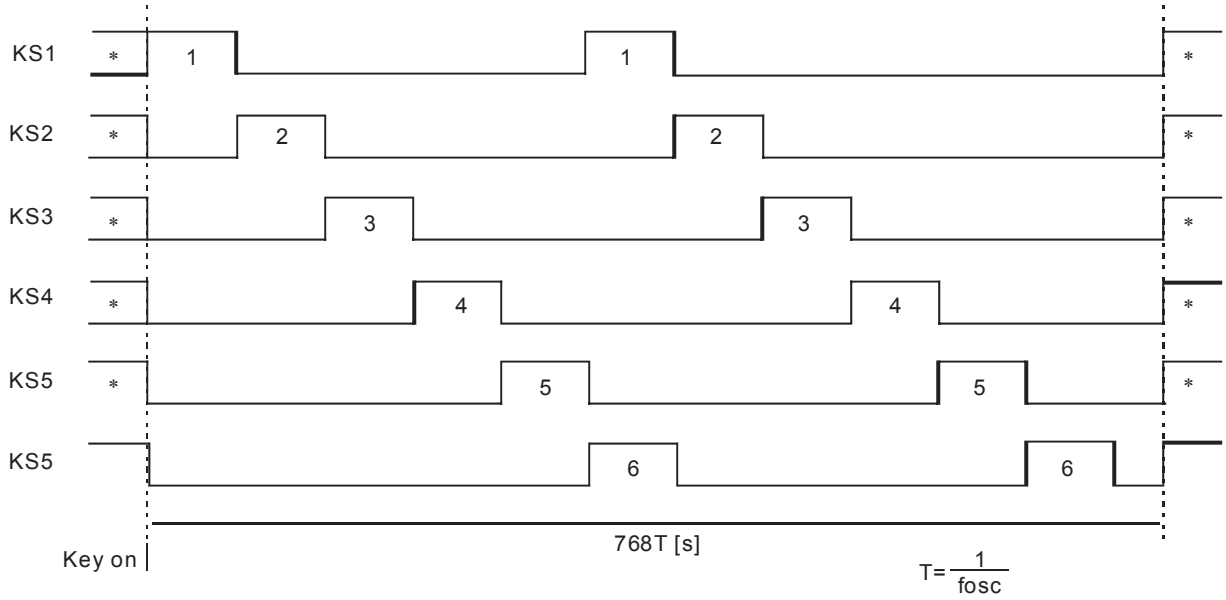
SLEEP MODE

Sleep mode is set up by setting S0 or S1 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with both S0 and S1 set to 0. However, note that the S1/P1 to S4/P4 outputs can be used as general -purpose output ports according to the state of the P0 to P2 control data bits, even in sleep mode. (See the control data description for details.)

KEY SCAN OPERATION FUNCTIONS

KEY SCAN TIMING

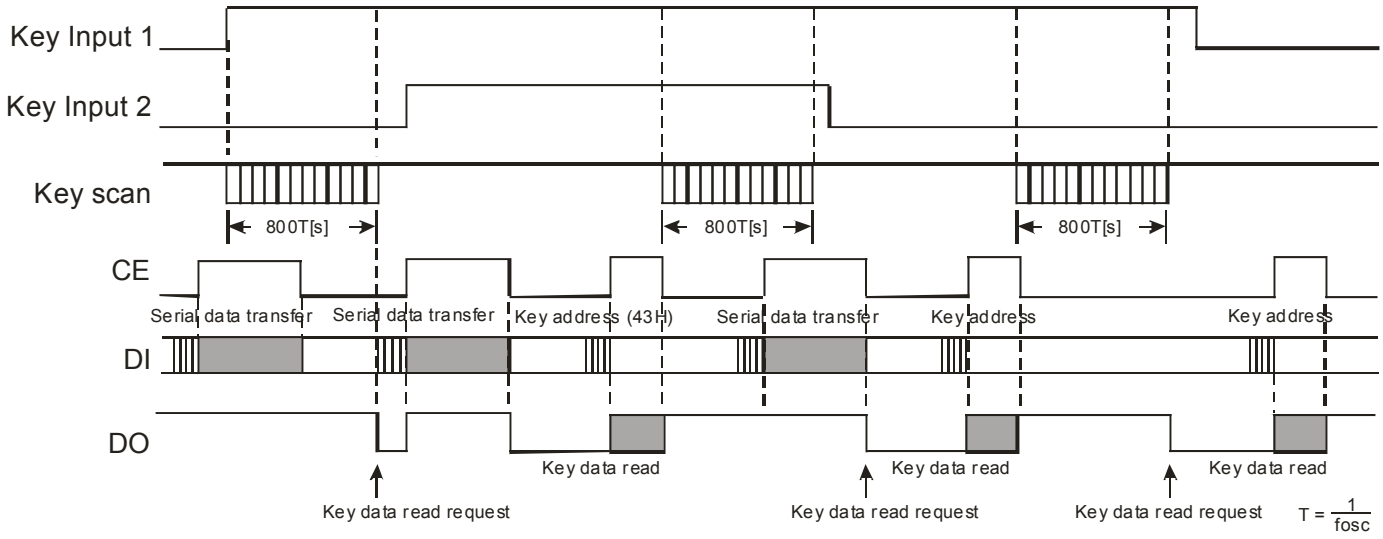
The key scan period is 384T(s). To reliably determine the on/off state of the keys, the PT6584 scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the PT6584 cannot detect a key press shorter than 800T(s).



Note:
*: In sleep mode the high/low state of these pins is determined by the S0 and S1 bits in the control data. Key scan output signals are not output from pins that are set low.

IN NORMAL MODE

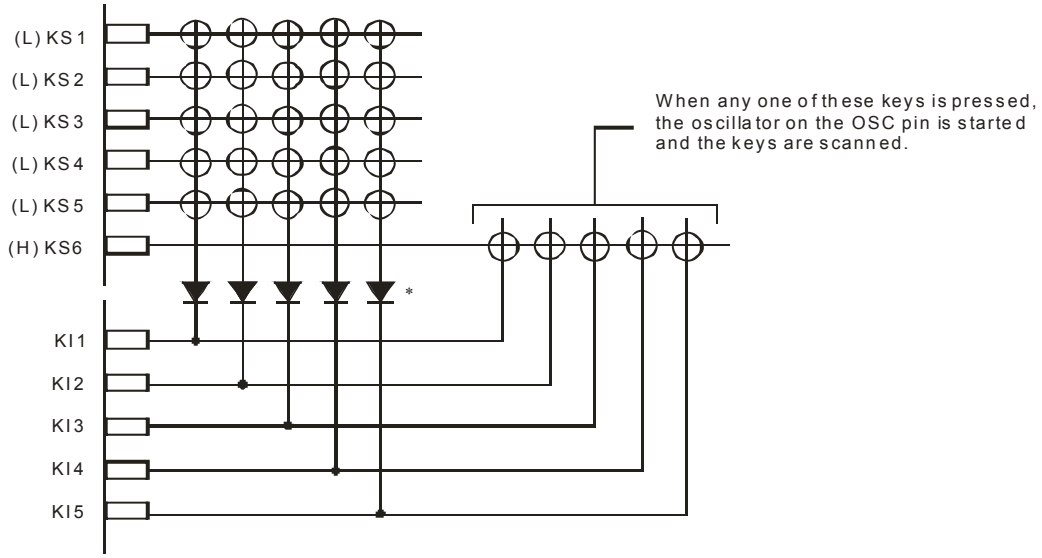
- The pins KS1 to KS6 are set high.
- When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 800T(s) (Where $T=\frac{1}{fosc}$) the PT6584 outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the PT6584 performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10KΩ).



IN SLEEP MODE

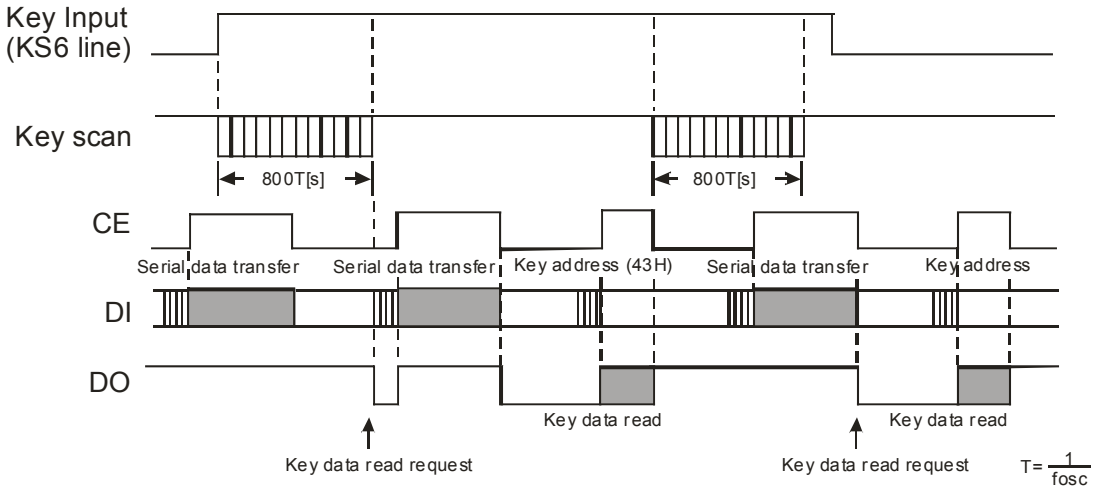
- The pins KS1 to KS6 are set to high or low by the S0 and S1 bits in the control data. (See the control data description for details.)
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 800T(s)(Where T= $\frac{1}{fosc}$) the PT6584 outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the PT6584 performs another key scan. However, this does not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10KΩ).
- Sleep mode key scan example

Example: S0=0, S1=1 (sleep with only KS6 high)



Note:

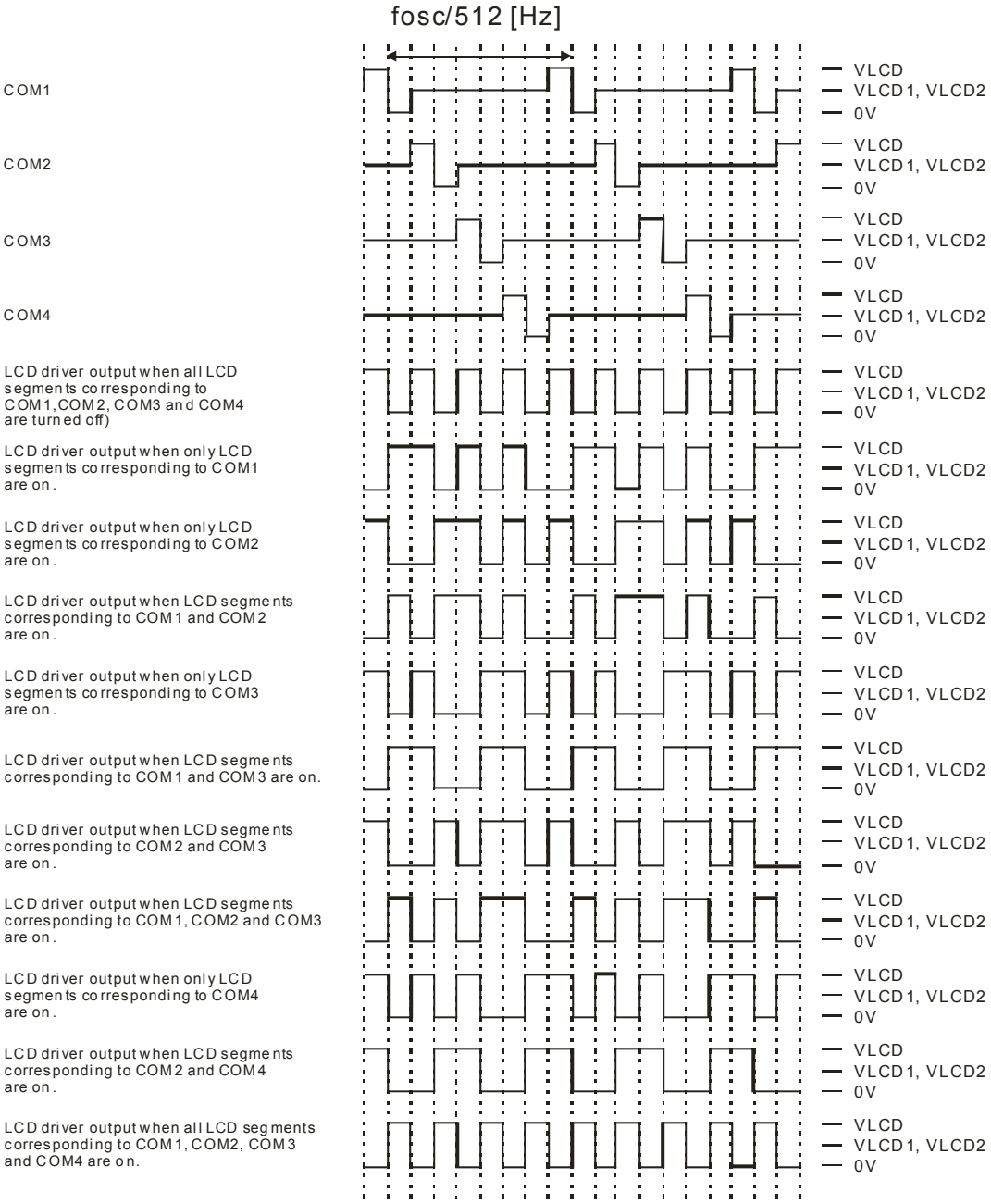
*: These diodes are required to reliable recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



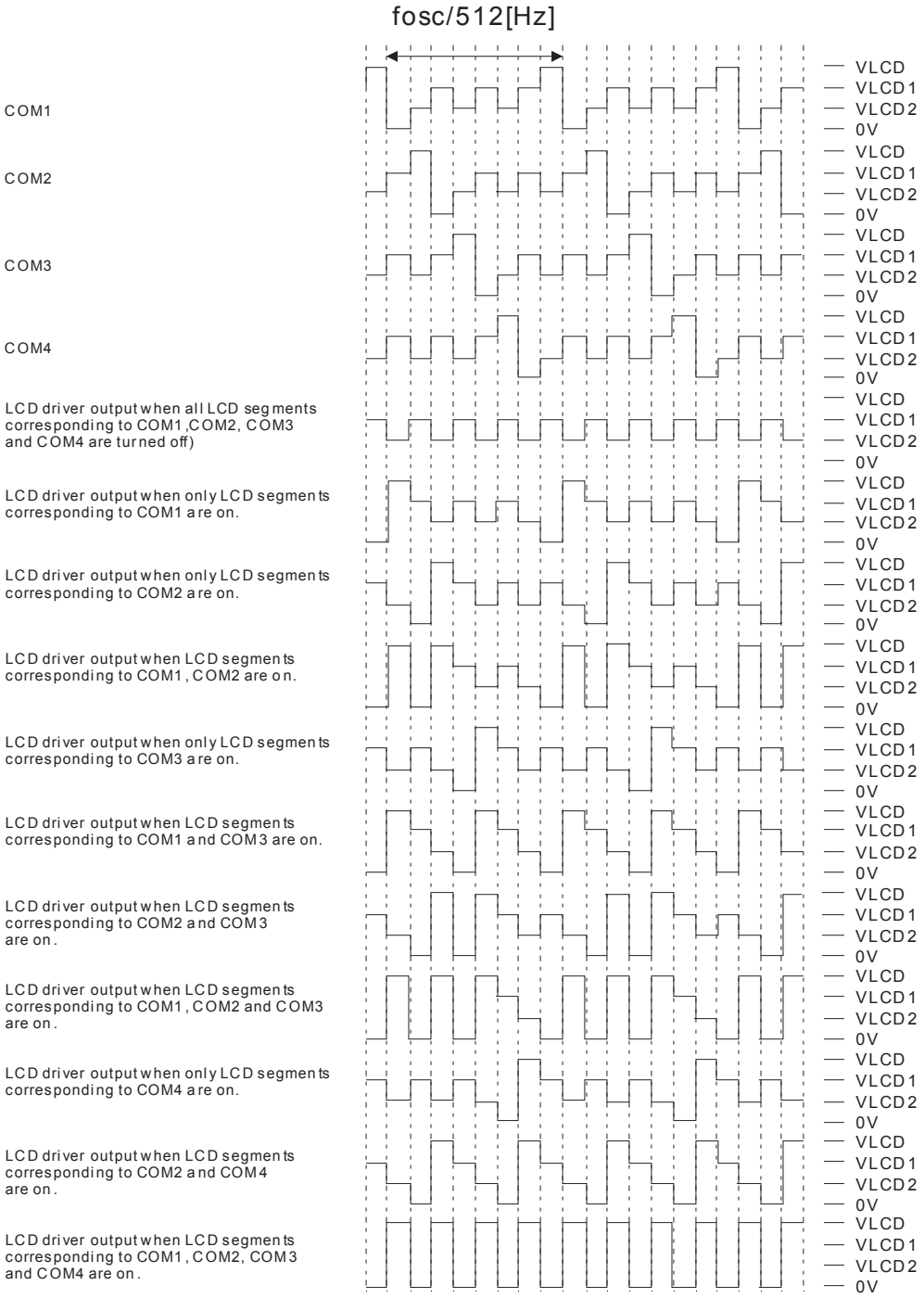
MULTIPLE KEY PRESSES

Although the PT6584 is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/4 DUTY, 1/2 BIAS DRIVE TECHNIQUE



1/4 DUTY, 1/3 BIAS DRIVE TECHNIQUE



VOLTAGE DETECTION TYPE RESET CIRCUIT (VDET)

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage VDET, which is 3.0V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage VDD rise time when the logic block power is first applied and the logic block power supply voltage VDD fall time when the voltage drops are both at least 1ms. (see Figure 3)

POWER SUPPLY SEQUENCE

The following sequences must be observed when power is turned on and off. (see Figure 3 and 4.)

- Power on: Logic block power supply(V_{DD}) on → LCD driver block power supply(V_{LCD}) on.
- Power off: LCD driver block power supply(V_{LCD}) off → Logic block power supply(V_{DD}) off.

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

SYSTEM RESET

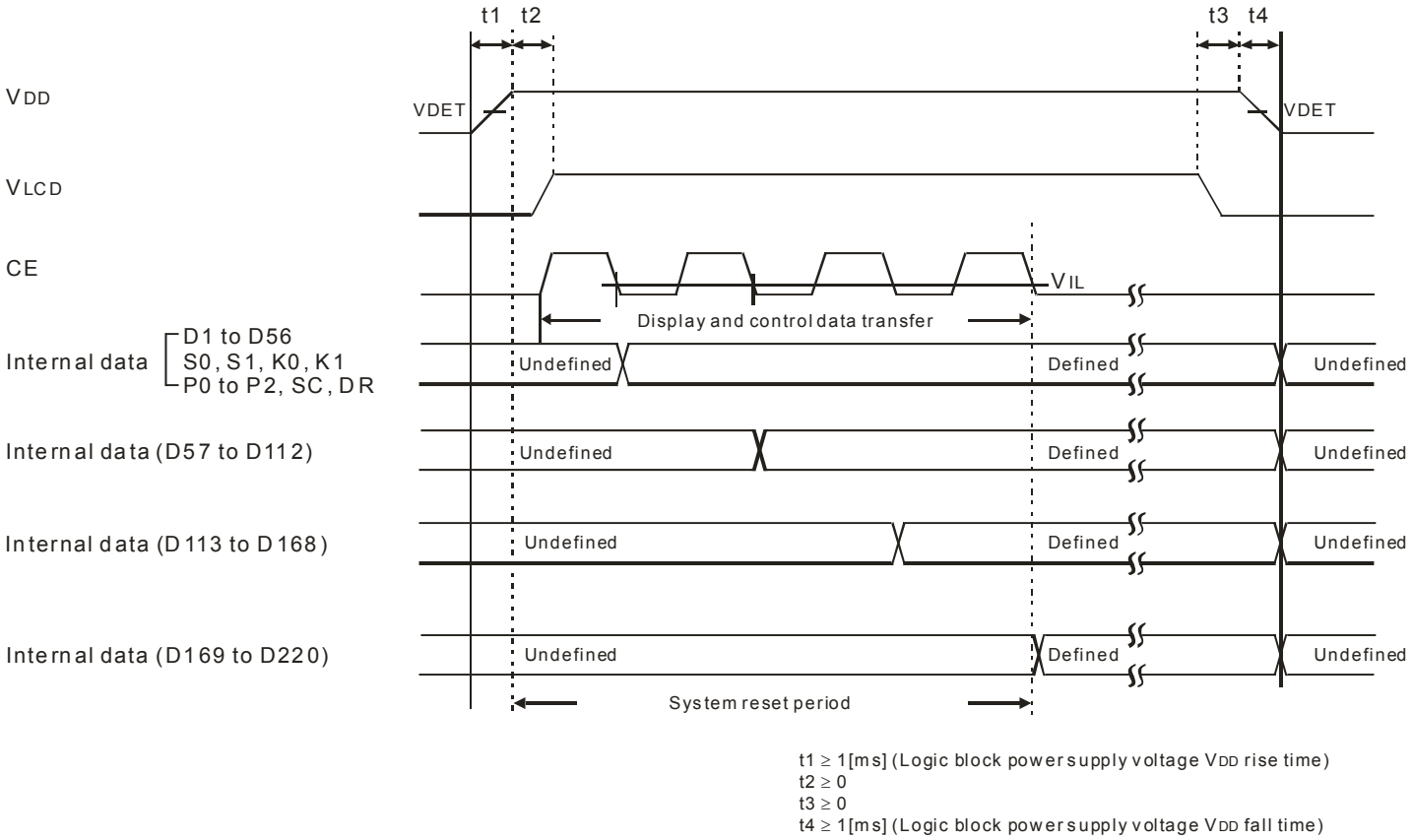
The PT6584 supports the reset methods described below. When a system reset is applied, display is turned off, key scanning is stopped, and all the key data is reset to low. When the reset is cleared, display is turned on and key scanning become possible.

RESET METHODS

(1) Reset at power-on and power-down

If at least 1ms is assured as the logic block supply voltage VDD rise time when logic block power is applied, a system reset will be applied by the VDET output signal when the logic block supply voltage is brought up. If at least 1 ms is assured as the logic block supply voltage VDD fall time when logic block power drops, a system reset will be applied in the same manner by the VDET output signal when the supply voltage is lowered. Note that the reset is cleared at the point when all the serial data (the display data D1 to D220 and the control data) has been transferred, i.e., on the fall of the CE signal on the transfer of the last direction data, after all the direction data has been transferred. However, the above operations will be performed regardless of the state (high or low) of the /RES pin. If RES is high, the reset will be cleared at the point the above operations are completed. On the other hand, if /RES is low, the system will remain in the reset period as long as /RES is not set high, even if the above operations are completed. (See Figure 3)

(2) Reset when the logic block power supply voltage is in the allowable operating range (VDD=3.3 to 6.0V). The system is reset when the /RES pin is set low, and the reset is cleared by setting /RES pin high.

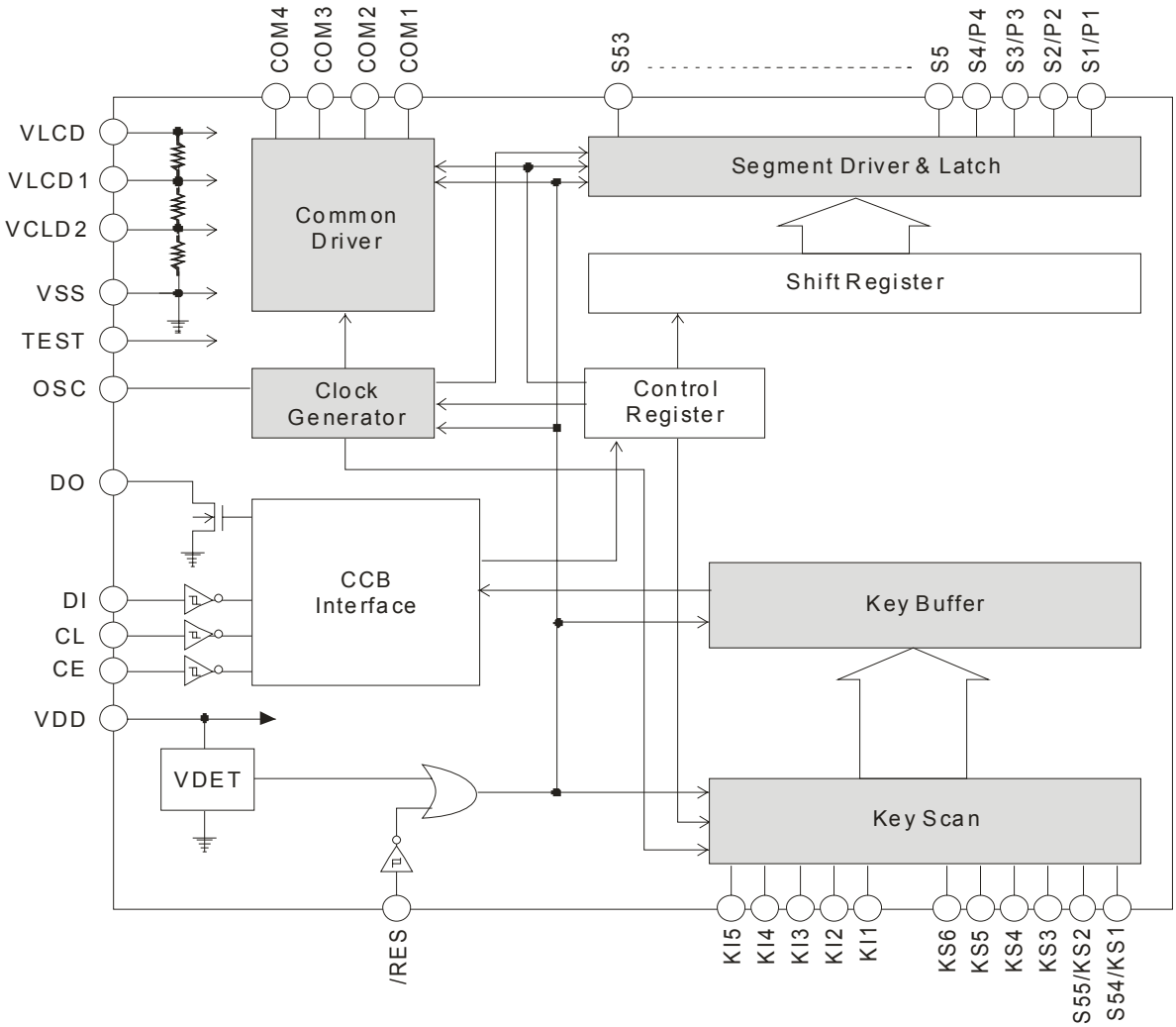


t1 ≥ 1[ms] (Logic block power supply voltage V_{DD} rise time)
t2 ≥ 0
t3 ≥ 0
t4 ≥ 1[ms] (Logic block power supply voltage V_{DD} fall time)

Figure 3

PT6584 INTERNAL BLOCK STATES DURING THE RESET PERIOD

- CLOCK GENERATOR
  Reset is applied and the base clock is stopped. However, the OSC pin state (normal or sleep mode) is determined after the S0 and S1 control data bits are transferred.
- COMMON DRIVER, SEGMENT DRIVER & LATCH
  Reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.
- KEY SCAN
  Reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.
- KEY BUFFER
  Reset is applied and all the key data is set to low.
- CCB INTERFACE, CONTROL REGISTER, SHIFT REGISTER
  Since serial data transfer is possible, these circuits are not reset.



Block that are reset

OUTPUT PIN STATES DURING THE RESET PERIOD

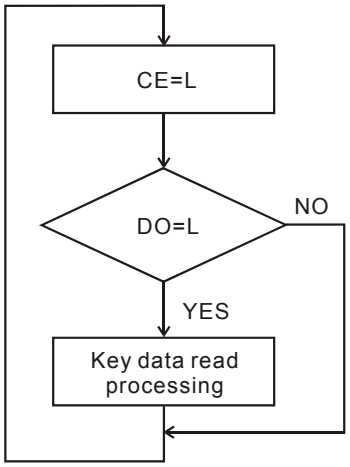
Output Pin	State during Reset
S1/P1 to S4/P4	L (Note 2)
S5 to S53	L
COM1 to COM4	L
KS1/S54. KS2/S55	L (Note 2)
KS3 to KS5	X (Note 3)
KS6	H
DO	H (Note 4)

Notes:
1. X=Don't care
2. These output pins are forcibly set to the segment output function and held low.
3. When power is first applied, these output pins are undefined until the S0 and S1 control data bits have been transferred.
4. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10KΩ is required. This pin remains high during the reset period even if a key data read operation is performed.

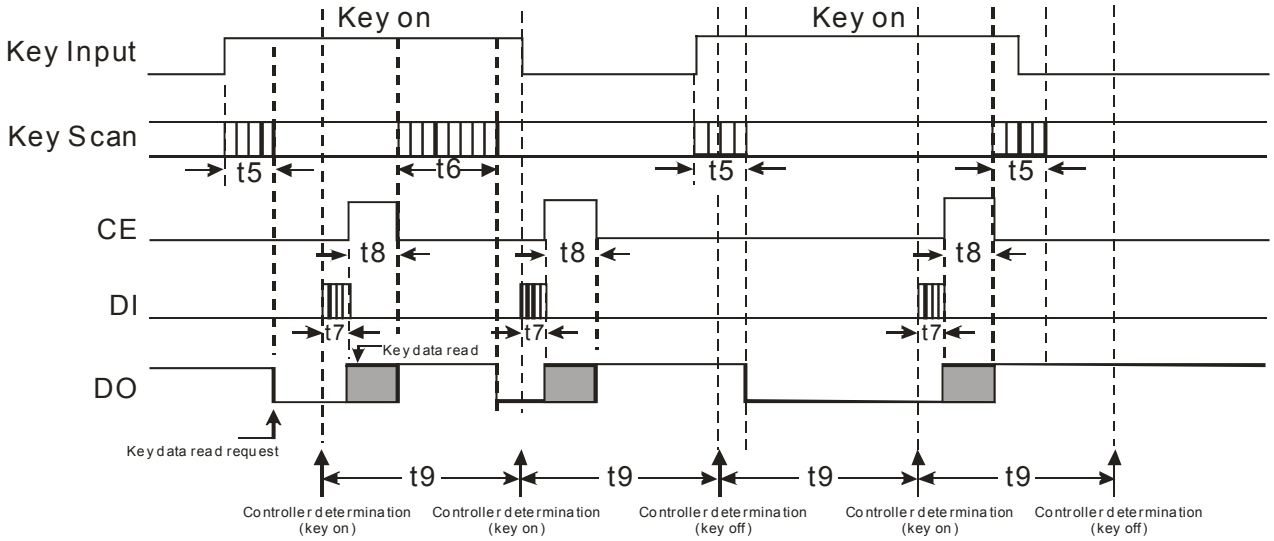
NOTE ON THE CONTROLLER KEY DATA READ TECHNIQUES

TIMER BASED KEY DATA ACQUISITION

- Flowchart



- Timing Chart



t5 : Key scan execution time when the key data agreed for two key scans. (800T(s))

t6 : Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1600T(s))

t7 : Key address (43H) transfer time $T = \frac{1}{fosc}$

t8 : Key data read time

- Explanation

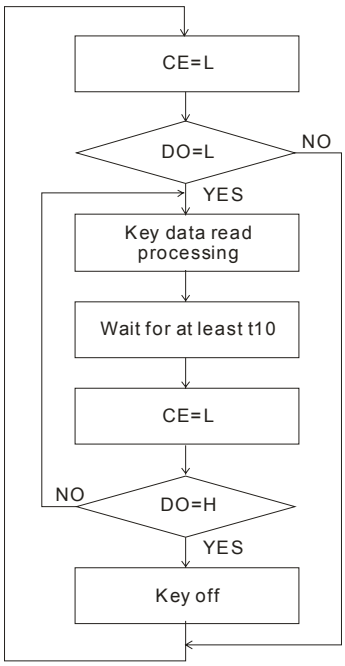
In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.
The period t9 in this technique must satisfy the following condition.

t9>t6+t7+t8

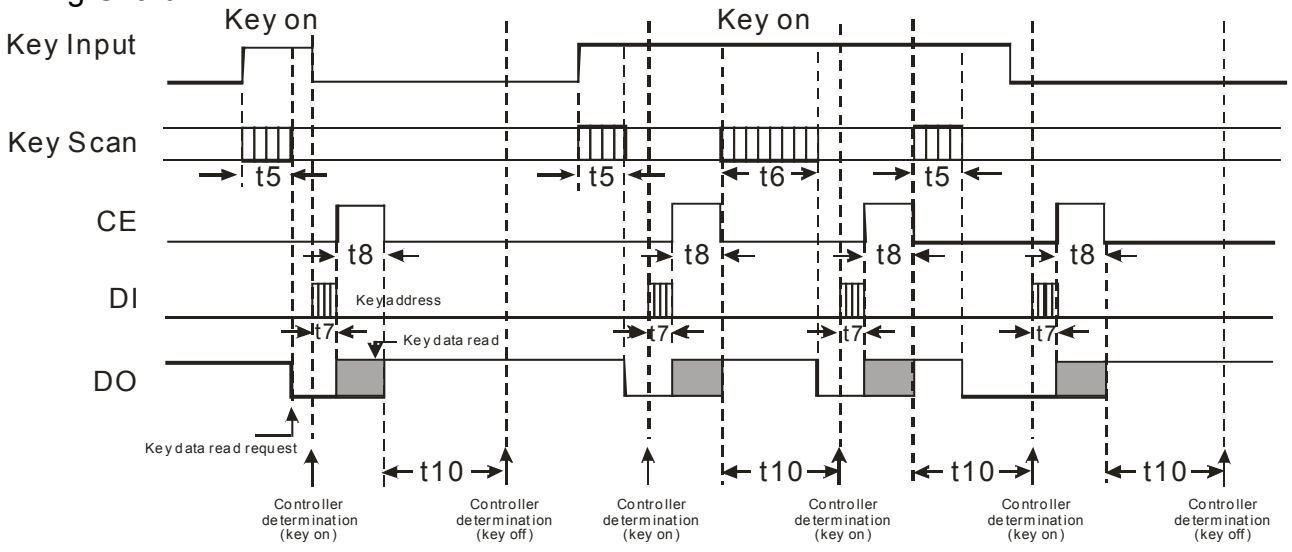
If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

INTERRUPT BASED KEY DATA ACQUISITION

- FLOWCHART



- Timing Chart



t5 : Key scan execution time when the key data agreed for two key scans. (800T(s))

t6 : Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1600T(s))

t7 : Key address (43H) transfer time $T = \frac{1}{fosc}$

t8 : Key data read time

- Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t10 has elapsed by checking the DO state when CE is low and reading the key data. The period t10 in this technique must satisfy the following condition.

t10 > t6

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

NOTE ON TRANSFERRING DISPLAY DATA FROM THE CONTROLLER

The display data (D1 to D220) is transferred to the PT6584 in four operations. All of the display data should be transferred within 30ms to maintain the quality of the displayed image.

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ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25℃)

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 ~ +7.0	V
	V_{LCD} max	V_{LCD}	-0.3 ~ +7.0	
Input voltage	V_{IN1}	CE, CL, DI, /RES	-0.3 ~ V_{DD}+0.3	V
	V_{IN2}	OSC, TEST	-0.3 ~ V_{DD}+0.3	
	V_{IN3}	V_{LCD1}, V_{LCD2}, KI1 to KI5	-0.3 ~ V_{LCD}+0.3	
Output voltage	V_{OUT1}	DO	-0.3 ~ V_{DD}+0.3	V
	V_{OUT2}	OSC	-0.3 ~ V_{DD}+0.3	
	V_{OUT3}	S1 to S55, COM1 to COM4, KS1 to KS6, P1 to P4	-0.3 ~ V_{LCD}+0.3	
Output current	I_{OUT1}	S1 to S55	300	μA
	I_{OUT2}	COM1 to COM4	3	mA
	I_{OUT3}	KS1 to KS6	1	
	I_{OUT4}	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85℃	200	mW
Operating temperature	Topr	-	-40 ~ +85	℃
Storage temperature	Tstg	-	-65 ~ +150	℃

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ALLOWABLE OPERATING RANGES

(Ta=-40 to +85℃, V_{SS}=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}	V_{DD}	3.3	-	6.0	V
	V_{LCD}	V_{LCD}	V_{DD}-0.5	-	6.0	V
Input voltage	V_{LCD1}	V_{LCD1}	-	2/3V_{LCD}	V_{LCD}	V
	V_{LCD2}	V_{LCD2}	-	1/3V_{LCD}	V_{LCD}	V
Input high level voltage	V_{IH1}	CE, CL, DI, /RES	0.8 V_{DD}	-	6.0	V
	V_{IH2}	KI1 to KI5	0.6 V_{DD}	-	V_{LCD}	V
Input low level voltage	V_{IL}	CE, CL, DI, /RES, KI1 to KI5	0	-	0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC	-	43	-	KΩ
Recommended external capacitance	C_{OSC}	OSC	-	680	-	pF
Guaranteed oscillator range	fosc	OSC	25	50	100	MHz
Data setup time	t_{ds}	CL,DI: Figure 4	160	-	-	ns
Data hold time	t_{dh}	CL, DI: Figure 4	160	-	-	ns
CE wait time	t_{cp}	CE, CL: Figure 4	160	-	-	ns
CE setup time	t_{cs}	CE, CL: Figure 4	160	-	-	ns
CE hold time	t_{ch}	CE, CL: Figure 4	160	-	-	ns
High level clock pulse width	$t_{\varnothing H}$	CL: Figure 4	160	-	-	ns
Low level clock pulse width	$t_{\varnothing L}$	CL: Figure 4	160	-	-	ns
Rise time	tr	CE, CL, DI: Figure 4	-	160	-	ns
Fall time	tf	CE, CL, DI: Figure 4	-	160	-	ns
DO output delay time	t_{dc}	DO, R_{PU}=4.7KΩ, C_L=10pf (see note): Figure 4	-	-	1.5	μs
DO rise time	t_{dr}	DO, R_{PU}=4.7KΩ, C_L=10pf (see note): Figure 4	-	-	1.5	μs

Note:
Since DO is an open-drain output, these values depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.

ELECTRICAL CHARACTERISTICS

(Ta=-40 to +85℃, V_{SS}=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Hysteresis	V_H	CE, CL, DI, /RES, KI1 to KI5	-	0.1VDD	-	V
Power-down Detection Voltage	V_{DET}		1.8	2.4	3.2	V
Input High level Current	I_{IH}	CE, CL, DI, /RES: V_I=6.0V	-	-	5.0	μA
Input Low Level Current	I_{IL}	CE, CL, DI, /RES: V_I=0V	-5.0	-	-	μA
Input Floating Voltage	V_{IF}	KI1 to KI5	-	-	$0.05V_{DD}$	V
Pull-down Resistance	R_{PD}	KI1 to KI5: V_{DD}=5.0V	50	100	250	KΩ
Output Off Leakage Current	I_{OFFH}	DO: VO=6.0V	-	-	6.0	μA
Output High Level Voltage	V_{OH1}	KS1 to KS6: I_O=-500μA	V_{LCD}-1.0	V_{LCD}-0.5	V_{LCD}-0.2	V
	V_{OH2}	P1 to P4: I_O=-1mA	V_{LCD}-1.0	-	-	
	V_{OH3}	S1 to S55: I_O=-20μA	V_{LCD}-1.0	-	-	
	V_{OH4}	COM1 to COM4: I_O=-100μA	V_{LCD}-1.0	-	-	
Output Low Level Voltage	V_{OL1}	KS1 to KS6: I_O=25μA	0.2	0.5	1.5	V
	V_{OL2}	P1 to P4: I_O=1mA	-	-	1.0	
	V_{OL3}	S1 to S55: I_O=20μA	-	-	1.0	
	V_{OL4}	COM1 to COM4: I_O=100μA	-	-	1.0	
	V_{OL5}	DO: I_O=1mA	-	0.1	0.5	
Output Middle Level Voltage (see note)	V_{MID1}	COM1 to COM4: 1/2 bias, I_O=±100μA	$1/2V_{LCD}$-1.0	-	$1/2V_{LCD}$+1.0	V
	V_{MID2}	S1 to S55: 1/3 bias, I_O=±20μA	$2/3V_{LCD}$-1.0	-	$2/3V_{LCD}$+1.0	
	V_{MID3}	S1 to S55: 1/3 bias, I_O=±20μA	$1/3V_{LCD}$-1.0	-	$1/3V_{LCD}$+1.0	
	V_{MID4}	COM1 to COM4: 1/3 bias, I_O=±100μA	$2/3V_{LCD}$-1.0	-	$2/3V_{LCD}$+1.0	
	V_{MID4}	COM1 to COM4: 1/3 bias, I_O=±100μA	$1/3V_{LCD}$-1.0	-	$1/3V_{LCD}$+1.0	
Oscillator Frequency	fosc	OSC: Rosc=43KΩ, Cosc=680pF	40	50	60	KHz
Current Drain	I_{DD1}	V_{DD}: Sleep mode	-	-	100	μA
	I_{DD2}	V_{DD}: V_{DD}=6.0V. output open, fosc=50KHz	-	270	540	
	I_{LCD1}	V_{LCD}: Sleep mode	-	-	5	
	I_{LCD2}	V_{LCD}: V_{LCD}=6.0V, output open, 1/2 bias, fosc=50KHz	-	200	400	
	I_{LCD3}	V_{LCD}: V_{LCD}=6.0V, output open, 1/3 bias, fosc=50KHz	-	120	240	

Note:
Excluding the bias voltage generation divider resistor built into VLCD1 and VLCD2. (See Figure 4.)

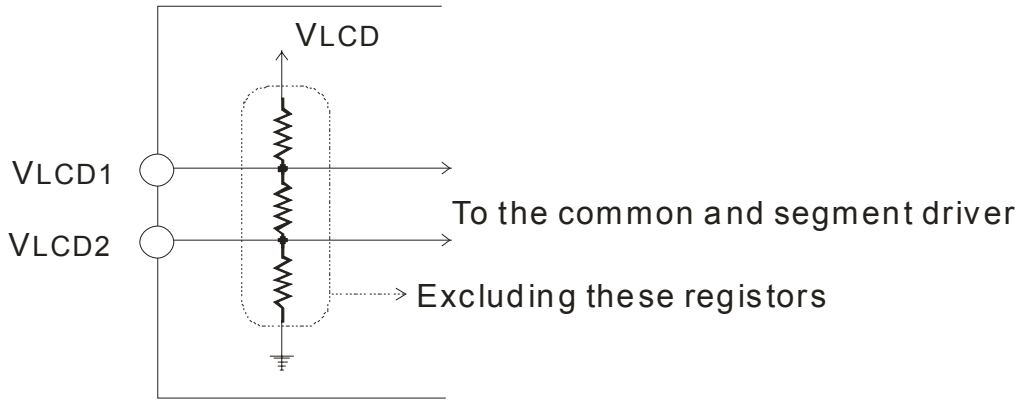
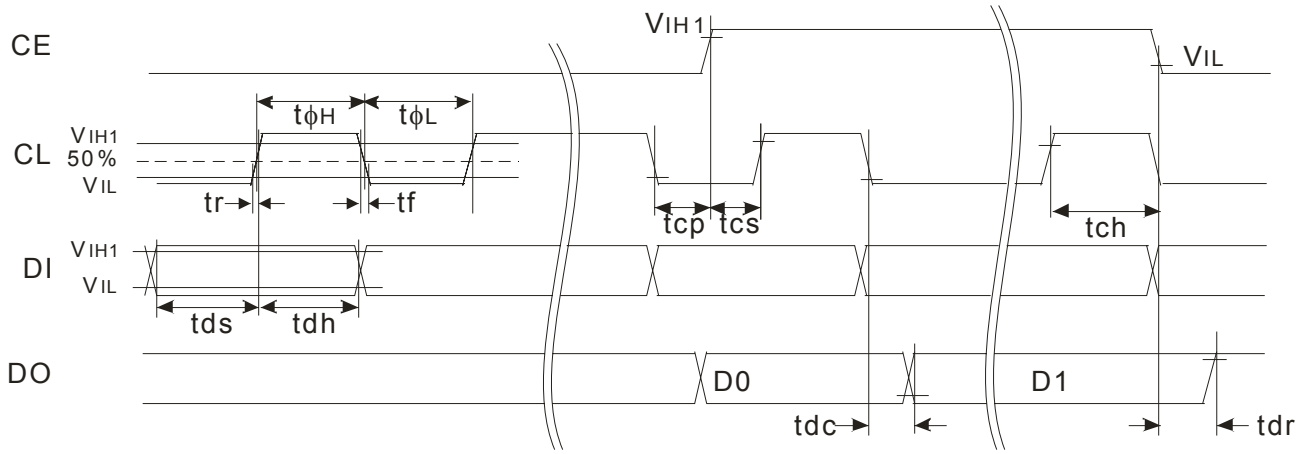


Figure 4

1. When CL is stopped at the low level



2. When CL is stopped at the high level

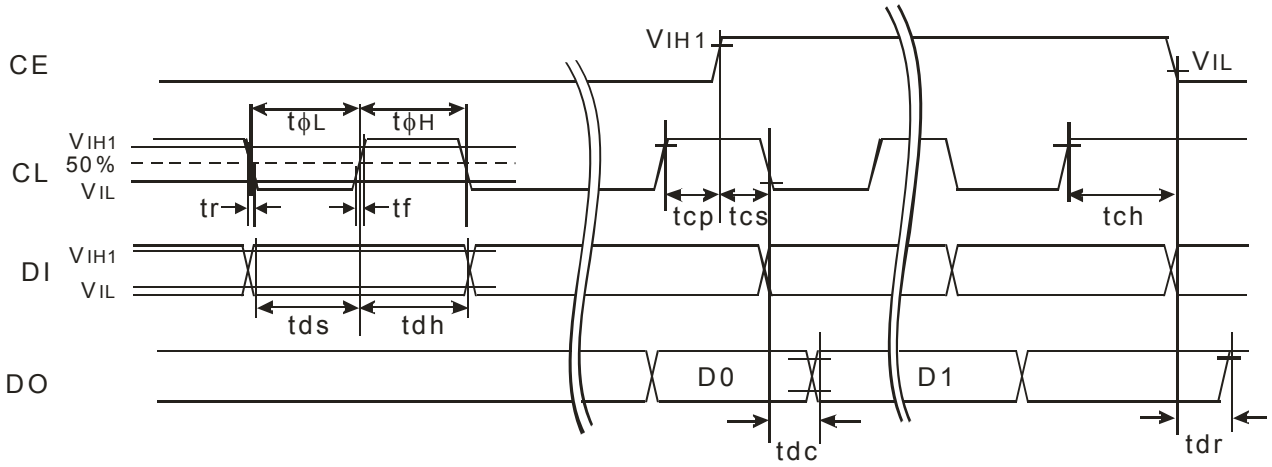
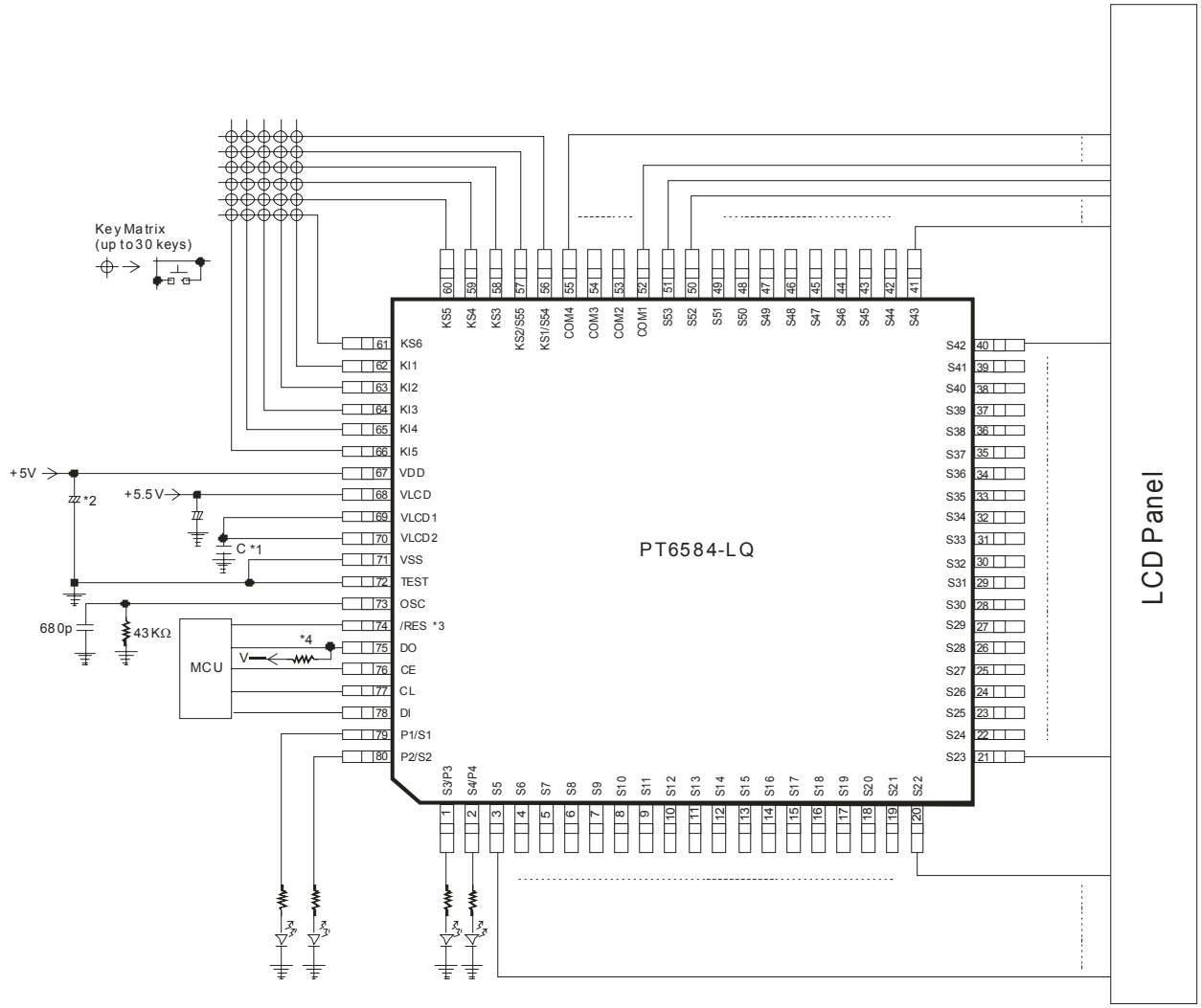


Figure 5

1/2 BIAS APPLICATION CIRCUIT

(FOR NORMAL PANEL USE)

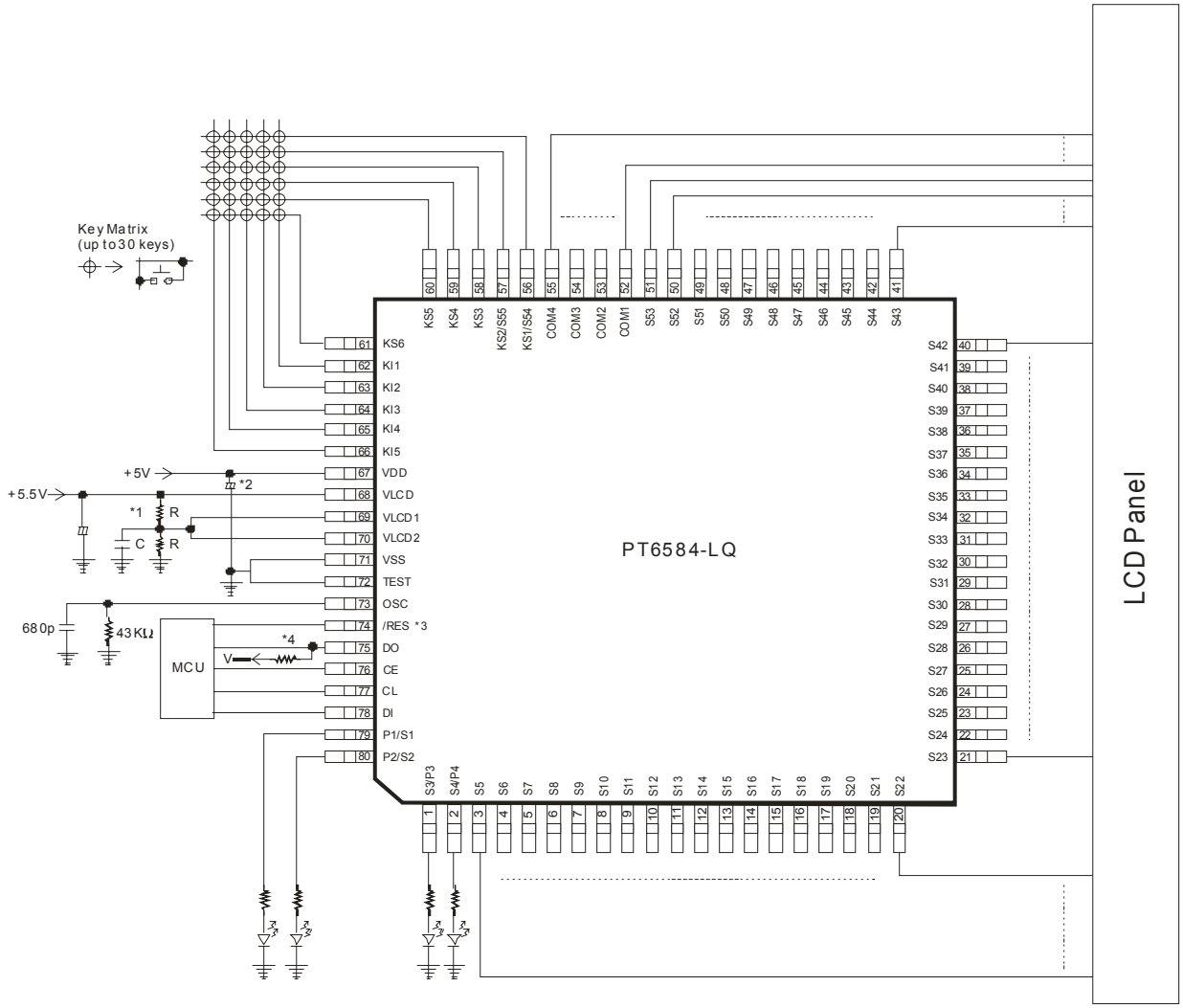


Notes:

1. C ≥ 0.047μF
2. Add a capacitor to the logic block power supply line so that the logic block power supply voltage VDD rise time when power is applied and the logic block power supply voltage VDD fall time when power drops are both at least 1ms, as the PT6584 is reset by the VDET.
3. If the /RES pin is not used for system reset, it must be connected to the logic block power supply VDD.
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1/2 BIAS APPLICATION CIRCUIT

(USE WITH LARGE PANEL)

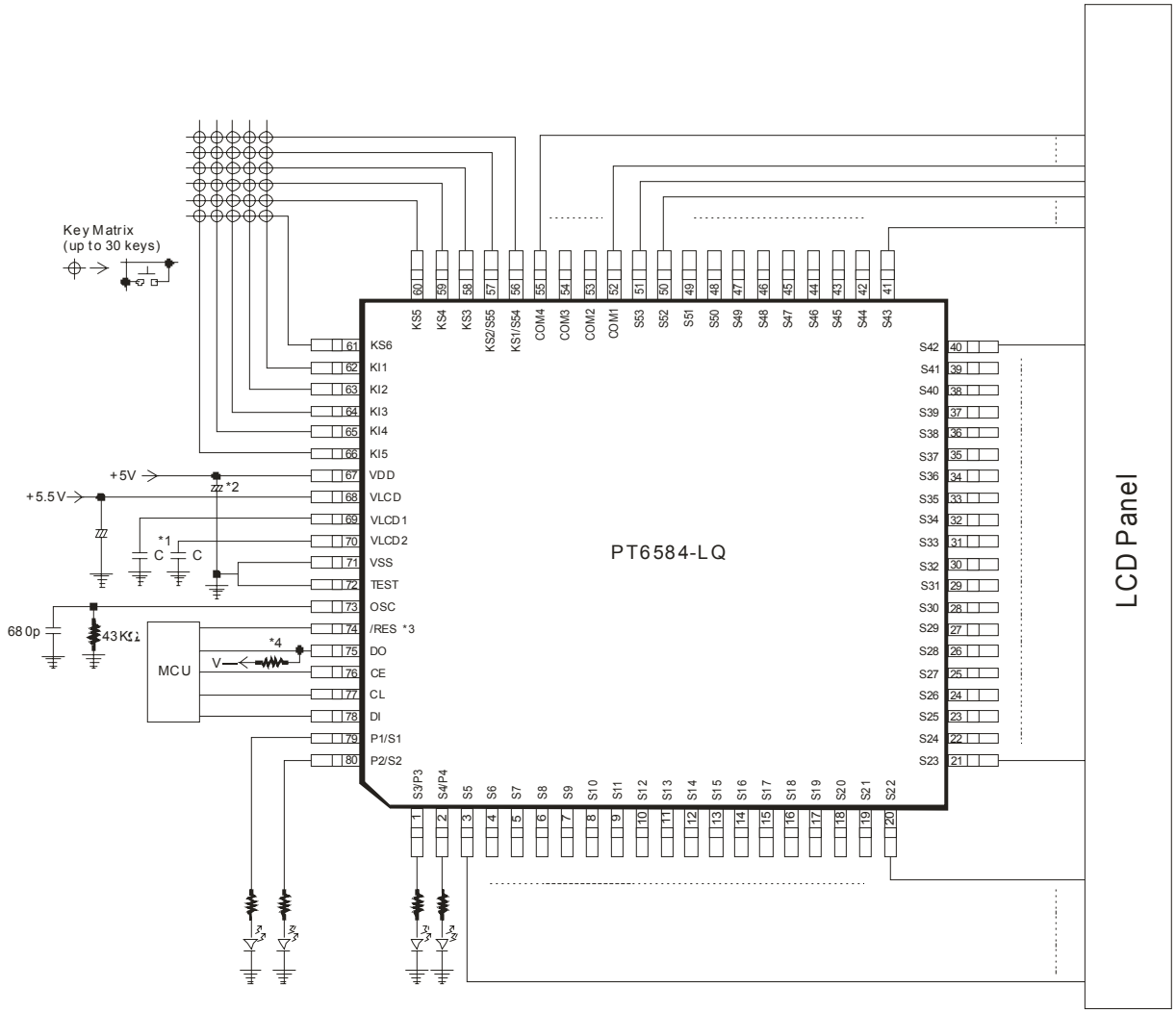


Notes:

1. C ≥ 0.047μF; 10KΩ ≥ R ≥ 1KΩ
2. Add a capacitor to the logic block power supply line so that the logic block power supply voltage VDD rise time when power is applied and the logic block power supply voltage VDD fall time when power drops are both at least 1ms, as the PT6584 is reset by the VDET.
3. If the /RES pin is not used for system reset, it must be connected to the logic block power supply VDD.
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1/3 BIAS APPLICATION CIRCUIT

(FOR NOEMAL LCD PANEL)

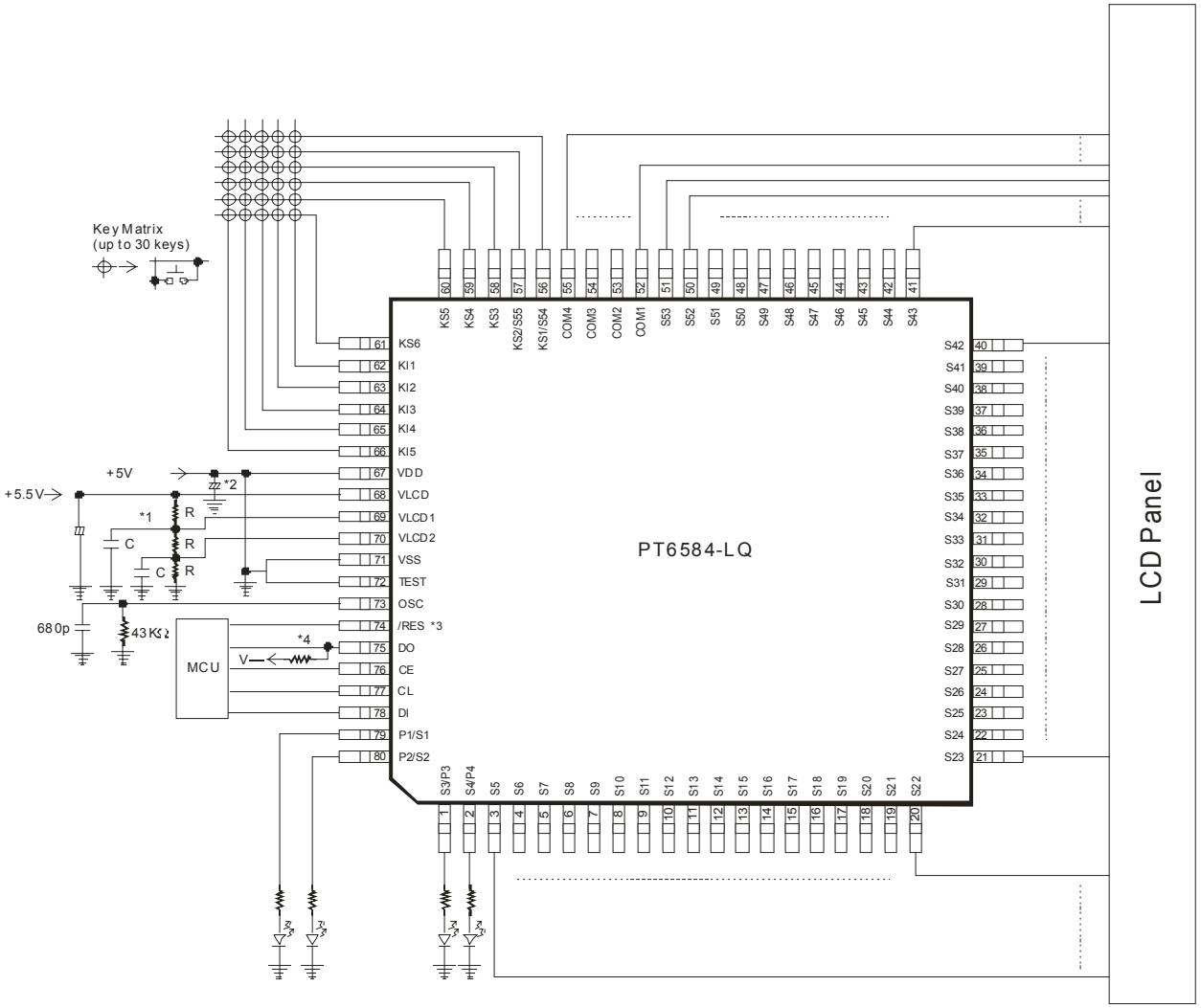


Notes:

1. C ≥ 0.047μF
2. Add a capacitor to the logic block power supply line so that the logic block power supply voltage VDD rise time when power is applied and the logic block power supply voltage VDD fall time when power drops are both at least 1ms, as the PT6584 is reset by the VDET.
3. If the /RES pin is not used for system reset, it must be connected to the logic block power supply VDD.
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1/3 BIAS APPLICATION CIRCUIT

(USE WITH LARGE PANEL)



Notes:

1. C ≥ 0.047μF; 10KΩ ≥ R ≥ 1KΩ
2. Add a capacitor to the logic block power supply line so that the logic block power supply voltage VDD rise time when power is applied and the logic block power supply voltage VDD fall time when power drops are both at least 1ms, as the PT6584 is reset by the VDET.
3. If the /RES pin is not used for system reset, it must be connected to the logic block power supply VDD.
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

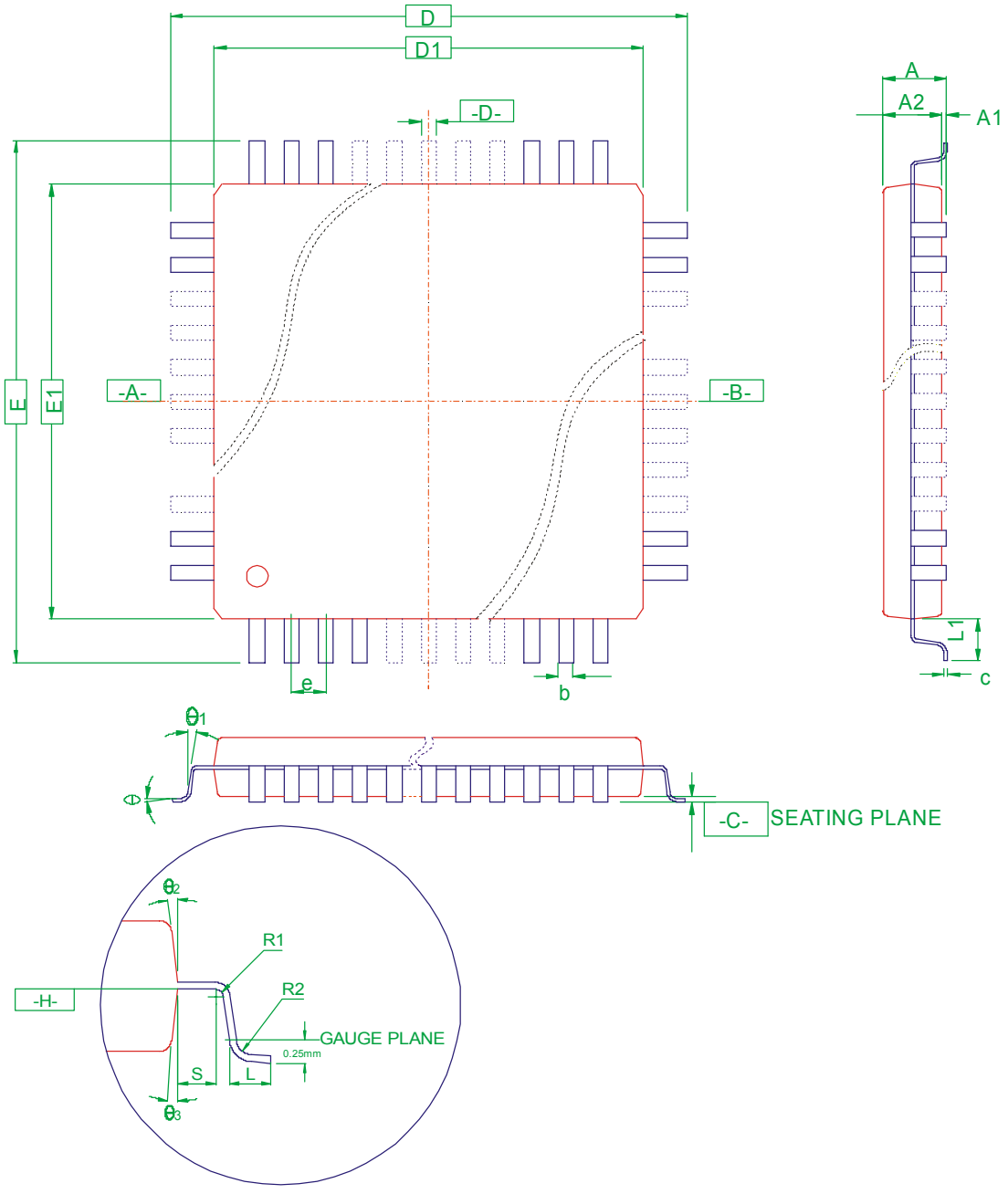
ORDER INFORMATION

Order Part Number	Package Type	Top Code
PT6584-Q	80 Pins, QFP	PT6584-Q
PT6584-LQ	80 Pins, LQFP	PT6584-LQ
PT6584-Q (L)	80 Pins, QFP	PT6584-Q
PT6584-LQ (L)	80 Pins, LQFP	PT6584-LQ

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the data code.

PACKAGE INFORMATION

80 PINS, QFP (BODY SIZE: 20MM X 14MM, PITCH: 0.80MM)

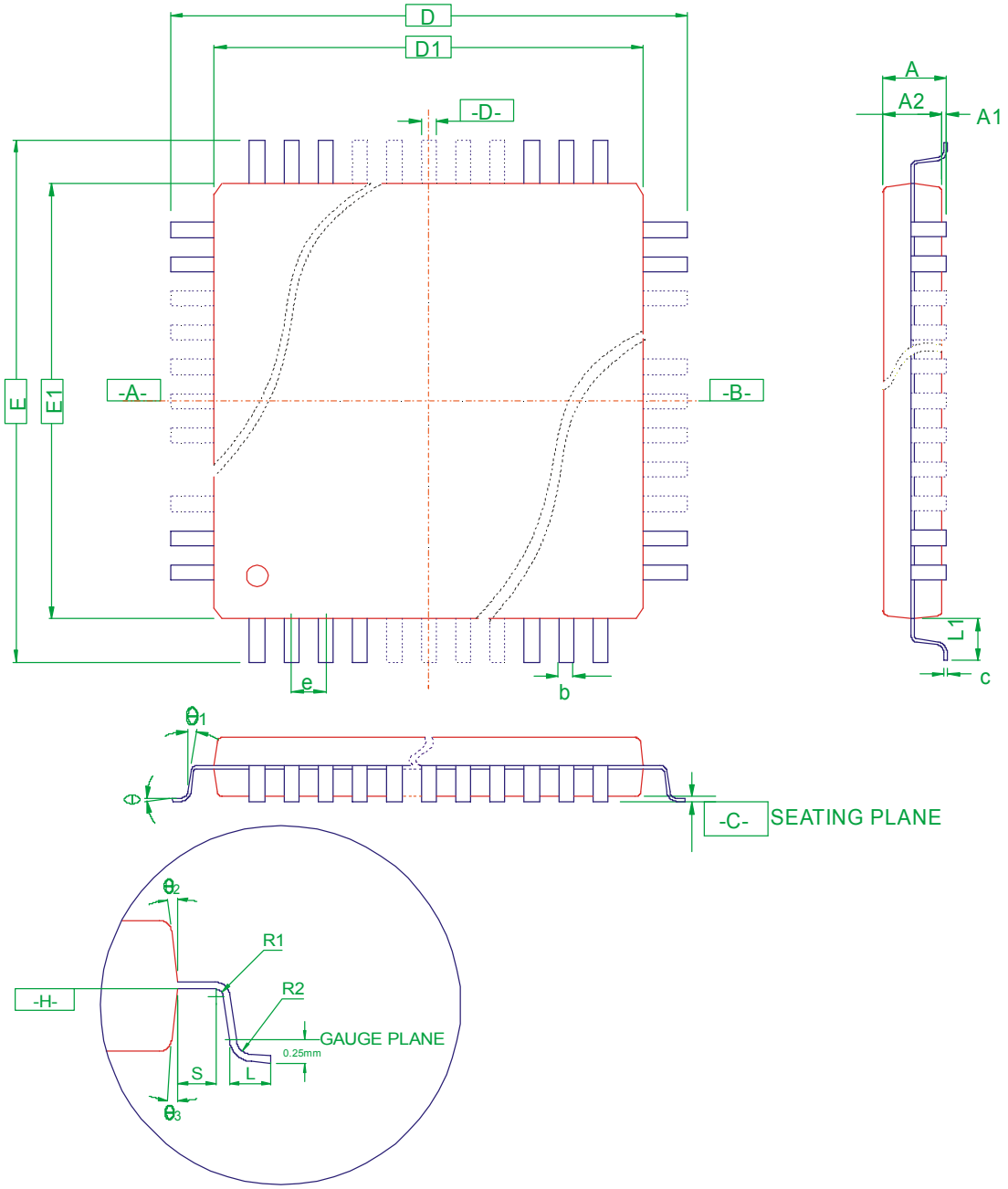


Symbol	Min.	Nom.	Max.
A	-	-	3.15
A1	0.00	-	0.25
A2	2.50	2.70	2.90
b	0.29	-	0.45
D	23.20 BSC.		
D1	20.00 BSC.		
E	17.20 BSC.		
E1	14.00 BSC.		
e	0.80 BSC.		
c	0.11	-	0.23
c1	0.11	0.15	0.19
L	0.73	0.88	1.03
L1	1.60 BSC.		
S	0.20	-	-
R1	0.13	-	-
R2	0.13	-	0.30
θ	0^o	-	7^o
$\theta1$	0^o	-	-
$\theta2$	5^o	-	16^o
$\theta3$	5^o	-	16^o

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Datum Plane H is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Datums A-B and D to be determined at Datum Plane H.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do not include mismatch and are determined at the datum plane H.
5. Details of Pin 1 identifier are optional but must be located within the zone indicated.
6. Regardless of the relative size of the upper and lower body sections, Dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold flash and gate burrs, but including any mismatch between the upper and lower section of the molded body.
7. Controlling Dimension: Millimeters
8. Dimension b does not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. dambar cannot be located on the lower radius or the lead foot.
9. N = No. of leads (N=80)
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.
11. Please refer to JEDEC MS-022 Variation GB-2.

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80 PINS, LQFP (BODY SIZE: 12X12, PITCH: 0.50, THK BODY: 1.40MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
S	0.20	-	-
R1	0.08	-	-
R2	0.08	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
C	0.09	-	0.20
θ	0^o	3.5^o	7^o
$\theta1$	0^o	-	-
$\theta2$	11^o	12^o	13^o
$\theta3$	11^o	12^o	13^o

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. The top package body may be smaller than the bottom package size as much as 0.15mm.
3. Datum A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25mm per side. d1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling Dimensions: Millimeters
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4mm and 0.5mm pitch package.
7. A1 is defined as the distance from the seating plane to the lowest point on the package body.
8. Refer to JEDEC MS-026 Variation BDD.

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