ESD134-B1-W0201

Bi-directional TVS device, 2.1 V, 0.25 pF, 0201

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Product description

This Infineon transient voltage suppressor (TVS) device has a bi-directional and symmetric *I*/*V* characteristic for optimized design and assembly.

Feature list

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD): ±28 kV (air) / ±23 kV (contact)
  - IEC61000-4-4 (EFT): ±2.5 kV (5/50 ns)
  - IEC61000-4-5 (Surge): ±7.5 A (8/20 µs)
- Bi-directional maximum working voltage: V_{WM} = ±2.1 V
- Line capacitance: C_L = 0.25 pF at f = 2.5 GHz
- Clamping voltage: V_{cl} = 7.7 V at I_{TLP} = 16 A with R_{dyn} = 0.28 Ω
- Very low leakage current: I_L = 20 nA (max.)
- Small form factor SMD size 0201, low profile (0.58 mm x 0.28 mm x 0.15 mm) *[2]*

RoHS

Potential applications

- USB 3.2 / 3.1 / 3.0 Gen 1 / Gen 2, Thunderbolt
- DVI, HDMI, Display Port

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

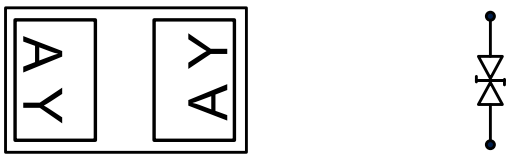

Figure 1 **Pin configuration (bottom view) and schematic diagram**

Table 1 **Part information**

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
ESD134-B1-W0201 / ESD134B1W0201E6327XTSA1	WLL-2-3	1 line, bi-directional	AY	15 k

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1 Absolute maximum ratings

Table 2 Absolute maximum ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Maximum working voltage	V_{WM}	-2.1	+2.1	V	
ESD discharge	V_{ESD} (contact)	-23	+23	kV	Discharge network: R = 330 Ω, C = 150 pF [1]
	V_{ESD} (air)	-28	+28		
Peak pulse power	P_{PK}	–	56	W	Stress pulse: 8/20 µs current waveform [2]
Peak pulse current	I_{PP}	-7.5	+7.5	A	Stress pulse: 8/20 µs current waveform [2]
Operating temperature range	T_{op}	-55	+125	°C	
Storage temperature	T_{stg}	-65	+150		

Attention**: **Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding only one of these values may cause irreversible damage to the component.

1 Based on IEC61000-4-2.
2 Based on IEC61000-4-5.

2 Electrical characteristics

Note: *T_A = 25 °C, unless otherwise specified. Device is electrically symmetrical.*

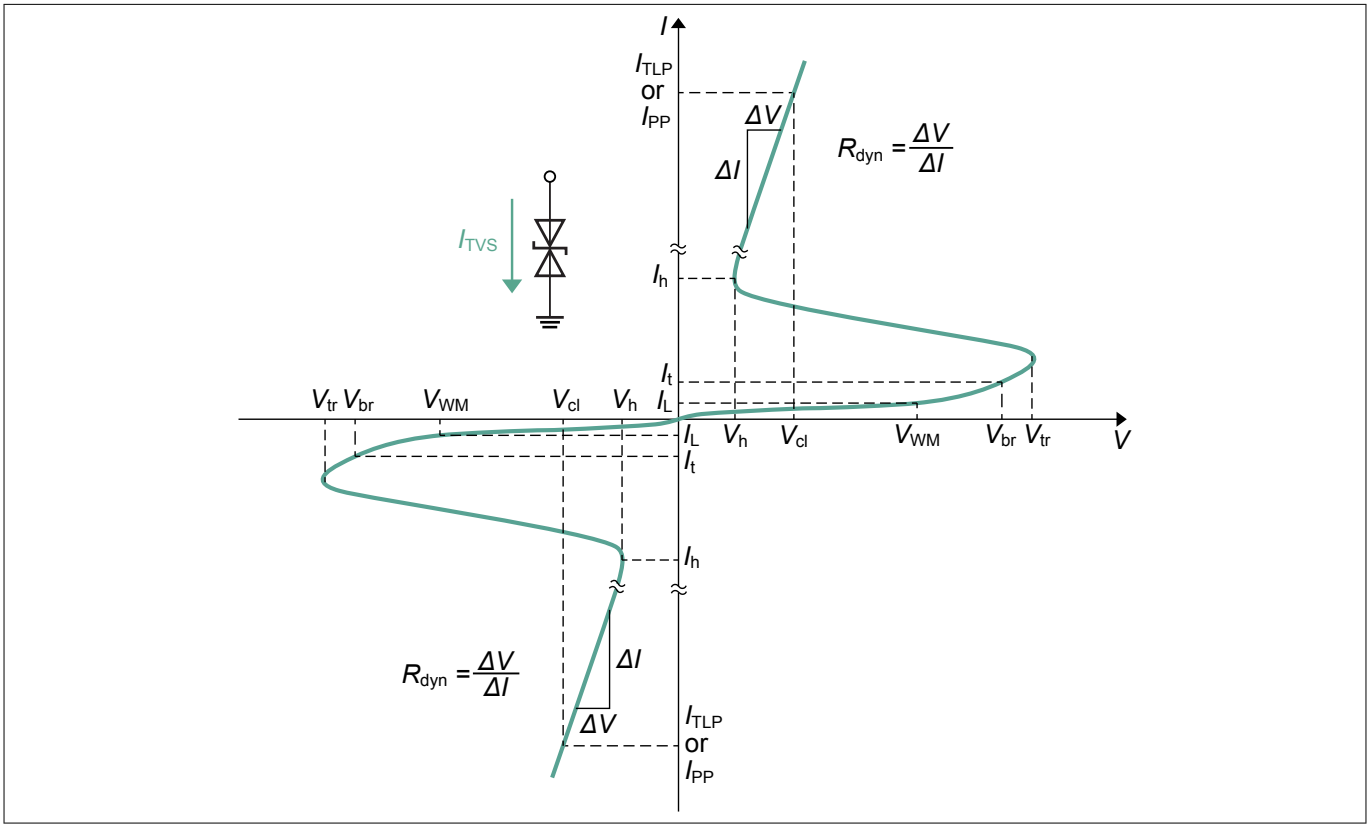

Figure 2 **Definitions of electrical characteristics**

Table 3 **Electrical parameters**

Symbol	Parameter
R_{dyn}	Dynamic resistance
V_{WM}	Maximum working voltage
V_{cl}	Clamping voltage
V_{TLP}	TLP voltage
I_{TLP}	TLP current
V_t	Test voltage
I_t	Test current
V_h	Holding voltage
I_h	Holding current
V_{br}	Breakdown voltage
V_{tr}	Trigger voltage
I_L	Leakage current
V_{ESD}	Maximum electrostatic discharge voltage, based on IEC61000-4-2
I_{PP}	Peak pulse current, based on IEC61000-4-5

Electrical characteristics

Table 4 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{br}	8	9.5	–	V	I_t = 1 mA
Holding voltage	V_h	–	1.8	–		$I = I_h$
Holding current	I_h	–	20	–	mA	$V = V_h$
Leakage current	I_L	–	–	20	nA	V_{WM} = ±2.1 V

Table 5 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.3	0.35	pF	V_t = 0 V, f = 1 MHz
		–	0.25	–		V_t = 0 V, f = 2.5 GHz

Table 6 ESD and surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage (TLP) [3]	V_{cl}	–	5.8	–	V	I_{TLP} = 8 A,
		–	7.7	–		I_{TLP} = 16 A
Clamping voltage (8/20) [4]		–	4.5	–		I_{PP} = 4 A,
		–	7.5	–		I_{PP} = 7.5 A
Dynamic resistance [3]	R_{dyn}	–	0.28	–	Ω	

3 Please refer to application note AN210 *[1]*. TLP parameters: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns

4 t_p = 8/20 µs. Stress pulse based on IEC61000-4-5.

3 Typical characteristic diagrams

Note: *T_A = 25 °C, unless otherwise specified.*

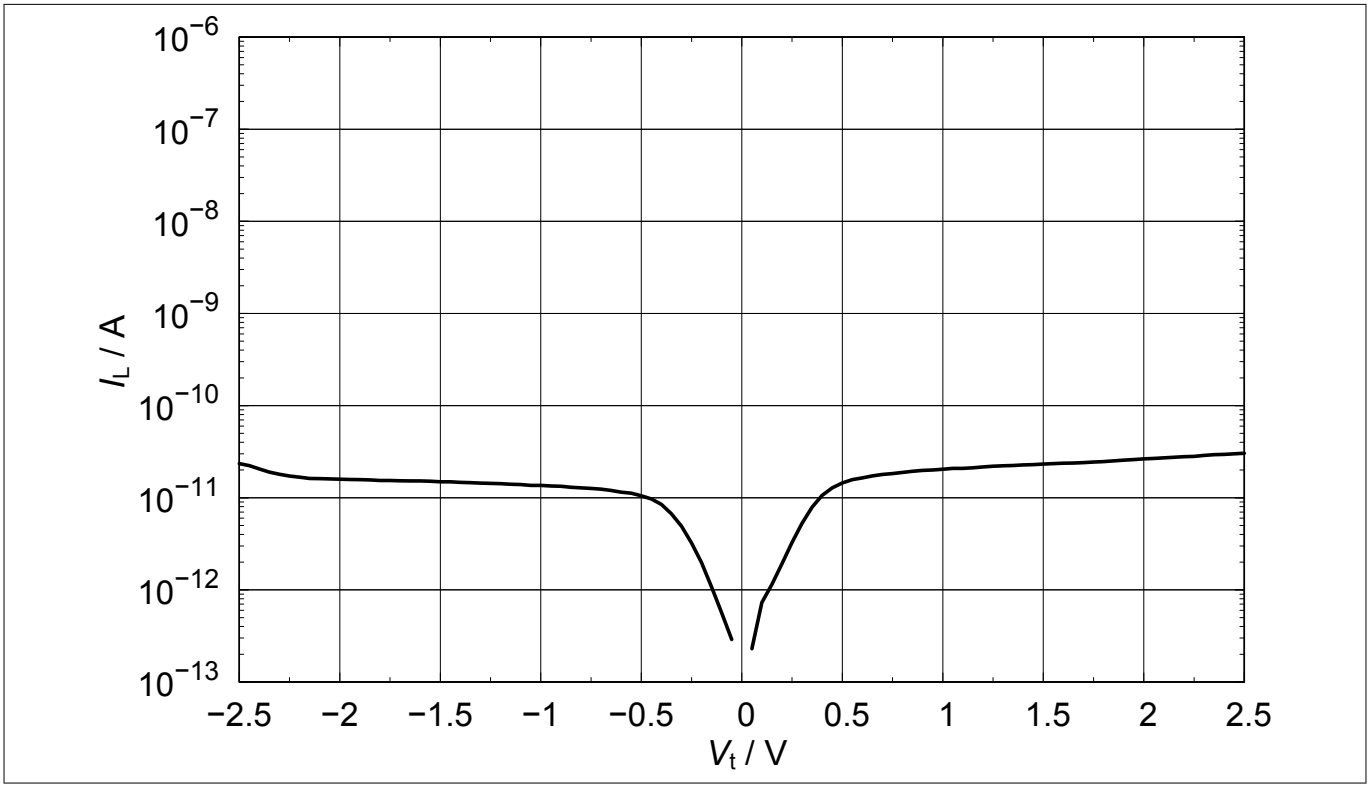

Figure 3 **Leakage current: $I_L = f(V_t)$**

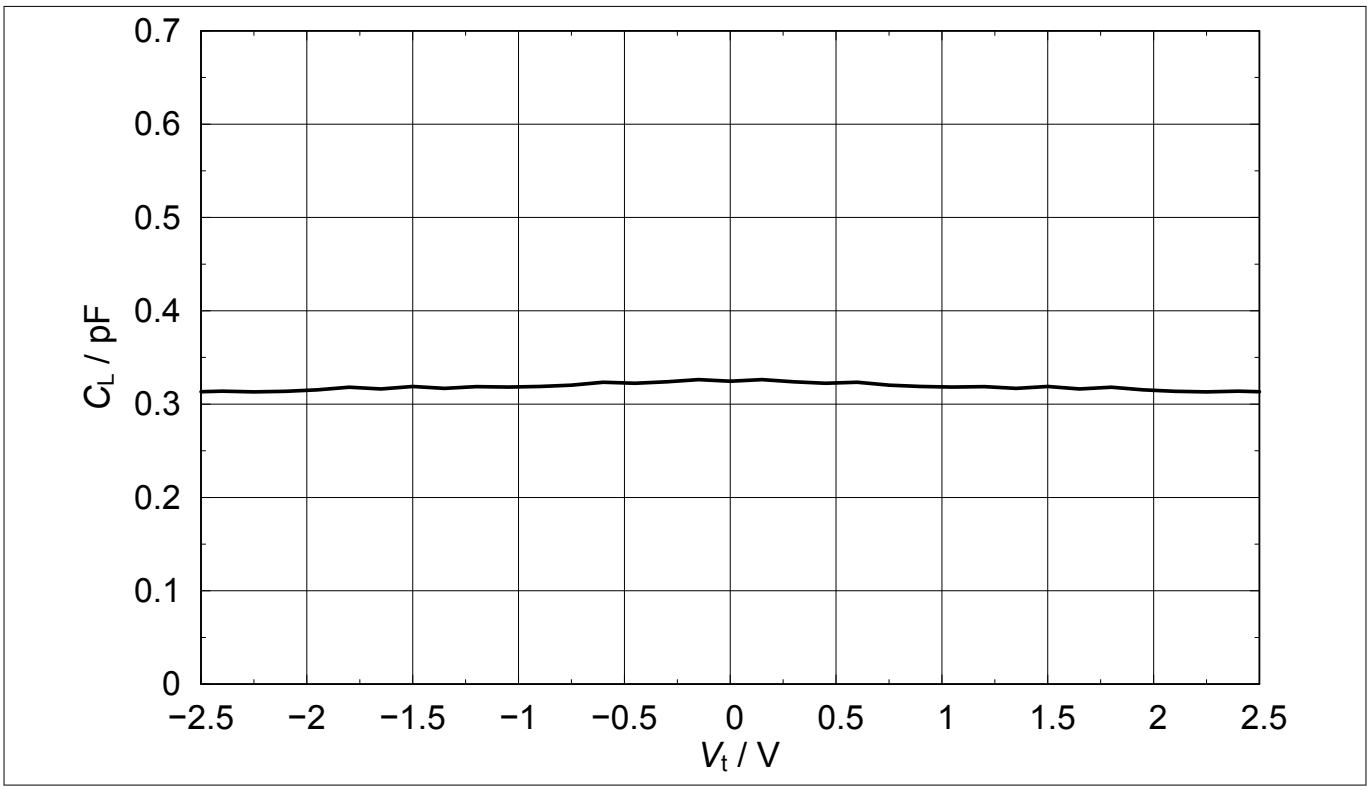

Figure 4 **Line capacitance: $C_L = f(V_t)$, f = 1 MHz**

Typical characteristic diagrams

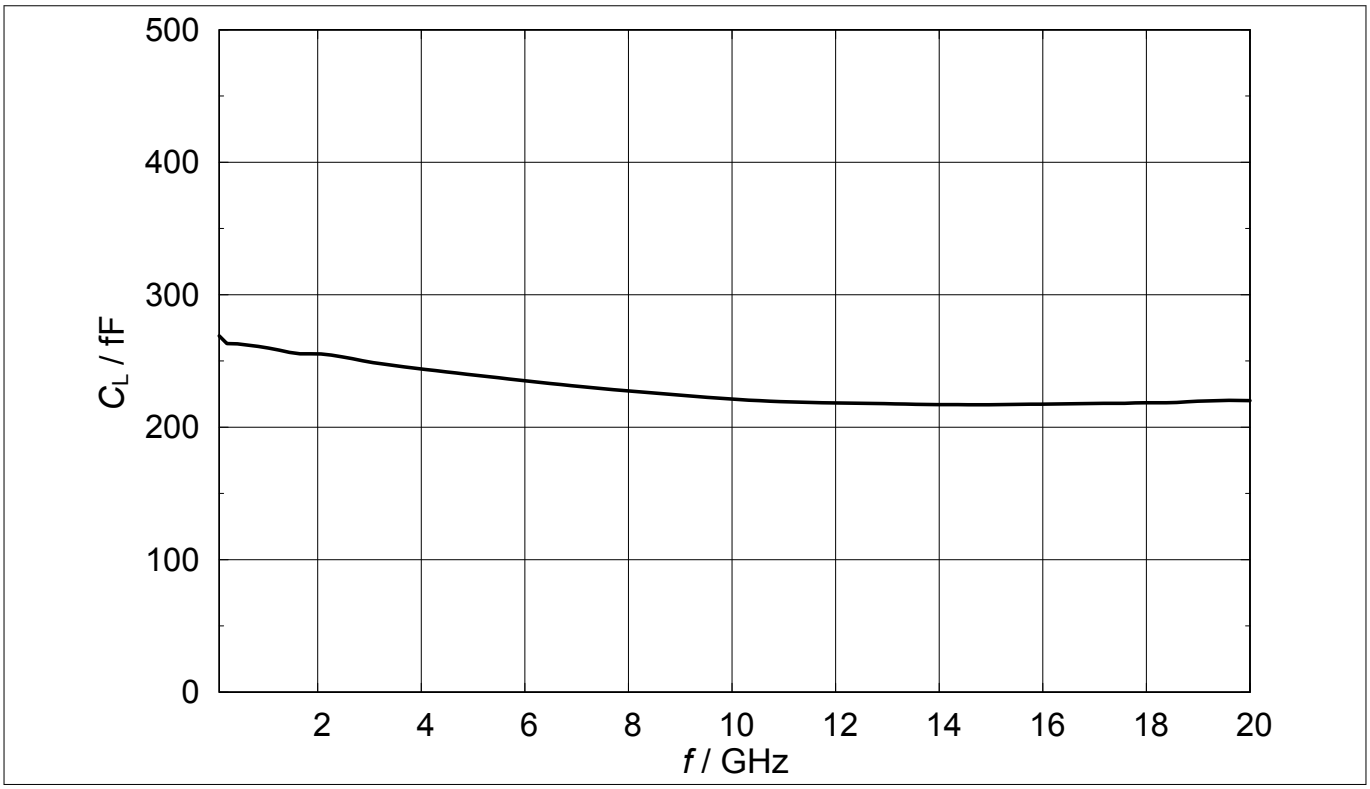

Figure 5 **Line capacitance: C_L = f(*f*), V_t = 0 V**

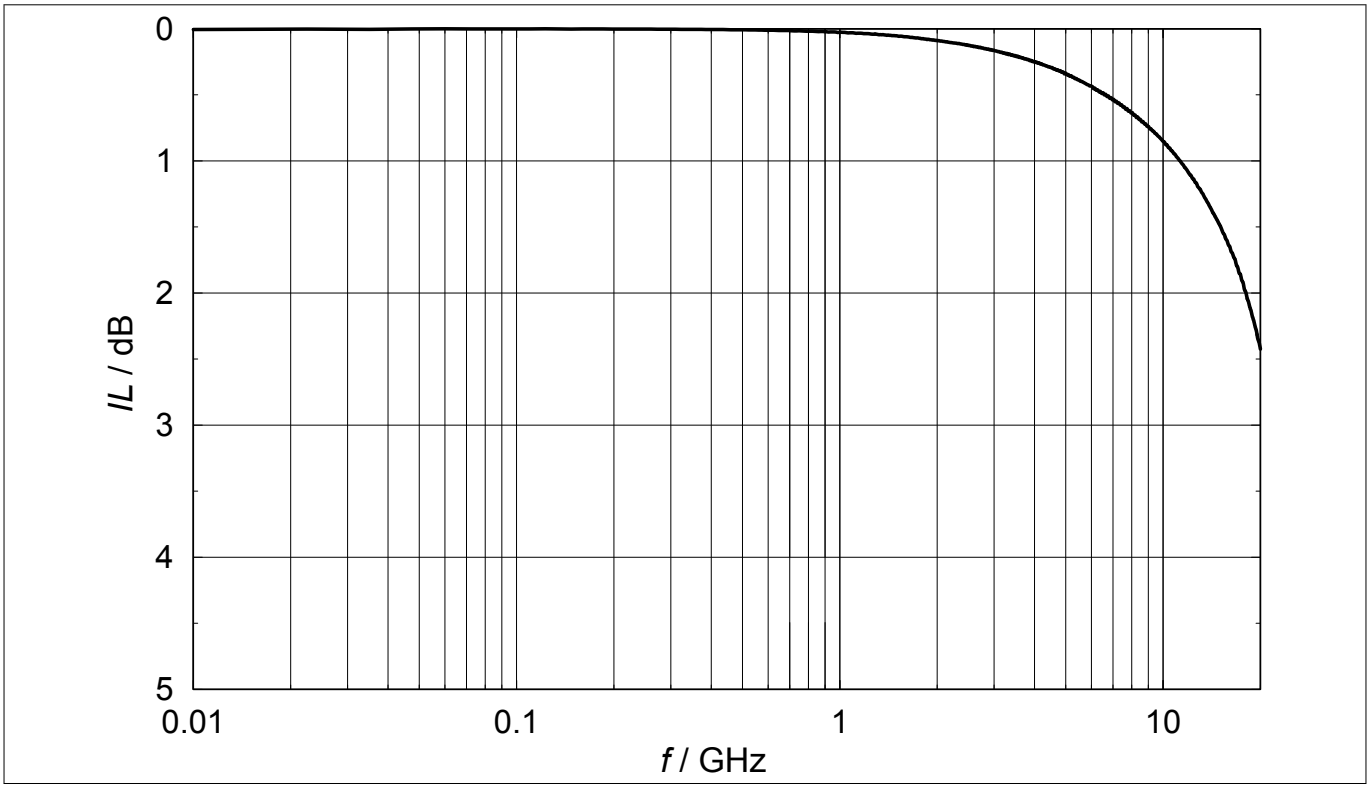

Figure 6 **Insertion loss: *IL* = f(*f*), measured in a 50 Ω system**

Typical characteristic diagrams

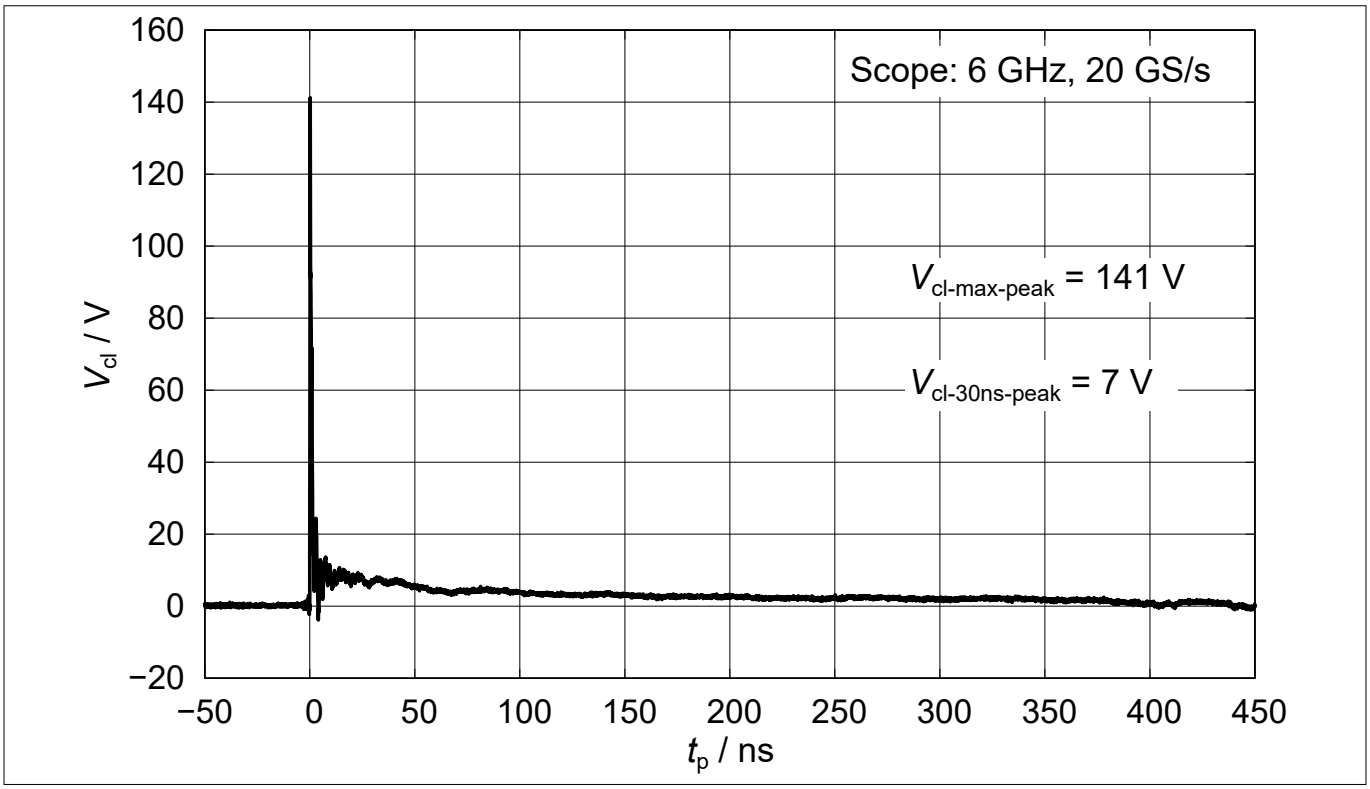

Figure 7 **Clamping voltage (ESD): V_{cl} = f(t_p), 8 kV positive pulse based on IEC61000-4-2**

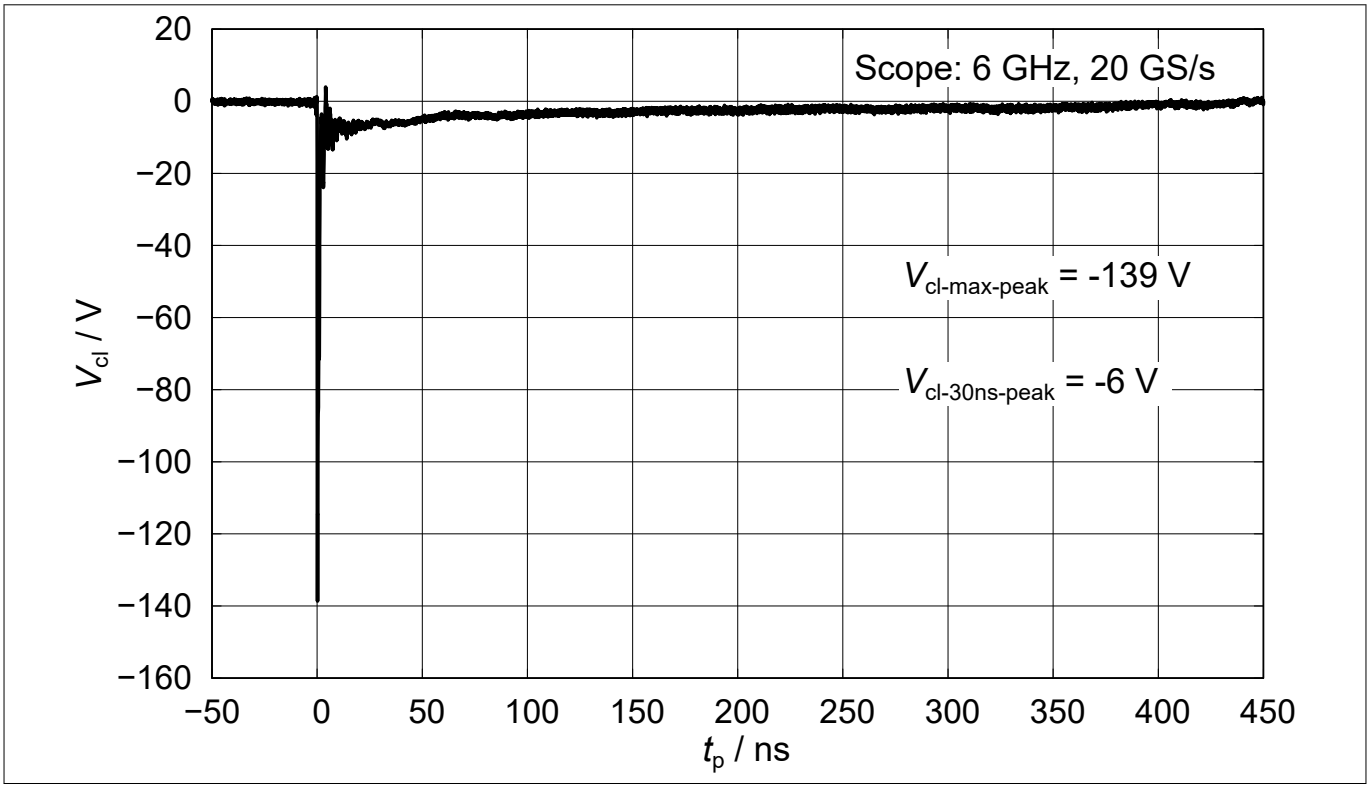

Figure 8 **Clamping voltage (ESD): V_{cl} = f(t_p), 8 kV negative pulse based on IEC61000-4-2**

Typical characteristic diagrams

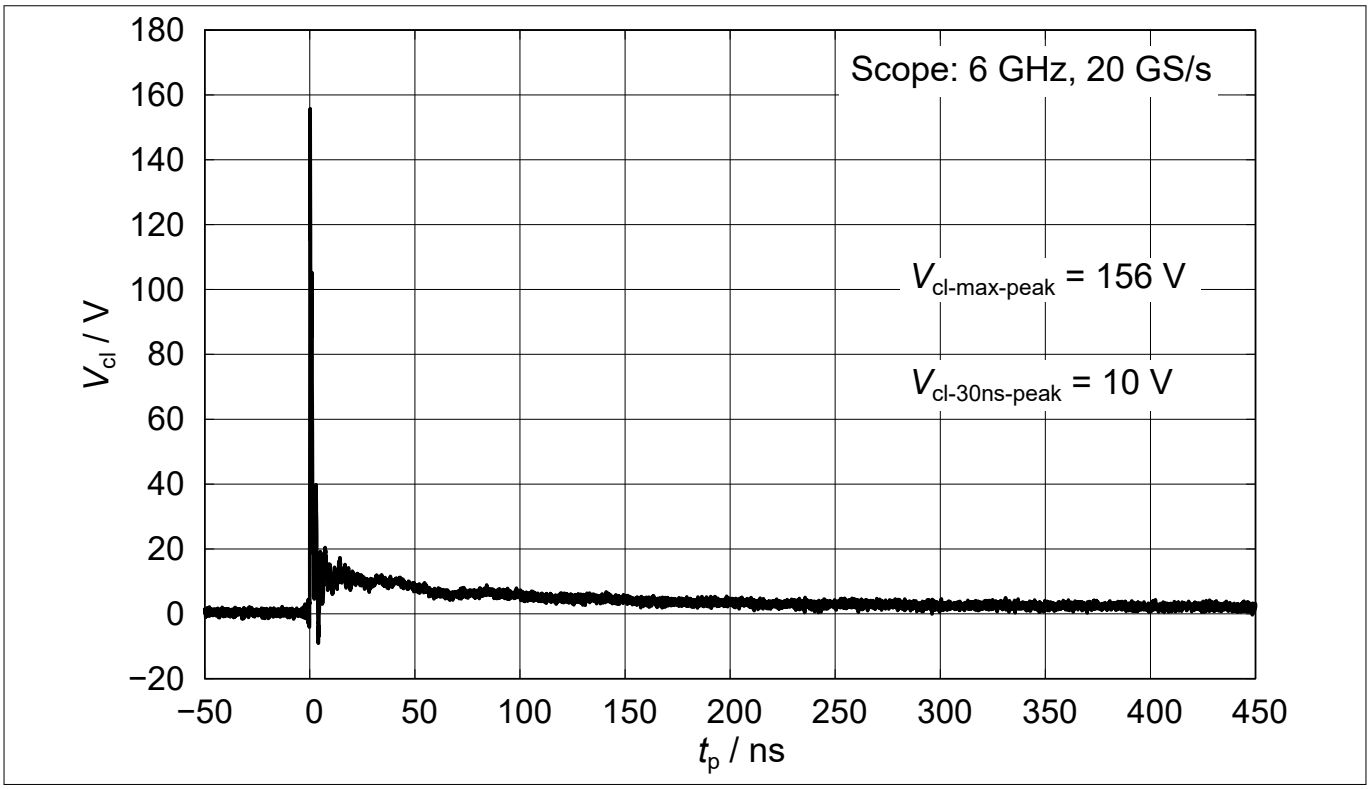

Figure 9 **Clamping voltage (ESD): V_{cl} = f(t_p), 15 kV positive pulse based on IEC61000-4-2**

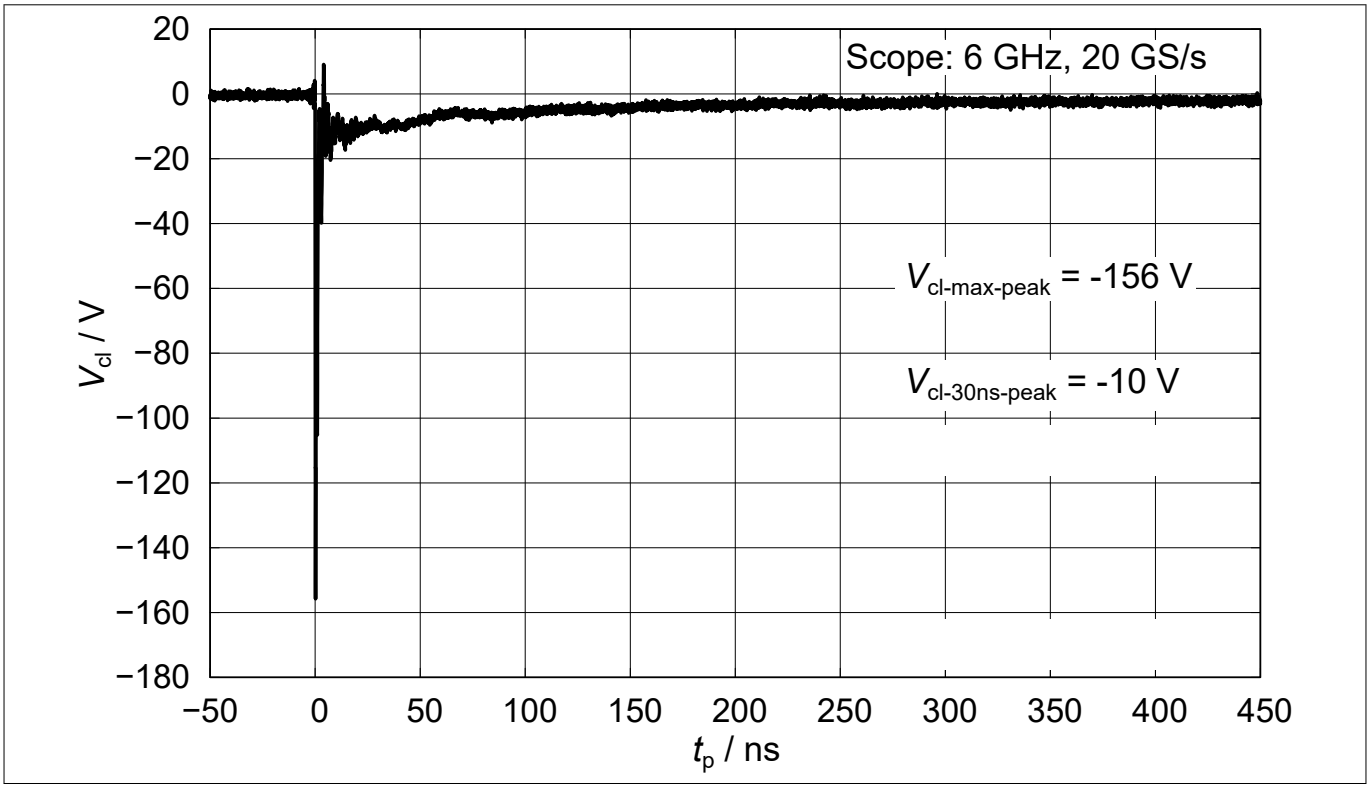

Figure 10 **Clamping voltage (ESD): V_{cl} = f(t_p), 15 kV negative pulse based on IEC61000-4-2**

Typical characteristic diagrams

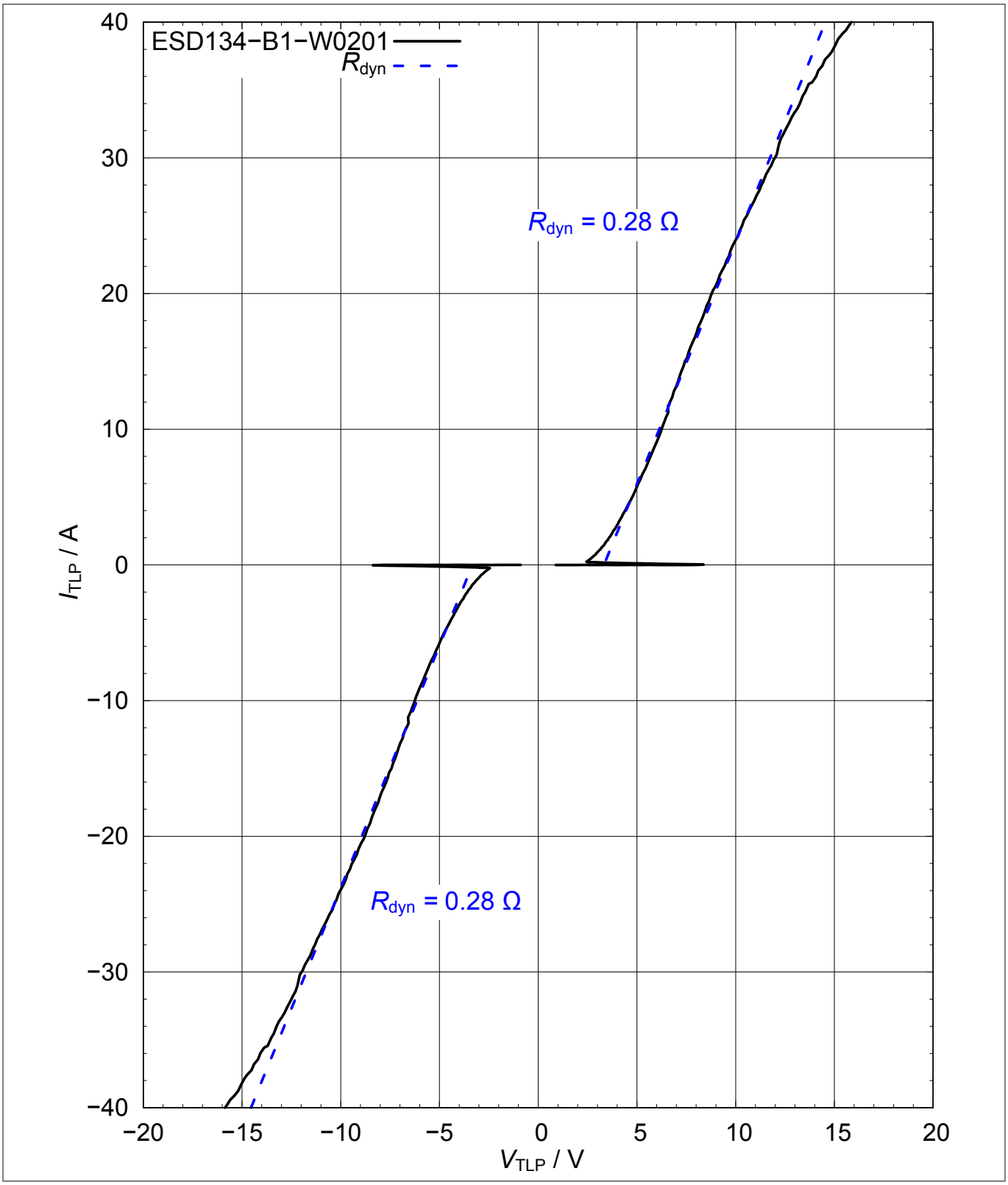

Figure 11 **Clamping voltage (TLP): I_{TLP} = f(V_{TLP})**

Typical characteristic diagrams

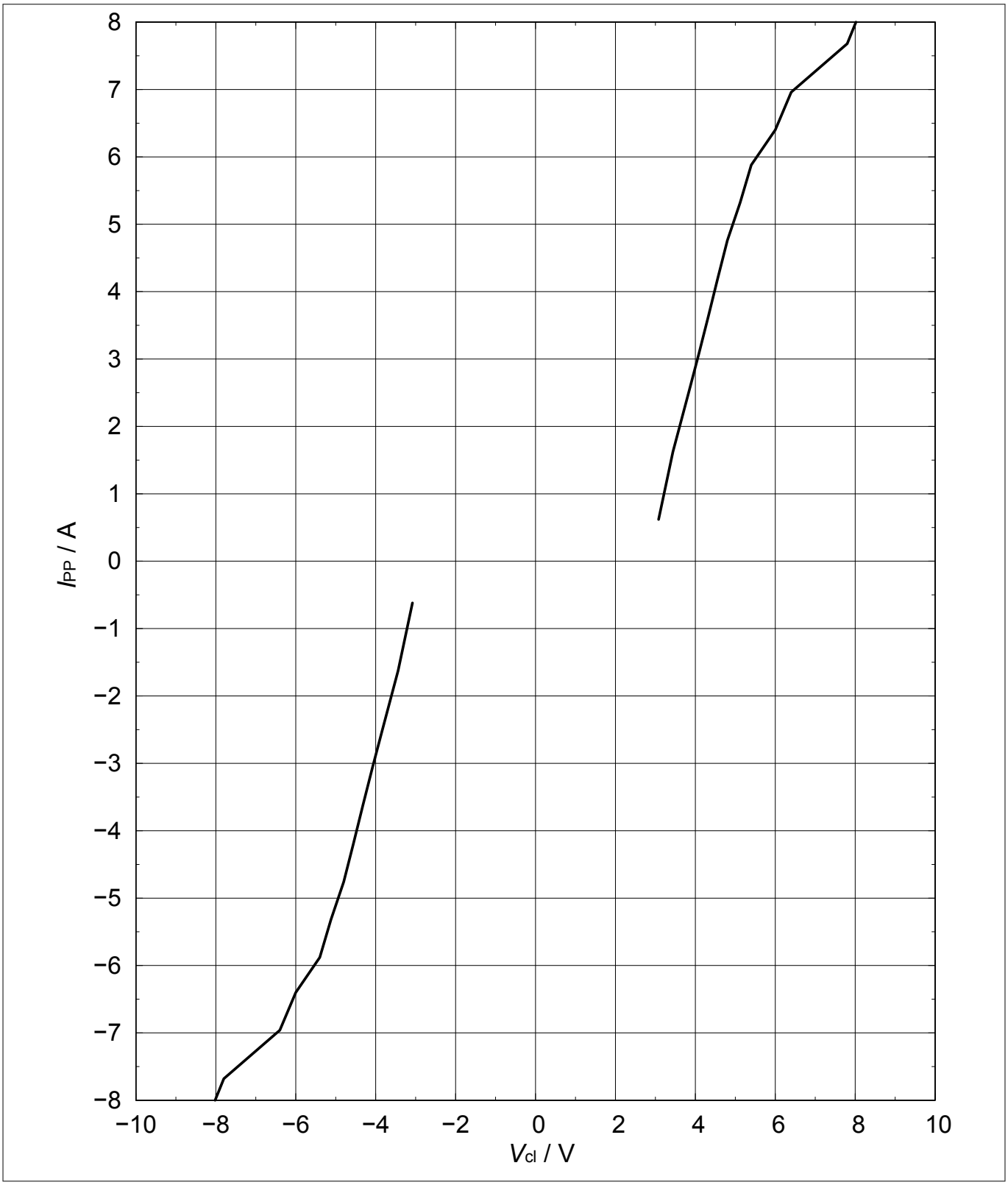

Figure 12 Clamping voltage (Surge): $I_{PP} = f(V_{cl})$, based on IEC61000-4-5

Typical characteristic diagrams

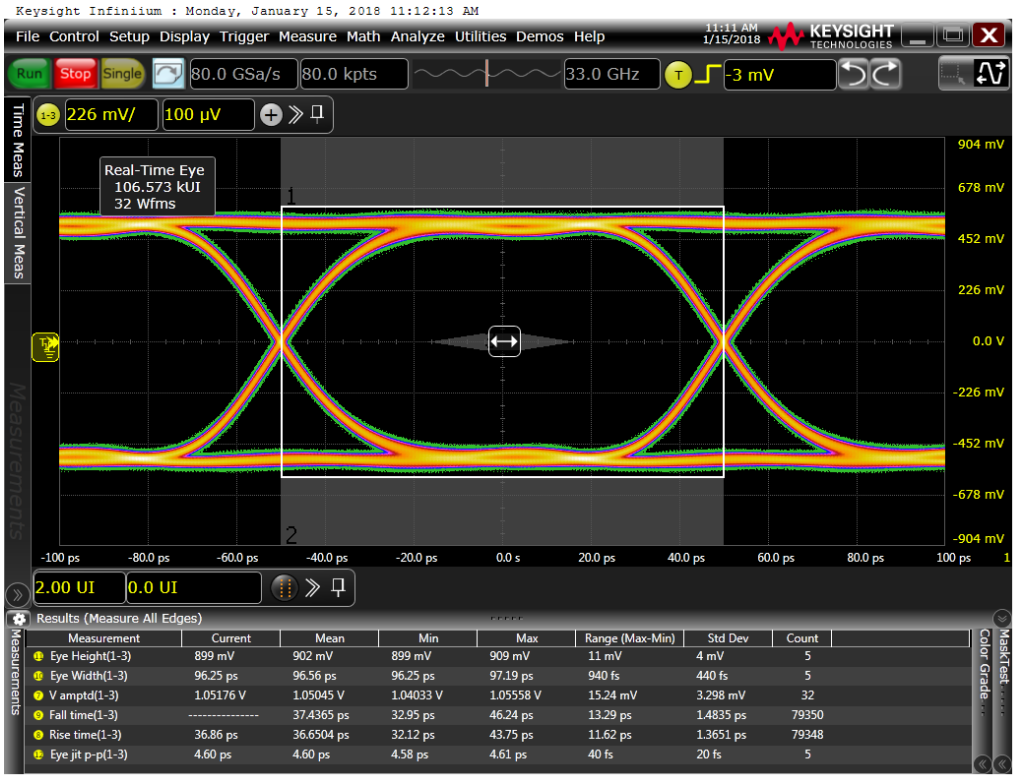

Figure 13 **10 Gbps Eye diagram with USB 3.1/3.2 Gen 2 Mask, test board only**

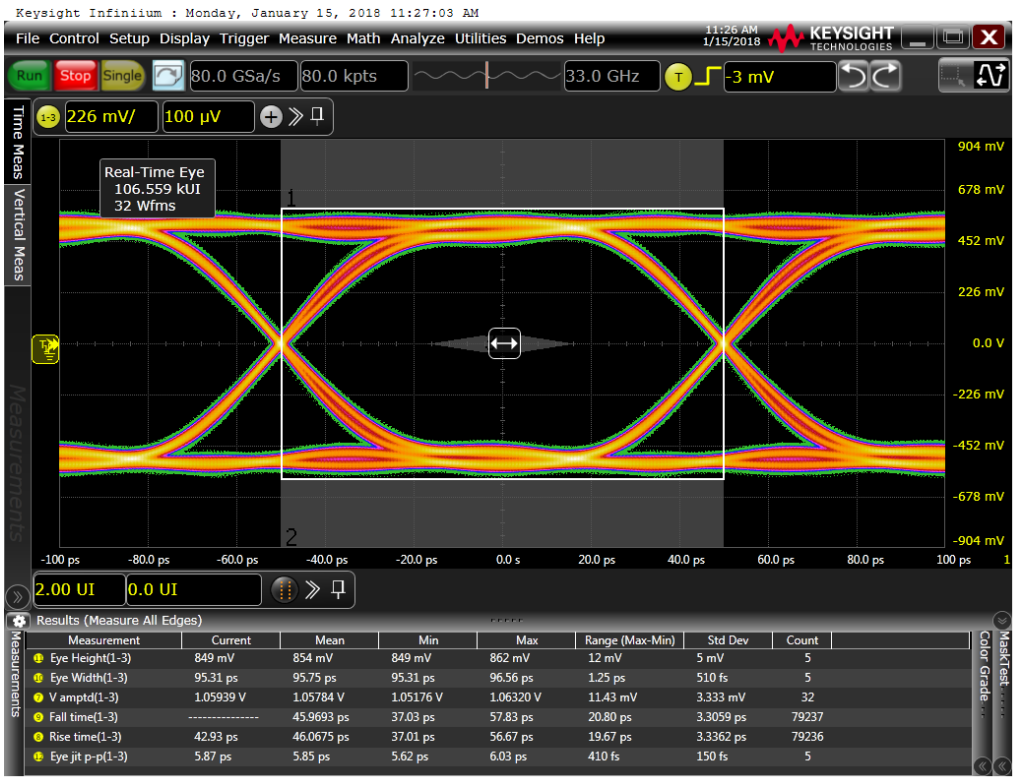

Figure 14 **10 Gbps Eye diagram with USB 3.1/3.2 Gen 2 Mask, test board + ESD134-B1-W0201**

4 Package information WLL-2-3

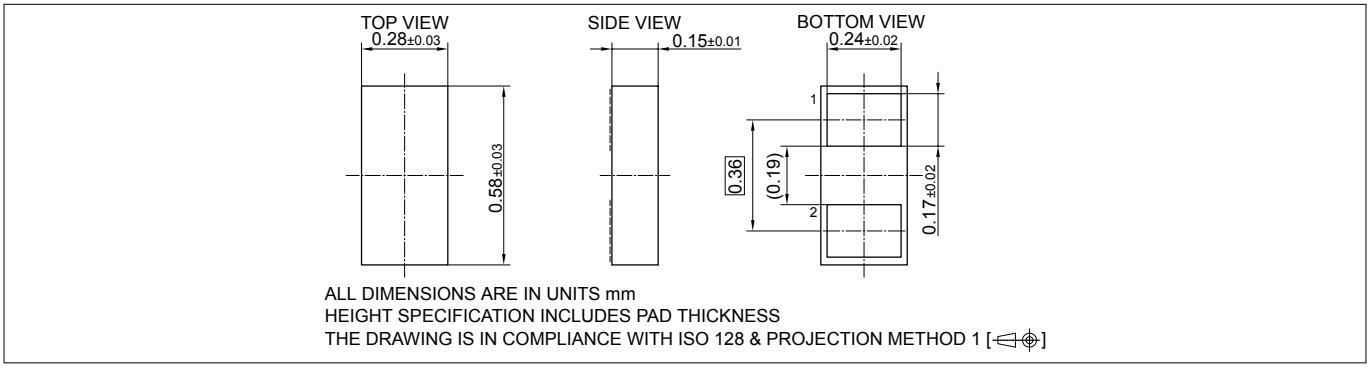

Figure 15 Package outline

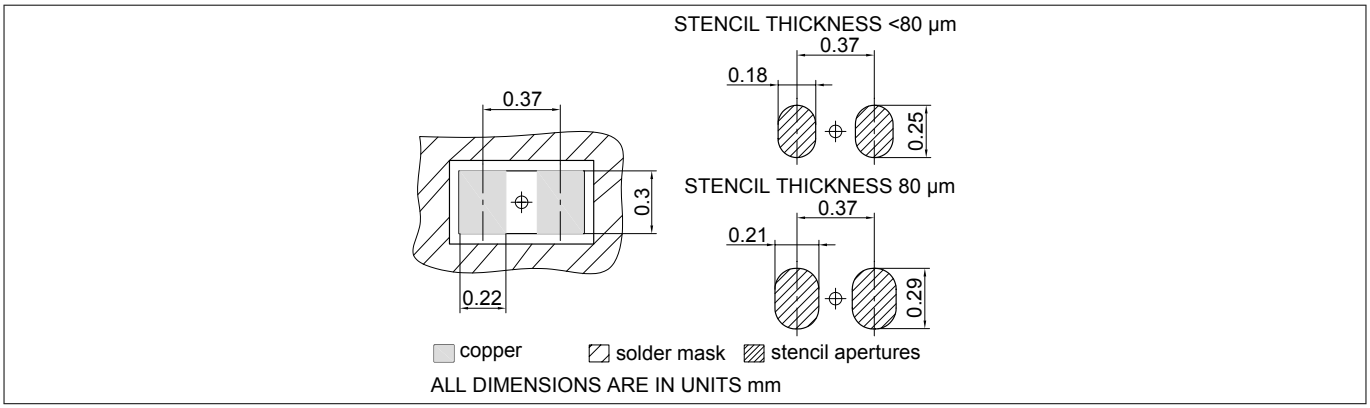

Figure 16 Footprint

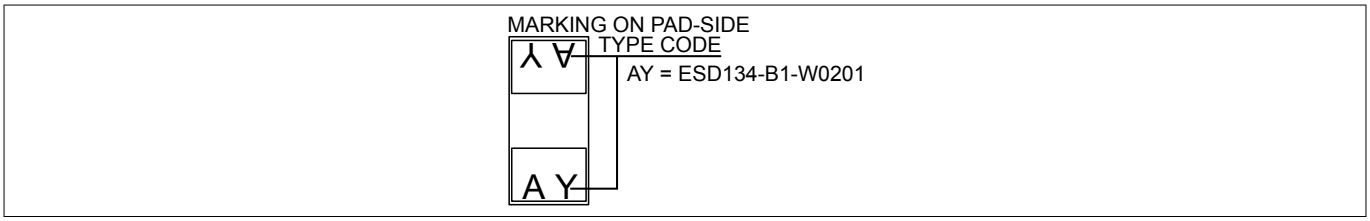

Figure 17 ESD134 Marking layout

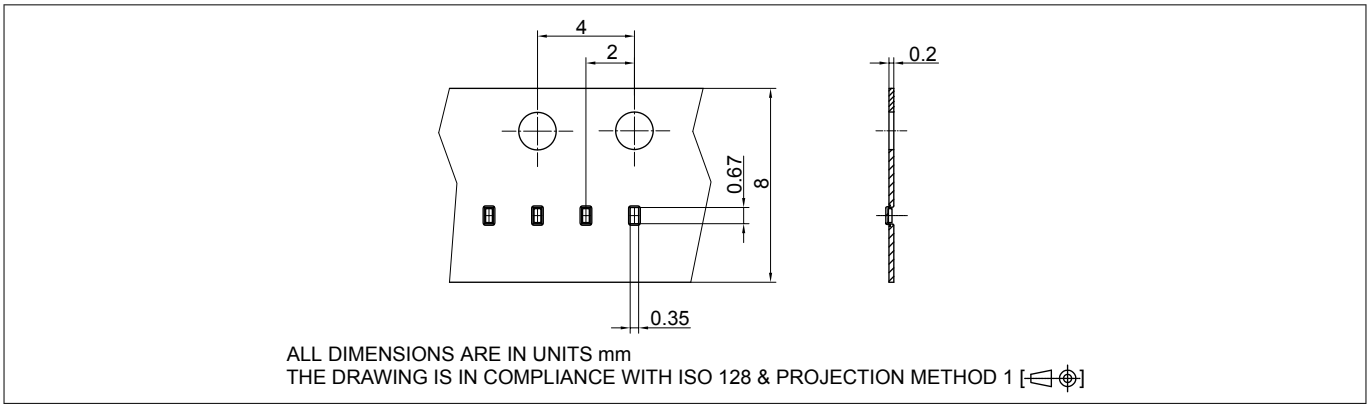

Figure 18 Packaging

5 References

[1]	Infineon AG - **Application note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
[2]	Infineon AG - **Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages** ***http://www.infineon.com/Packageinformation_WLL***

Revision history

Document version	Date of release	Description of changes
0.9.1	2018-04-17	• Values of V_{br} parameter updated
1.0	2018-11-23	• ESD values updated • Capacitance diagram C_L = f(f) added
2.0	2019-08-09	• New datasheet layout

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