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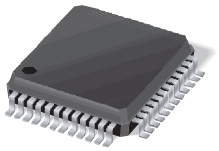


SINGLE 11-BIT, 65-MSPS HIGH IF SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 11-Bit Resolution
- 65-MSPS Maximum Sample Rate
- 2-V_{pp} Differential Input Range
- 3.3-V Single Supply Operation
- 1.8-V to 3.3-V Output Supply
- 400-mW Total Power Dissipation
- Two's Complement Output Format
- On-Chip S/H and Duty Cycle Adjust Circuit
- Internal or External Reference
- 63.3-dBFS SNR and 72.9-dBc SFDR at 65 MSPS and 220-MHz Input
- Power-Down Mode
- Single-Ended or Differential Clock
- 1-GHz −3-dB Input Bandwidth
- 48-Pin TQFP Package With PowerPad (7 mm x 7 mm body size)

APPLICATIONS

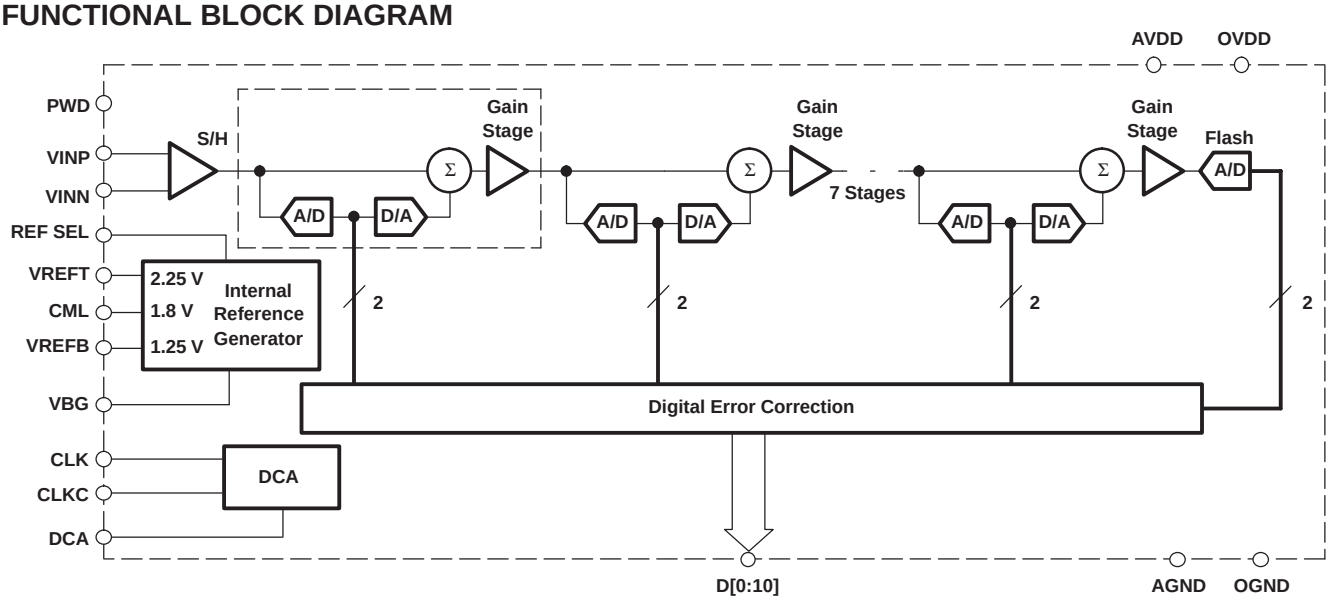
- Cellular Base Transceiver Station Receive Channel
  - − High IF Sampling Applications
  - − CDMA: IS-95, UMTS, CDMA1X
  - − TDMA: GSM, IS-136, EDGE/UWC-136
  - − Wireless Local Loop
  - − Wideband Baseband Receivers

DESCRIPTION

The ADS5413−11 is a low power, 11-bit, 65-MSPS, CMOS pipeline analog-to-digital converter (ADC) that operates from a single 3.3-V supply, while offering the choice of digital output levels from 1.8 V to 3.3 V. The low noise, high linearity, and low clock jitter makes the ADC well suited for high-input frequency sampling applications. On-chip duty cycle adjust circuit allows the use of a non-50% duty cycle. This can be bypassed for applications requiring low jitter or asynchronous sampling. The device can also be clocked with single ended or differential clock, without change in performance. The internal reference can be bypassed to use an external reference to suit the accuracy and low drift requirements of the application.

The device is specified over full temperature range (−40°C to +85°C).

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CommsADC is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5413−11	HTQFP-48(2) PowerPAD	PHP	−40°C to 85°C	A5413−11	ADS5413−11IPHP	Tray, 250

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 3,5 mm × 3,5 mm

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNITS
Supply voltage range	AVDD measured with respect to AGND	−0.3 V to 3.9 V
	OVDD measure with respect to OGND	−0.3 V to 3.9 V
Digital input, measured with respect to AGND		−0.3 V to AVDD + 0.3 V
Reference inputs Vrefb or Vreft, measured with respect to AGND		−0.3 V to AVDD + 0.3 V
Analog inputs Vinp or Vinn, measured with respect to AGND		−0.3 V to AVDD + 0.3 V
Maximum storage temperature		150°C
Soldering reflow temperature		235°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

	MIN	NOM	MAX	UNIT
ENVIRONMENTAL				
Operating free-air temperature, T_A	−40		85	°C
SUPPLIES				
Analog supply voltage, $V_{(AVDD)}$	3	3.3	3.6	V
Output driver supply voltage, $V_{(OVDD)}$	1.6		3.6	V
ANALOG INPUTS				
Input common-mode voltage		CML(2)		V
Differential input voltage range		2		V_{PP}
CLOCK INPUTS, CLK AND CLKC				
Sample rate, $f_S = 1/t_C$	5		65	MHz
Differential input swing (see Figure 16)	1		6	V_{PP}
Differential input common-mode voltage		1.65		V
Clock pulse width high, $t_{W(H)}$ (see Figure 15, with DCA off)	6.92			ns
Clock pulse width low, $t_{W(L)}$ (see Figure 15, with DCA off)	6.92			ns

(1) Recommended by design and characterization but not tested at final production unless specified under the *electrical characteristics* section.
(2) See $V_{(CML)}$ in the internal reference generator section.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, clock frequency = 65 MSPS, 50% clock duty cycle (AVDD = OVDD = 3.3 V), duty cylce adjust off, internal reference, A_{IN} = −1 dBFS, 1.2-V_{PP} square differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
Power Supply						
$I_{(AVDD)}$	Total analog supply current with internal reference and DCA on	A_{IN} = 0 dBFS, f_{IN} = 2 MHz		113		mA
	Analog supply current with external reference and DCA on			96		
	Analog supply current with internal reference and DCA off			107		
$I_{(OVDD)}$	Digital output driver supply current	A_{IN} = 0 dBFS, f_{IN} = 2 MHz		8		mA
P_D	Total power dissipation	A_{IN} = 0 dBFS, f_{IN} = 2 MHz		400	480	mW
P_D	Power down dissipation	PWDN = high		30	75	mW
DC Accuracy						
	No missing codes			Assured		
DNL	Differential nonlinearity	Sinewave input, f_{IN} = 2 MHz	−0.75	±0.3	0.75	LSB
INL	Integral nonlinearity	Sinewave input, f_{IN} = 2 MHz	−1	±0.5	1	LSB
E_O	Offset error	Sinewave input, f_{IN} = 2 MHz		3		mV
E_G	Gain error	Sinewave input, f_{IN} = 2 MHz		0.3		%FS
Internal Reference Generator						
V_{REFB}	Reference bottom		1.1	1.25	1.4	V
V_{REFT}	Reference top		2.1	2.25	2.4	V
	$V_{REFT} - V_{REFB}$			1.06		V
	$V_{REFT} - V_{REFB}$ variation (6σ)			0.06		V
$V_{(CML)}$	Common-mode output voltage			1.8		V
Digital Inputs (PWD, DCA, REF SEL)						
I_{IH}	High-level input current	V_I = 2.4 V	−60		60	µA
I_{IL}	Low-level input current	V_I = 0.3 V	−60		60	µA
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
Digital Outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = −50 µA			0.8	V
AC PERFORMANCE						
SNR	Signal-to-noise ratio	f_{IN} = 14 MHz	61.5	65.7		dBFS
		f_{IN} = 39 MHz		65.9		
		f_{IN} = 70 MHz		65.7		
		f_{IN} = 150 MHz		64.3		
		f_{IN} = 190 MHz		63.9		
		f_{IN} = 220 MHz		63.3		
SINAD	Signal-to-noise and distortion	f_{IN} = 14 MHz	61	65.3		dBFS
		f_{IN} = 39 MHz		65.3		
		f_{IN} = 70 MHz		65.5		
		f_{IN} = 150 MHz		63.2		
		f_{IN} = 190 MHz		62.3		
		f_{IN} = 220 MHz		62.4		

ELECTRICAL CHARACTERISTICS (CONTINUED)

over operating free-air temperature range, clock frequency = 65 MSPS, 50% clock duty cycle (AVDD = OVDD = 3.3 V), duty cylce adjust off, internal reference, A_{IN} = −1 dBFS, 1.2-V_{PP} square differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE (Continued)						
SFDR	Spurious free dynamic range	f_{IN} = 14 MHz	70	77.7		dBc
		f_{IN} = 39 MHz		75.8		
		f_{IN} = 70 MHz		84.5		
		f_{IN} = 150 MHz		70.5		
		f_{IN} = 190 MHz		68.3		
		f_{IN} = 220 MHz		72.9		
HD2	Second order harmonic	f_{IN} = 14 MHz		95		dBc
		f_{IN} = 39 MHz		94		
		f_{IN} = 70 MHz		89		
		f_{IN} = 150 MHz		79		
		f_{IN} = 190 MHz		84.5		
		f_{IN} = 220 MHz		72		
HD3	Third order harmonic	f_{IN} = 14 MHz		77.6		dBc
		f_{IN} = 39 MHz		75.4		
		f_{IN} = 70 MHz		85.5		
		f_{IN} = 150 MHz		70.5		
		f_{IN} = 190 MHz		68.3		
		f_{IN} = 220 MHz		77.6		
	Analog input bandwidth	−3 dB BW respect to −3 dBFS input at low frequency		1		GHz

TIMING CHARACTERISTICS

25°C, C_L = 10 pF

			MIN	TYP	MAX	UNIT
$t_{d(A)}$	Aperture delay			2		ns
	Aperture jitter			0.4		ps
$t_{d(Pipe)}$	Latency			6		Cycles
t_{d1}	Propagation delay from clock input to beginning of data stable(1)	DCS off, OVDD = 1.8 V		8		ns
t_{d2}	Propagation delay from clock input to end of data stable(1)			20.3		
t_{d1}	Propagation delay from clock input to beginning of data stable(1)	DCS off, OVDD = 3.3 V		7		ns
t_{d2}	Propagation delay from clock input to end of data stable(1)			20.3		
t_{d1}	Propagation delay from clock input to beginning of data stable(1)	DCS on, OVDD = 1.8 V		10		ns
t_{d2}	Propagation delay from clock input to end of data stable(1)			22.3		
t_{d1}	Propagation delay from clock input to beginning of data stable(1)	DCS on, OVDD = 3.3 V		9		ns
t_{d2}	Propagation delay from clock input to end of data stable(1)			22.3		

(1) Data stable if V_O < 10% OVDD or V_O > 90% OVDD

TIMING DIAGRAM

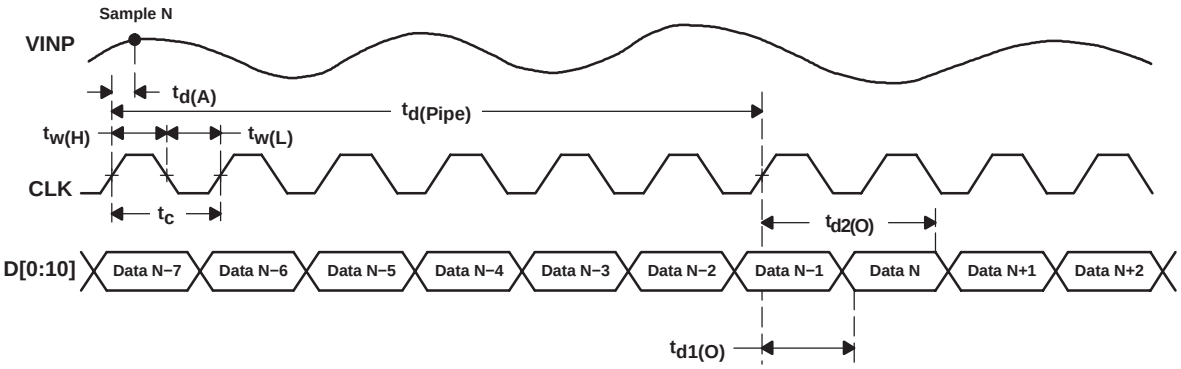
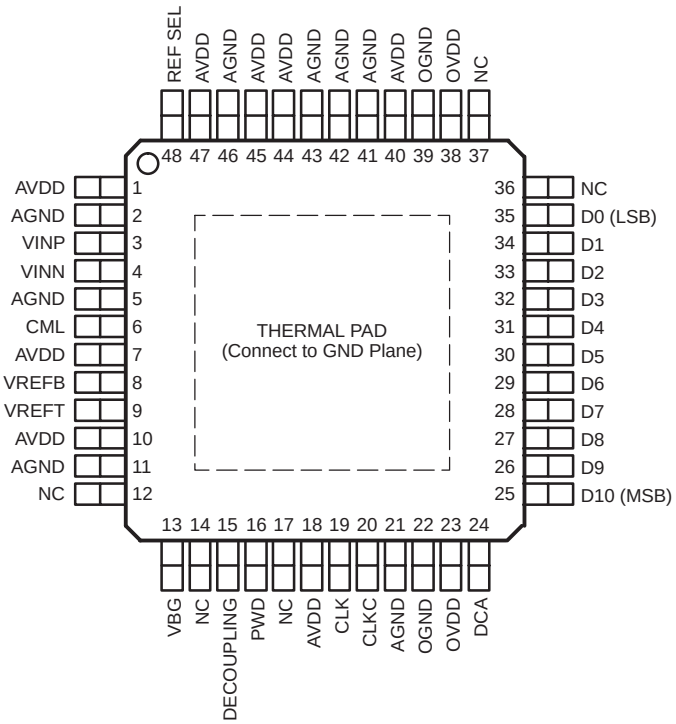


Figure 1. ADS5413−11 Timing Diagram

PIN ASSIGNMENTS

PHP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVDD	1, 7, 10, 18, 40, 44, 45, 47	I	Analog power supply
AGND	2, 5, 11, 21, 41, 42, 43, 46	I	Analog ground
CLK	19	I	Clock input
CLKC	20	I	Complementary clock input
CML	6	O	Common-mode output voltage
D10−D0	25−35	O	Digital outputs, D10 is most significant data bit, D0 is least significant data bit.
DCA	24	I	Duty cycle adjust control. High = enable, low = disable, NC = enable
DECOUPLING	15	O	Decoupling pin. Add 0.1 μF to GND
NC	12, 14, 17, 36, 37		Internally not connected
OGND	22, 39	I	Digital driver ground
OVDD	23, 38	I	Digital driver power supply
PWD	16	I	Power down. High = powered down, low = powered up, NC = powered up
REF SEL	48	I	Reference select. High = external reference, low = internal reference, NC = internal reference
VBG	13	O	Bandgap voltage output
VINN	4	I	Complementary analog input
VINP	3	I	Analog input
VREFB	8	I/O	Reference bottom
VREFT	9	I/O	Reference top

TYPICAL CHARACTERISTICS†

SPECTRAL PERFORMANCE

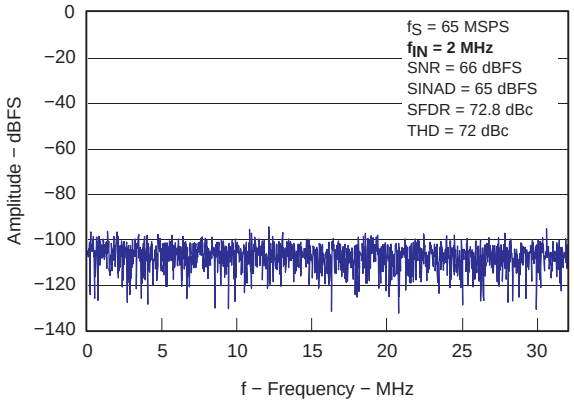


Figure 2

SPECTRAL PERFORMANCE

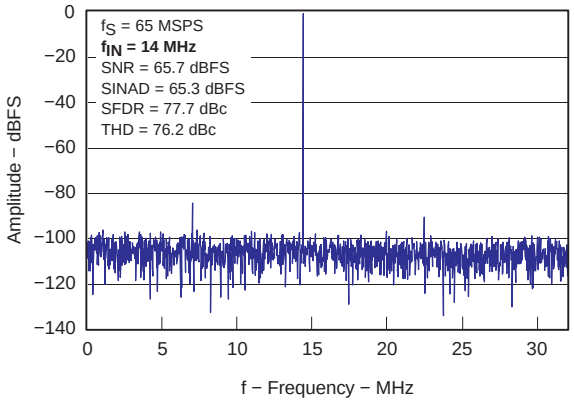


Figure 3

SPECTRAL PERFORMANCE

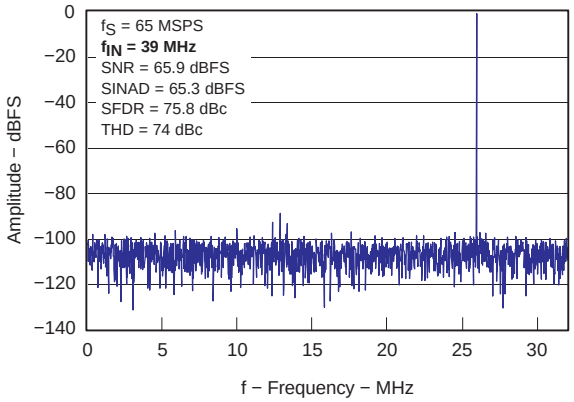


Figure 4

SPECTRAL PERFORMANCE

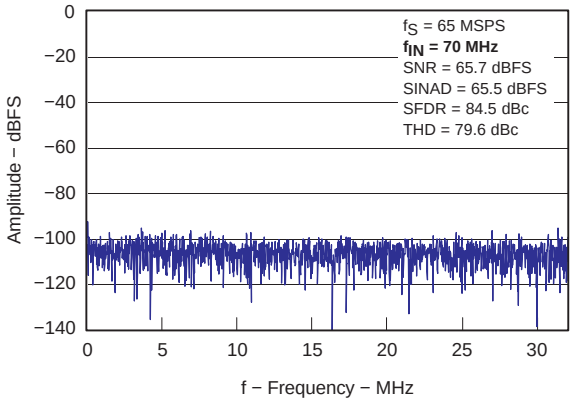


Figure 5

SPECTRAL PERFORMANCE

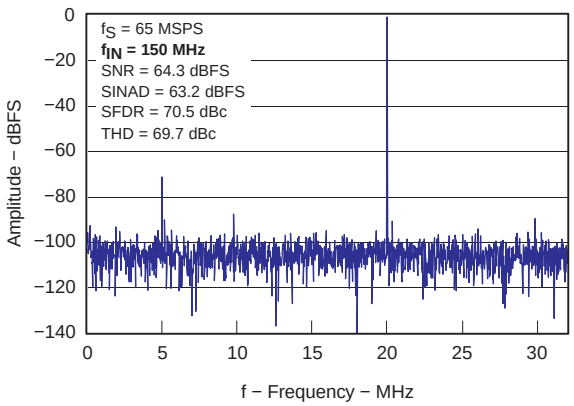


Figure 6

SPECTRAL PERFORMANCE

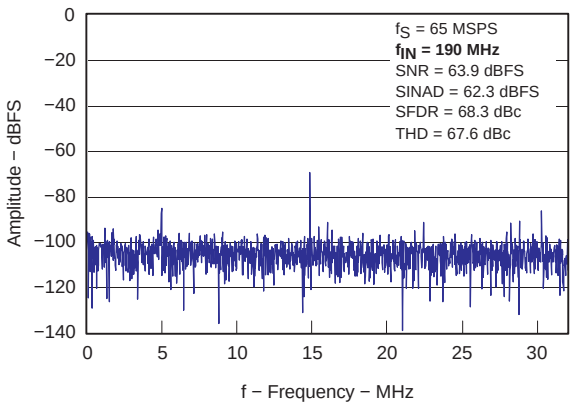


Figure 7

† 50% duty cycle. AV_{DD} = 3.3 V, OV_{DD} = 3.3 V, 25°C, DCA off, internal reference, A_{in} = –1 dBFS, CLK 2.8-V_{PP} sine wave single ended, unless otherwise noted

TYPICAL CHARACTERISTICS†

SPECTRAL PERFORMANCE

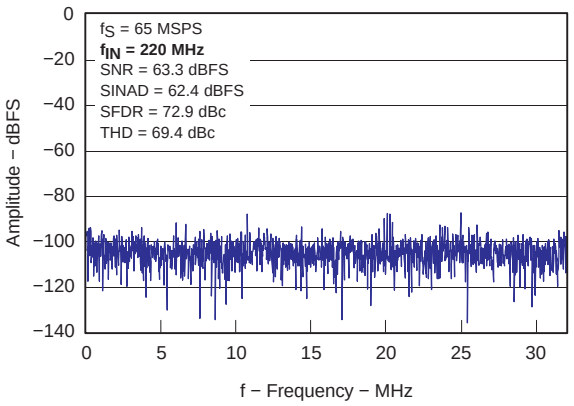


Figure 8

SPECTRAL PERFORMANCE

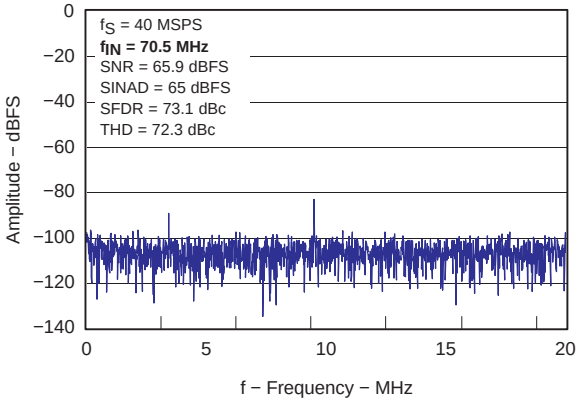


Figure 9

AC PERFORMANCE
vs
REFERENCE VOLTAGES

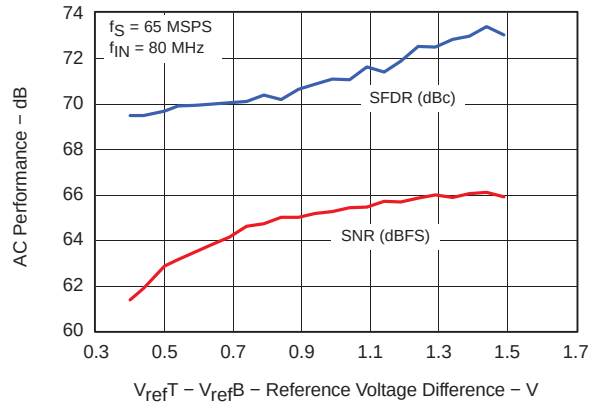


Figure 10

AC PERFORMANCE
vs
INPUT AMPLITUDE

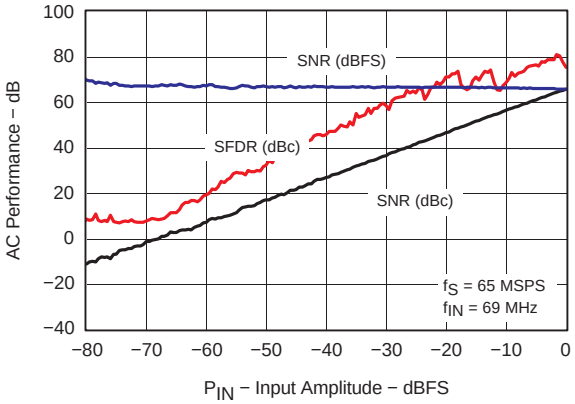


Figure 11

AC PERFORMANCE
vs
INPUT AMPLITUDE

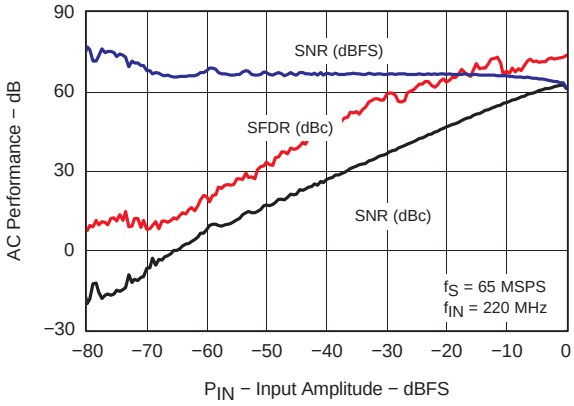


Figure 12

† 50% duty cycle. AV_{DD} = 3.3 V, OV_{DD} = 3.3 V, 25°C, DCA off, internal reference, A_{in} = –1 dBFS, CLK 2.8-V_{PP} sine wave single ended, unless otherwise noted

TYPICAL CHARACTERISTICS†

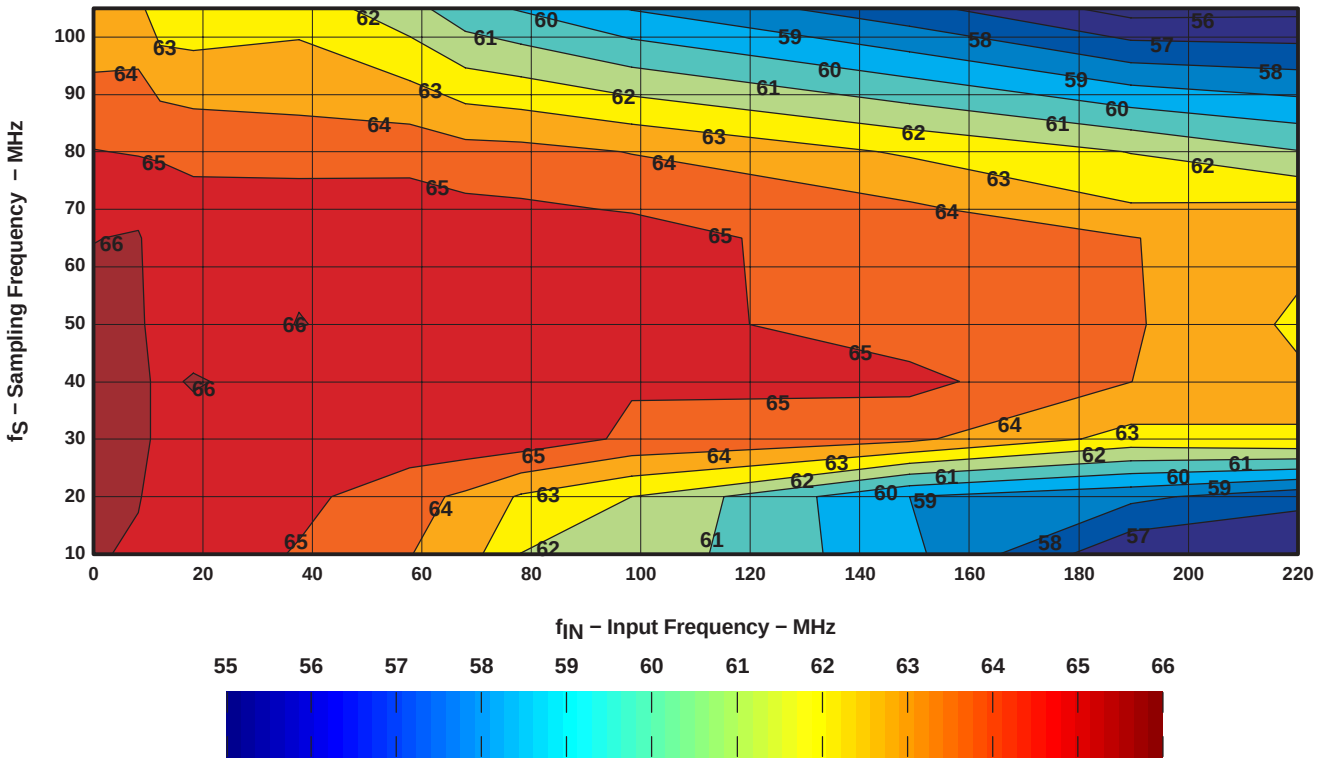


Figure 13. SNR– dBFS

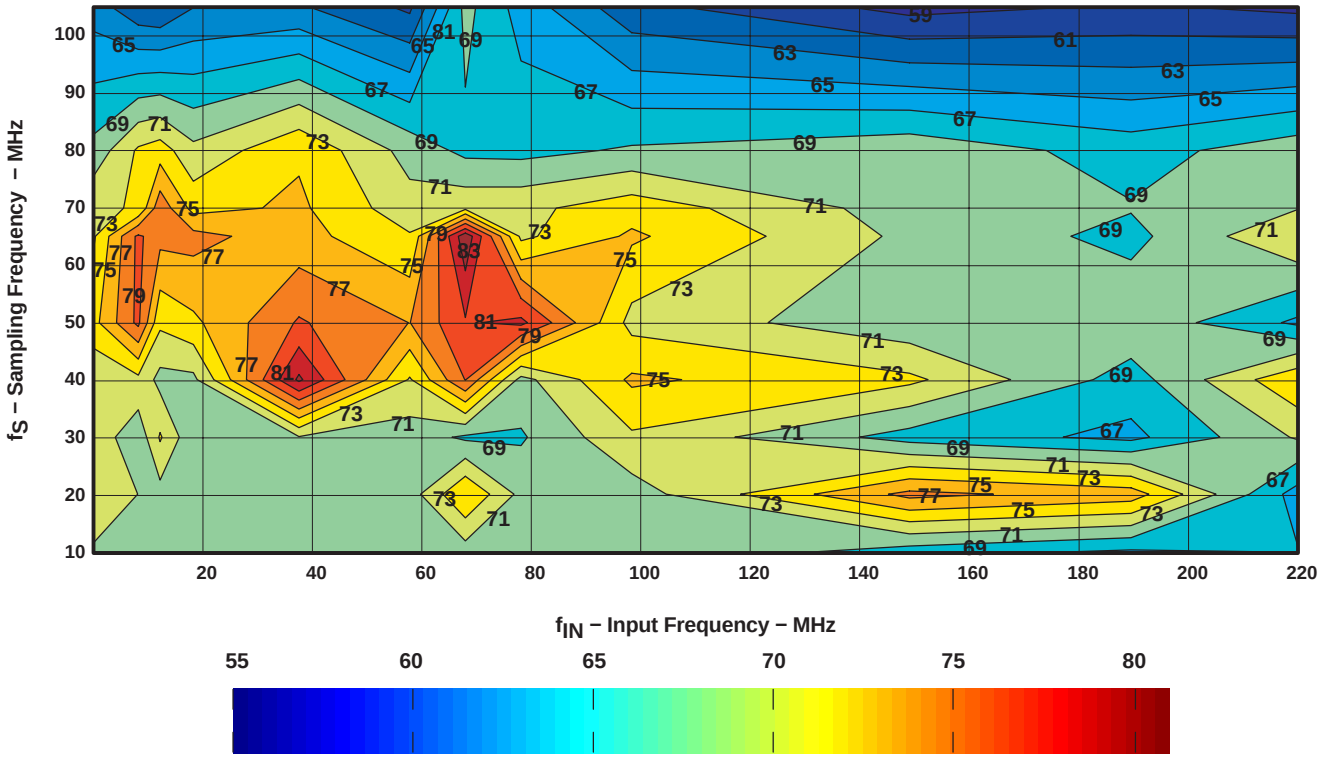
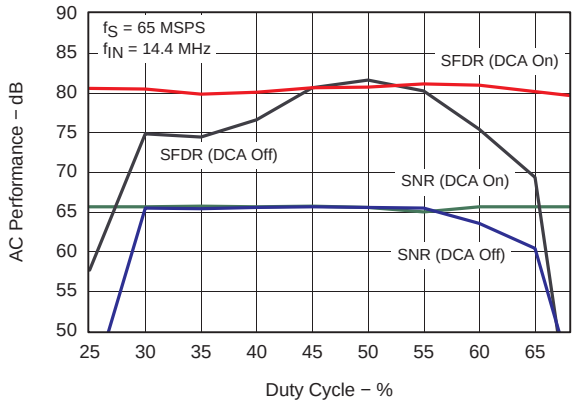


Figure 14. SFDR – dBc

† 50% duty cycle. AV_{DD} = 3.3 V, OV_{DD} = 3.3 V, 25°C, DCA off, internal reference, A_{in} = –1 dBFS, CLK 2.8-V_{PP} sine wave single ended, unless otherwise noted

TYPICAL CHARACTERISTICS†

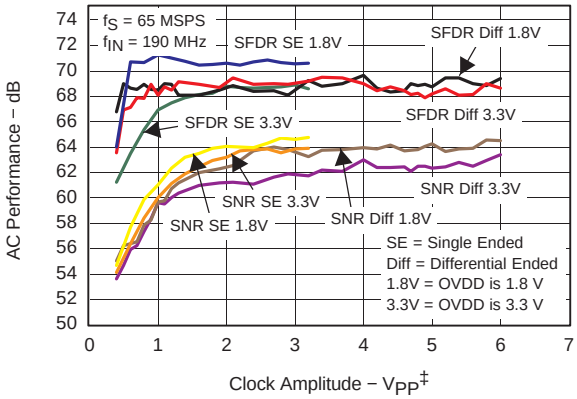
AC PERFORMANCE vs DUTY CYCLE



NOTE: CLK 1.15-V_{PP} square-wave differential

Figure 15

AC PERFORMANCE vs CLOCK AMPLITUDE



‡ Measured from CLK to CLKC

Figure 16

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

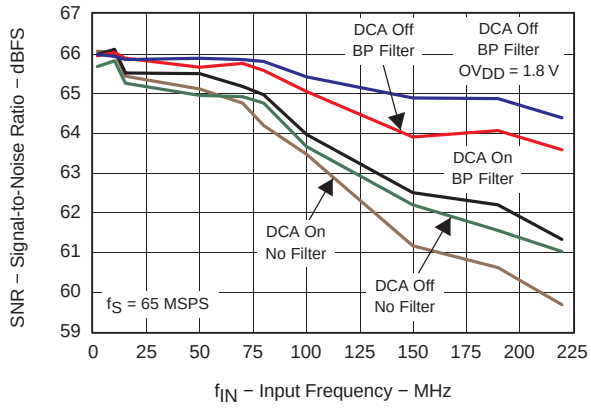


Figure 17

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

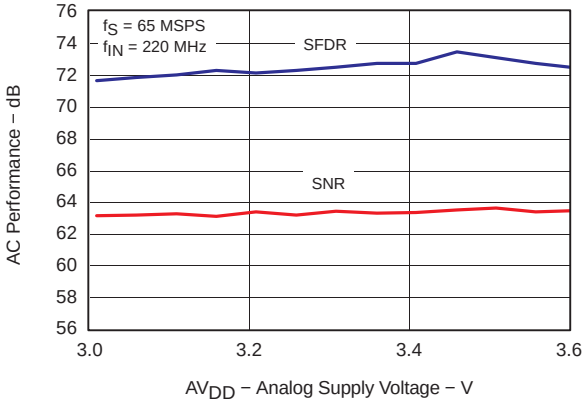


Figure 18

AC PERFORMANCE vs OUTPUT SUPPLY VOLTAGE

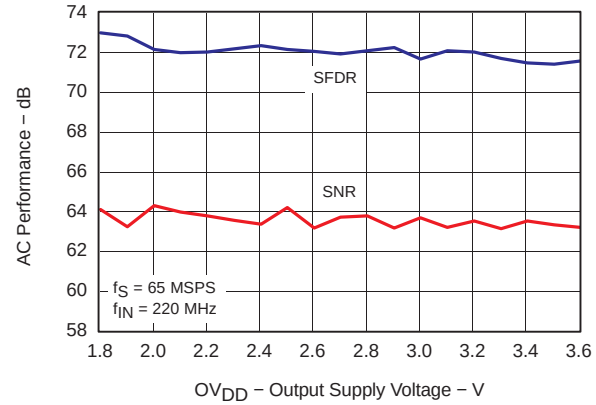


Figure 19

† 50% duty cycle. AV_{DD} = 3.3 V, OV_{DD} = 3.3 V, 25°C, DCA off, internal reference, A_{in} = –1 dBFS, CLK 2.8-V_{PP} sine wave single ended, unless otherwise noted

TYPICAL CHARACTERISTICS†

DIFFERENTIAL NONLINEARITY

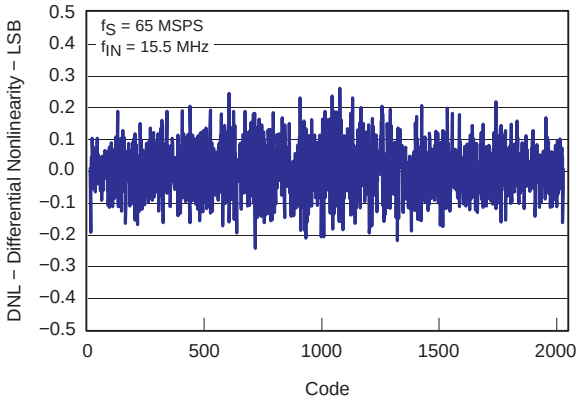


Figure 20

INTEGRAL NONLINEARITY

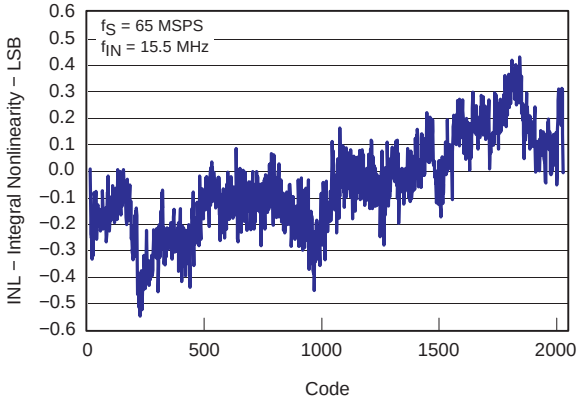


Figure 21

AC PERFORMANCE vs FREE-AIR TEMPERATURE

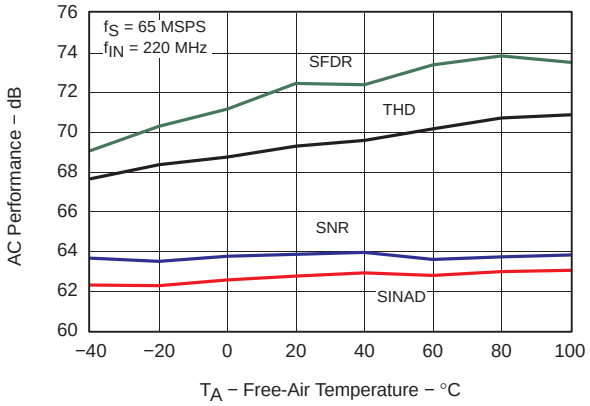
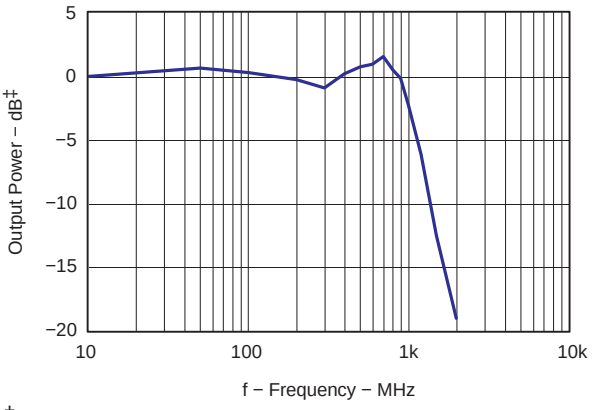


Figure 22

INPUT BANDWIDTH



‡ dB with respect to −3 dBFS

Figure 23

† 50% duty cycle. AV_{DD} = 3.3 V, OV_{DD} = 3.3 V, 25°C, DCA off, internal reference, A_{in} = –1 dBFS, CLK 2.8-V_{PP} sine wave single ended, unless otherwise noted

EQUIVALENT CIRCUITS

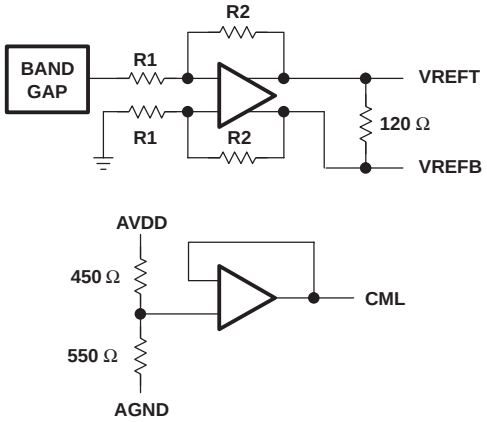


Figure 24. References

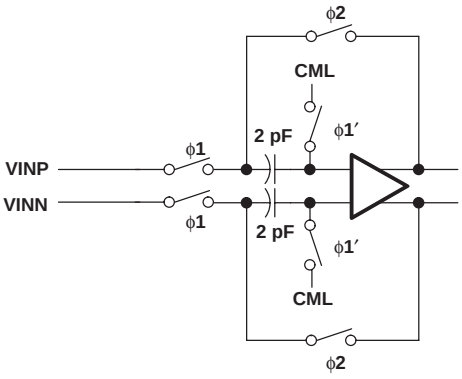


Figure 25. Analog Input Stage

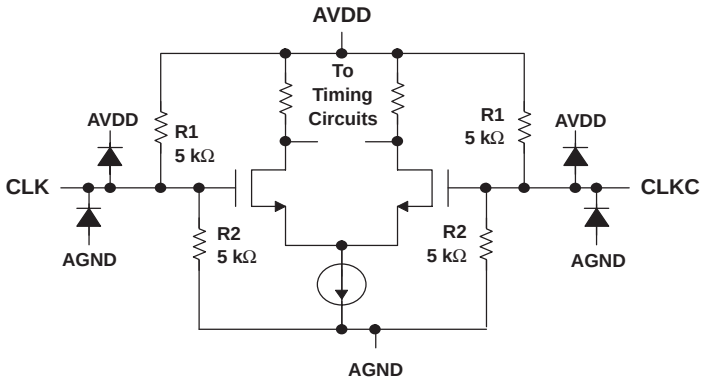


Figure 26. Clock Inputs

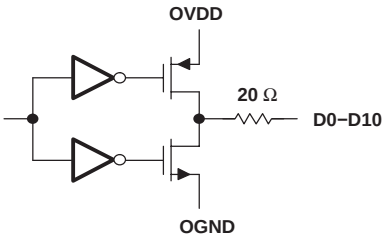


Figure 27. Digital Outputs

APPLICATION INFORMATION

CONVERTER OPERATION

The ADS5413−11 is a 11-bit pipeline ADC. Its low power (400 mW) at 65 MSPS and high sampling rate is achieved using a state-of-the-art switched capacitor pipeline architecture built on an advanced low-voltage CMOS process. The ADS5413−11 analog core operates from a 3.3 V supply consuming most of the power. For additional interfacing flexibility, the digital output supply (OVDD) can be set from 1.6 V to 3.6 V. The ADC core consists of 10 pipeline stages and one flash ADC. Each of the stages produces 1.5 bits per stage. Both the rising and the falling clock edges are utilized to propagate the sample through the pipeline every half clock, for a total of six clock cycles.

ANALOG INPUTS

The analog input for the ADS5413−11 consists of a differential track-and-hold amplifier implemented using a switched capacitor technique, shown in Figure 25. This differential input topology, along with closely matched capacitors, produces a high level of ac-performance up to high sampling and input frequencies.

The ADS5413−11 requires each of the analog inputs (VINP and VINM) to be externally biased around the common mode level of the internal circuitry (CML, pin 6).

For a full-scale differential input, each of the differential lines of the input signal (pins 3 and 4) swings symmetrically between CML+(Vreft+Vrefb)/2 and CML−(Vreft+Vrefb)/2. The maximum swing is determined by the difference between the two reference voltages, the top reference (REFT), and the bottom reference (REFB). The total differential full-scale input swing is 2(Vreft − Vrefb). See the reference circuit section for possible adjustments of the input full scale.

Although the inputs can be driven in single-ended configuration, the ADS5413−11 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 28 shows one possible configuration. The single-ended signal is fed to the primary of an RF transformer. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode (CML) reference from the ADS5413−11 is connected to the center-tap of the secondary. To ensure a steady low noise CML reference, the best performance is obtained when the CML output is connected to ground with a 0.1-µF and 0.01-µF low inductance capacitor.

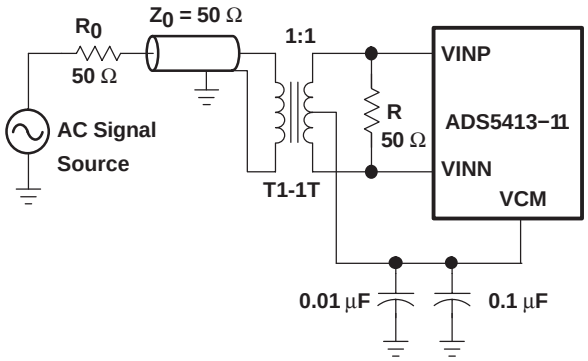


Figure 28. Driving the ADS5413−11 Analog Input With Impedance Matched Transmission Line

If it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine a single-ended amplifier with an RF transformer as shown in Figure 29. Texas Instruments offers a wide selection of operational amplifiers, as the THS3001/2, the OPA847, or the OPA695 that can be selected depending on the application. R_{IN} and C_{IN} can be placed to isolate the source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. Although not needed, it is recommended to lay out the circuit with placement for those three components, which allows fine tune of the prototype if necessary. Nevertheless, any mismatch between the differential lines of the input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even harmonics. In this case, special care should be taken keeping as much electrical symmetry as possible between both inputs. This includes shorting R_{IN} and leaving C_{IN} unpopulated.

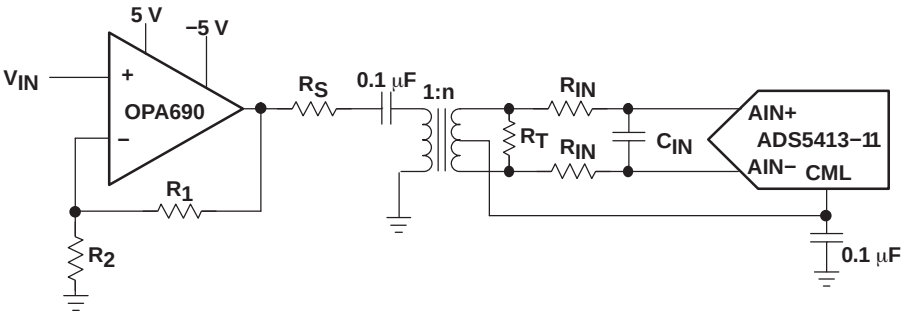


Figure 29. Converting a Single-Ended Input Signal Into a Differential Signal Using an RF Transformer

Another possibility is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring input dc coupling. Flexible in their configurations (see Figure 30), such amplifiers can be used for single ended to differential conversion, for signal amplification, and for filtering prior to the ADC.

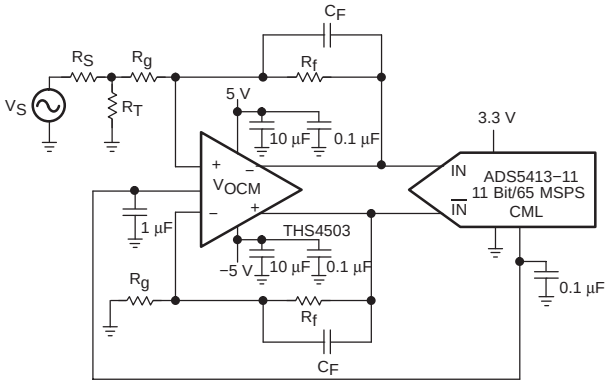


Figure 30. Using the THS4503 With the ADS5413−11

REFERENCE CIRCUIT

The ADS5413−11 has its own internal reference generation saving external circuitry in the design. For optimum performance, it is best to connect both VREFB and VREFT to ground with a 1-µF and a 0.1-µF decoupling capacitor in parallel and a 0.1-µF capacitor between both pins (see Figure 31). The series inductance with these capacitors should be minimized as much as possible. For that we recommend to follow the layout of the EVM. In particular, the 0.1-µF capacitors should be placed on the same side of the printed circuit board as the ADS5413−11, and as close as possible to the pins 8, 9, and 11. The band-gap voltage output is not a voltage source to be used external to the ADS5413−11. However, it should be decoupled to ground with a 1-µF and a 0.01-µF capacitor in parallel.

For even more design flexibility, the internal reference can be disabled using the pin 48. By default, this pin is internally connected with a 70-kΩ pulldown resistor to ground, which enables the internal reference circuit. Tying this pin to AVDD powers down the internal reference generator, allowing the user to provide external voltages for VREFT (pin 9) and VREFB (pin 8). In addition to the power consumption reduction (typically 56 mW) which is now transferred to the external circuitry, it also allows for a precise setting of the input range. To further remove any variation with external factors, such as temperature or supply voltage, the user has direct access to the internal resistor divider, without any intermediate buffering. The equivalent circuit for the reference input pins is shown in Figure 24. The core of the ADC is designed for a 1 V difference between the reference pins. Nevertheless, the user can use these pins to set a different input range. Figure 10 shows the variation on SNR and SFDR for a sampling rate of 65 MHz and a single-tone input of 80 MHz at −1 dBFS for different VREFT−VREFB voltage settings.

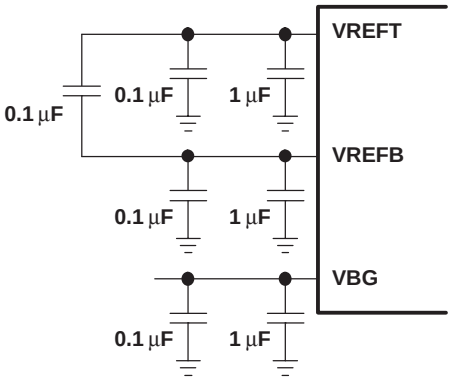


Figure 31. Internal Reference Usage

CLOCK INPUTS

The ADS5413−11 clock input can be driven with either a differential clock signal or a single ended clock input with little or no difference in performance between the single-ended and differential-input configurations (see Figure 16). The common mode of the clock inputs is set internally to AVDD/2 using 5-kΩ resistors (see Figure 26).

When driven with a single-ended clock input, it is best to connect the CLKC input to ground with a 0.01-µF capacitor (see Figure 32), while CLK is ac-coupled with 0.01 µF to the clock source.

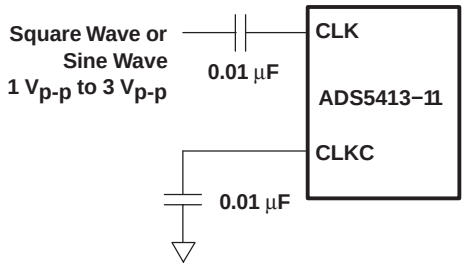


Figure 32. AC-Coupled Single-Ended Clock Input

The ADS5413−11 clock input can also be driven differentially. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-µF capacitors (see Figure 33). The differential input swing can vary between 1 V and 6 V with little or no performance degradation (see Figure 16).

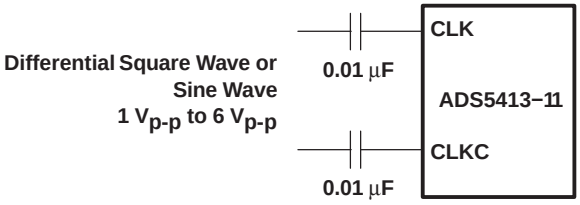


Figure 33. AC-Coupled Differential Clock Input

The ADS5413−11 can be driven either with a sine wave or a square wave. The internal ADC core uses both edges of the clock for the conversion process. This means that ideally, a 50% duty cycle should be provided. Nevertheless, the ADC includes an on-board duty cycle adjuster (DCA) that adjusts the incoming clock duty cycle which may not be 50%, to a 50% duty cycle for the internal use. By default, this circuit is enabled internally (with a pull-up resistor of 70 kΩ), which relaxes the design specifications of the external clock. Nevertheless, there are some situations where the user may prefer to disable the DCA. For asynchronous clocking, i.e., when the sampling period is purposely not constant, this circuit should be disabled. Another situation is the case of high input frequency sampling. For high input frequencies, a low jitter clock should be provided. On that sense, we recommend to band-pass filter the source which, consequently, provides a sinusoidal clock with 50% duty cycle. The use of the DCA on that case would not be beneficial and adds noise to the internal clock, increasing the jitter and degrading the performance. Figure 17 shows the performance versus input frequency for the different clocking schemes. Finally, adding the DCA introduces delay between the input clock and the output data and what is more important, slightly bigger variation of this delay versus external conditions, such as temperature. To disable the DCA, user should connect it to ground.

POWER DOWN

When power down (pin 16) is tied to AVDD, the device reduces its power consumption to a typical value of 23 mW. Connecting this pin to AGND or leaving it not connected (an internal 70-kΩ pulldown resistor is provided) enables the device operation.

DIGITAL OUTPUTS

The ADS5413−11 output format is 2s complement. The voltage level of the outputs can be adjusted by setting the OVDD voltage between 1.6 V and 3.6 V, allowing for direct interface to several digital families. For better performance, customers should select the smaller output swing required in the application. To improve the performance, mainly on the higher output voltage swing configurations, the addition of a series resistor at the outputs, limiting peak currents, is recommended. The maximum value of this resistor is limited by the maximum data rate of the application. Values between 0 Ω and 200 Ω are usual. Also, limiting the length of the external traces is a good practice.

All the data sheet plots have been obtained in the worst case situation, where OVDD is 3.3 V. The external series resistors were 150 Ω and the load was a 74AVC16244 buffer, as the one used in the evaluation board. In this configuration, the rising edge of the ADC output is 5 ns, which allows for a window to capture the data of 10.4 ns (without including other factors).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog bandwidth is the analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB in respect to the value measured at low input frequencies.

Aperture Delay

The delay between the 50% point of the rising edge of the CLK command and the instant at which the analog input is sampled.

Aperture Uncertainity (Jitter)

The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The average deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a *best straight line* determined by a least square curve fit.

Clock Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the CLK pulse should be left in logic 1 state to achieve rated performance; pulse width low is the minimum time CLK pulse should be left in low state. At a given clock rate, these specifications define acceptable clock duty cycles.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic and it is reported in dBc.

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product reported in dBc.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5413-11IPHP	OBSOLETE	HTQFP	PHP	48		TBD	Call TI	Call TI	-40 to 85		
ADS5413-11IPHPG4	OBSOLETE	HTQFP	PHP	48		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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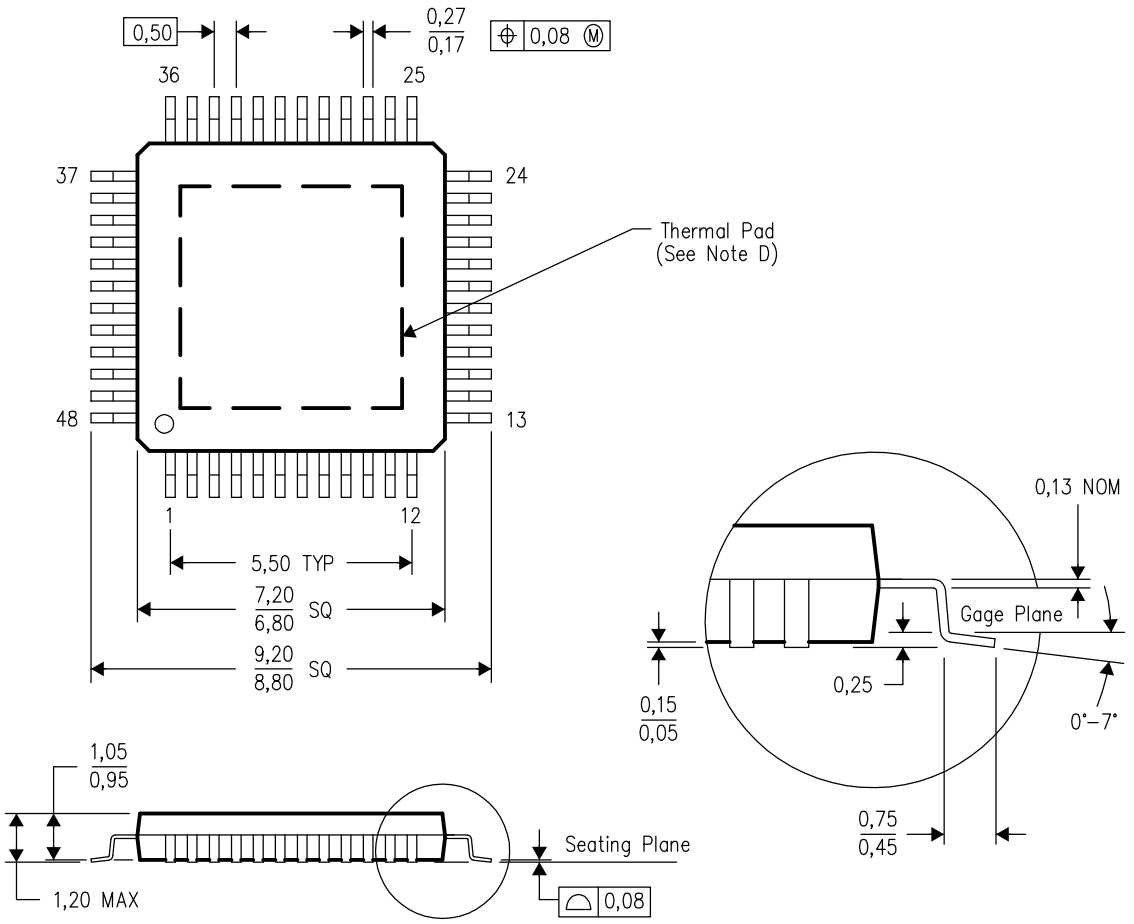

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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