12-Bit Rail-to-Rail Micropower DAC in MSOP Package

FEATURES

- **Buffered True Rail-to-Rail Voltage Output**
- **Maximum DNL Error: 0.5LSB**
- 12-Bit Resolution
- Supply Operation: 3V to 5V
- Output Swings from 0V to V_{REF}
- V_{REF} Can Tie to V_{CC}
- Schmitt Trigger On Clock Input Allows Direct Optocoupler Interface
- Power-On Reset Clears DAC to 0V
- 3-Wire Cascadable Serial Interface
- Low Cost
- 8-Lead SO and MSOP Packages

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1659 is a single supply, rail-to-rail voltage output, 12-bit digital-to-analog converter (DAC) in an MSOP package. It includes a rail-to-rail output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1659 output swings from 0V to REF. The REF input can be tied to V_{CC} which can range from 2.7V to 5.5V. This allows a rail-to-rail output swing from 0V to V_{CC}. The LTC1659 draws only 250µA from a 5V supply.

Its guaranteed ±0.5LSB maximum DNL makes the LTC1659 excel in calibration, control and trim/adjust applications. The low power supply current and the small MSOP package make the LTC1659 ideal for battery-powered applications.

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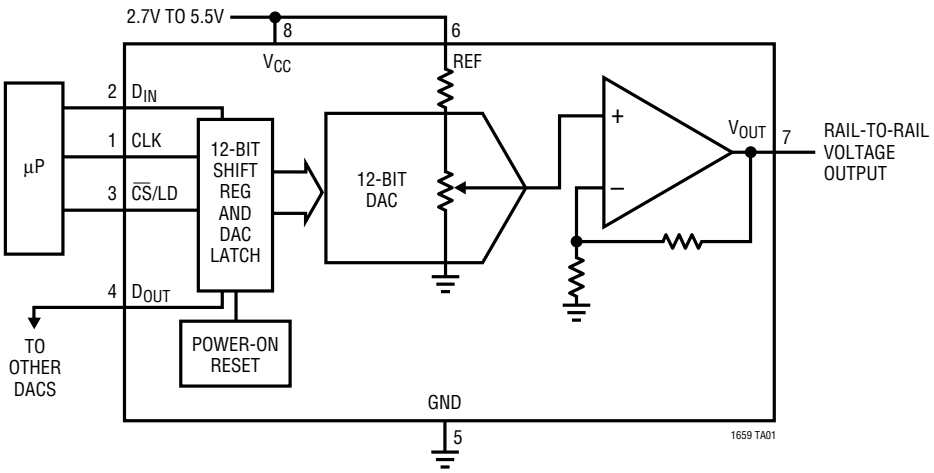
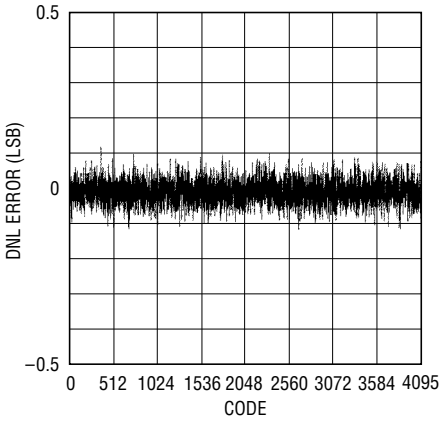
TYPICAL APPLICATION

Functional Block Diagram: 12-Bit Rail-to-Rail DAC



Differential Nonlinearity vs Input Code

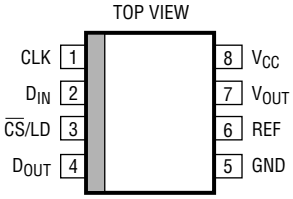


ABSOLUTE MAXIMUM RATINGS (Note 1)

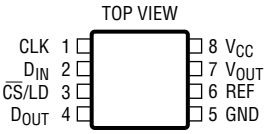
V_{CC} to GND ..... –0.5V to 7.5V
Logic Inputs to GND ..... –0.5V to 7.5V
V_{OUT} ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1659CS8 ..... 0°C to 70°C
LTC1659IS8 ..... –40°C to 85°C
LTC1659CMS8 ..... 0°C to 70°C
LTC1659IMS8 ..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 160°C/W



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 140°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1659CS8#PBF	LTC1659CS8#TRPBF	1659	8-Lead Plastic SO	0°C to 70°C
LTC1659IS8#PBF	LTC1659IS8#TRPBF	1659I	8-Lead Plastic SO	–40°C to 85°C
LTC1659CMS8#PBF	LTC1659CMS8#TRPBF	LTCK	8-Lead Plastic MSOP	0°C to 70°C
LTC1659IMS8#PBF	LTC1659IMS8#TRPBF	LTCK	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
	Monotonicity		●	12			Bits
DNL	Differential Nonlinearity	V_{REF} ≤ V_{CC} – 0.1V (Note 2)	●			±0.5	LSB
INL	Integral Nonlinearity	V_{REF} ≤ V_{CC} – 0.1V (Note 2)	 ●			±5.0 ±5.5	LSB LSB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Offset Error	Measured at Code 20	 ●			±12 ±18	mV mV
V_{OS} TC	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	REF = 4.096V	 ●	4.070 4.060	4.095 4.095	4.120 4.130	V V
V_{FS} TC	Full-Scale Voltage Temperature Coefficient				10		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	(Note 5)	●		240	450	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		70	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		65	120	mA
	Output Impedance to GND	Input Code = 0	●		40	150	Ω
	Output Line Regulation	Input Code = 4095, V_{CC} = 4.5V to 5.5V			0.1	1.5	LSB/V
AC Performance							
	Voltage Output Slew Rate	(Note 3)	●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 3, 4) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV • s
Reference Input							
R_{IN}	REF Input Resistance		●	17	28	40	kΩ
REF	REF Input Range	(Notes 6, 7)	●	0		V_{CC}	V
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 5V	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 5V	●			0.8	V
V_{OH}	Digital Output High Voltage	V_{CC} = 5V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 1.0			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 5V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
V_{IH}	Digital Input High Voltage	V_{CC} = 3V	●	2.0			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V	●			0.6	V
V_{OH}	Digital Output High Voltage	V_{CC} = 3V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 3V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 7)	●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded, REF ≤ V_{CC}, T_A = T_{MIN} to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching (V_{CC} = 4.5V to 5.5V							
t_1	D_{IN} Valid to CLK Setup		●	40			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 7)	●	40			ns
t_4	CLK Low Time	(Note 7)	●	40			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 7)	●	50			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 7)	●	40			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 7)	●	20			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●	5		150	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 7)	●	20			ns
Switching (V_{CC} = 2.7V to 5.5V)							
t_1	D_{IN} Valid to CLK Setup		●	60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High Time	(Note 7)	●	60			ns
t_4	CLK Low Time	(Note 7)	●	60			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 7)	●	80			ns
t_6	LSB CLK to $\overline{CS}$/LD	(Note 7)	●	60			ns
t_7	$\overline{CS}$/LD Low to CLK	(Note 7)	●	30			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●	10		220	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 7)	●	30			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Nonlinearity is defined from code 20 to code 4095 (full scale). See Applications Information.

Note 3: Load is 5kΩ in parallel with 100pF.

Note 4: DAC switched between all 1s and the code corresponding to V_{OS} for the part.

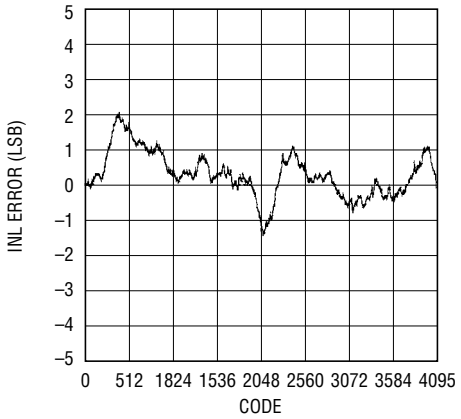
Note 5: Digital inputs at 0V or V_{CC}.

Note 6: V_{OUT} can only swing from (GND + $|V_{OS}|$) to (V_{CC} – $|V_{OS}|$) when output is unloaded.

Note 7: Guaranteed by design, not subject to test.

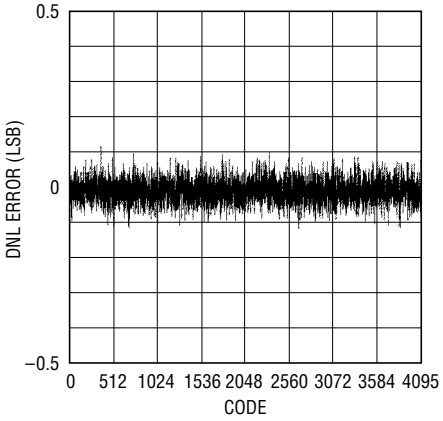
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (INL)



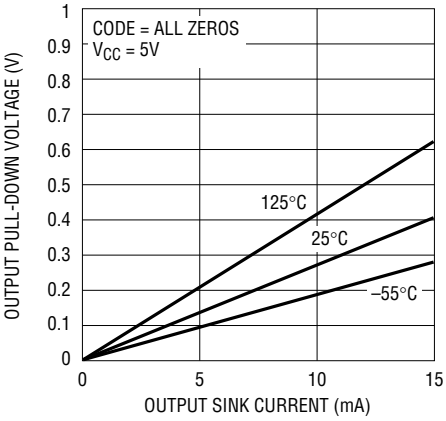
1659 • G01

Differential Nonlinearity (DNL)



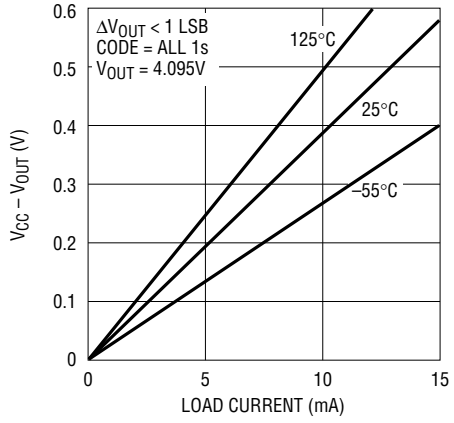
1659 • G02

Minimum Output Voltage vs Output Sink Current



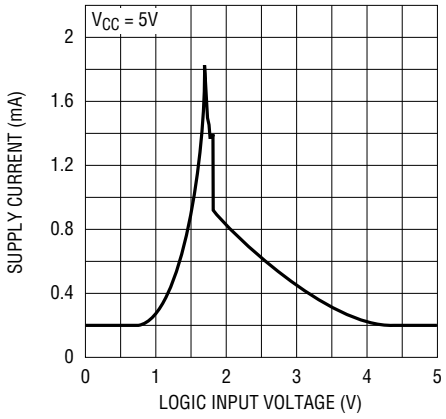
1659 • G03

Supply Headroom for Full Output Swing vs Load Current



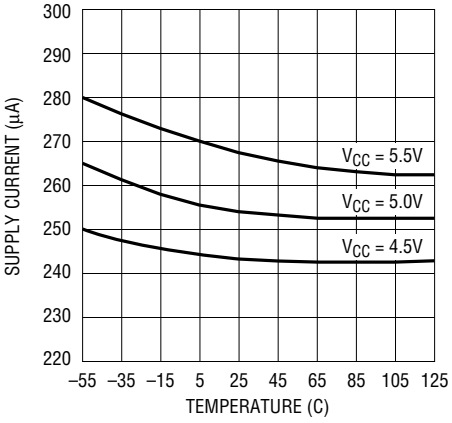
1659 • G04

Supply Current vs Logic Input Voltage



1659 • G05

Supply Current vs Temperature



1659 • G06

PIN FUNCTIONS

CLK (Pin 1): Serial Interface Clock. Internal Schmitt trigger on this input allows direct optocoupler interface.

D_{IN} (Pin 2): Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{CS}$/LD (Pin 3): Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output and the CLK is disabled internally.

D_{OUT} (Pin 4): Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

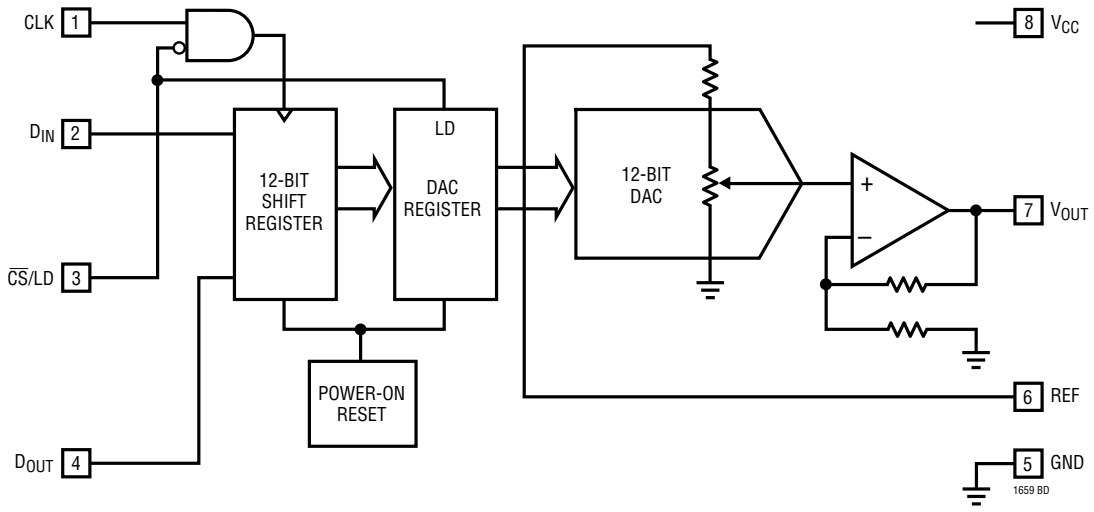
GND (Pin 5): Ground.

REF (Pin 6): Reference Input. This pin can be tied to V_{CC}. The output will swing from 0V to REF. The typical input resistance is 28k.

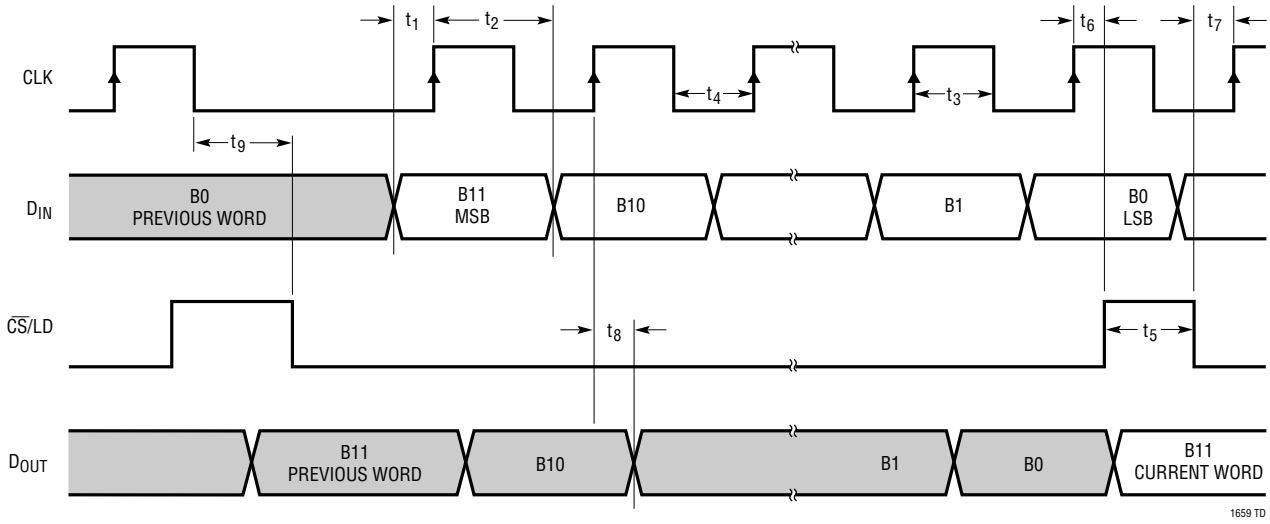
V_{OUT} (Pin 7): Buffered DAC Output.

V_{CC} (Pin 8): Positive Supply Input. 2.7V ≤ V_{CC} ≤ 5.5V. Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAM



DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

$$LSB = V_{REF}/4096$$

Resolution (n): Defines the number of DAC output states (2n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}. Multiple LTC1659s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Voltage Output

The LTC1659's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

The output swings from 0V to the voltage at the REF pin, i.e., there is a gain of 1 from the REF to V_{OUT}. Please note if REF is tied to V_{CC} the output can only swing to (V_{CC} – V_{OS}). See Applications Information.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown is Figure 1c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

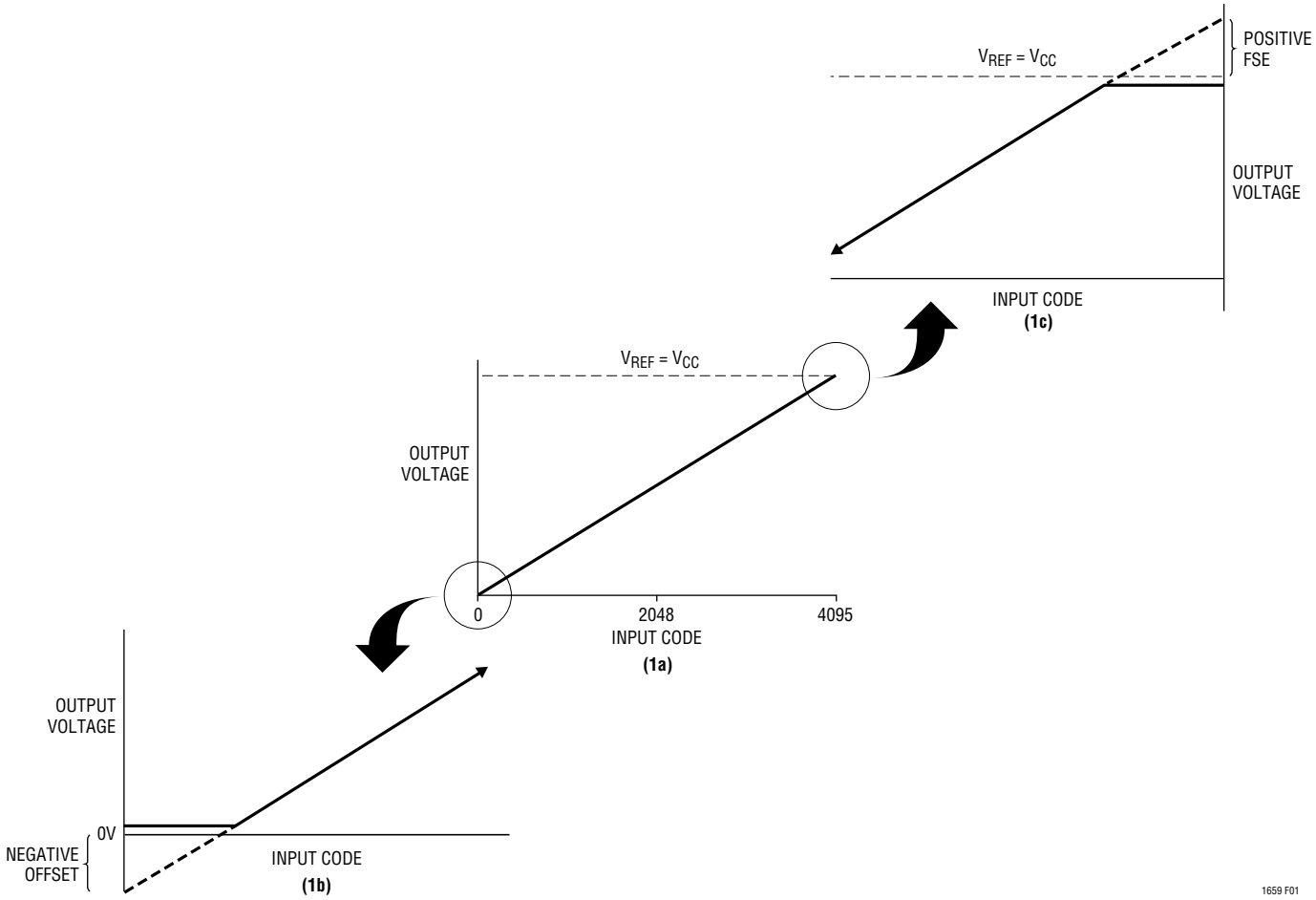
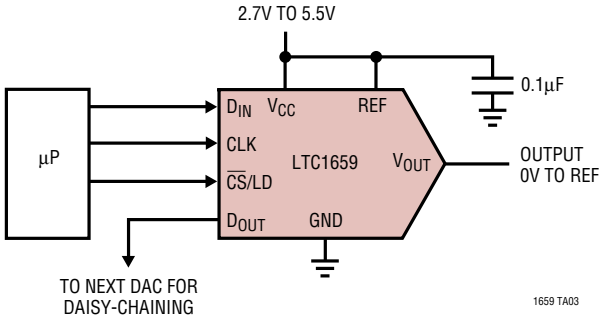


Figure 1. Effects of Rail-to-Rail Operation on a DAC Transfer Curve
(1a) Overall Transfer Function
(1b) Effect of Negative Offset for Codes Near Zero Scale
(1c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

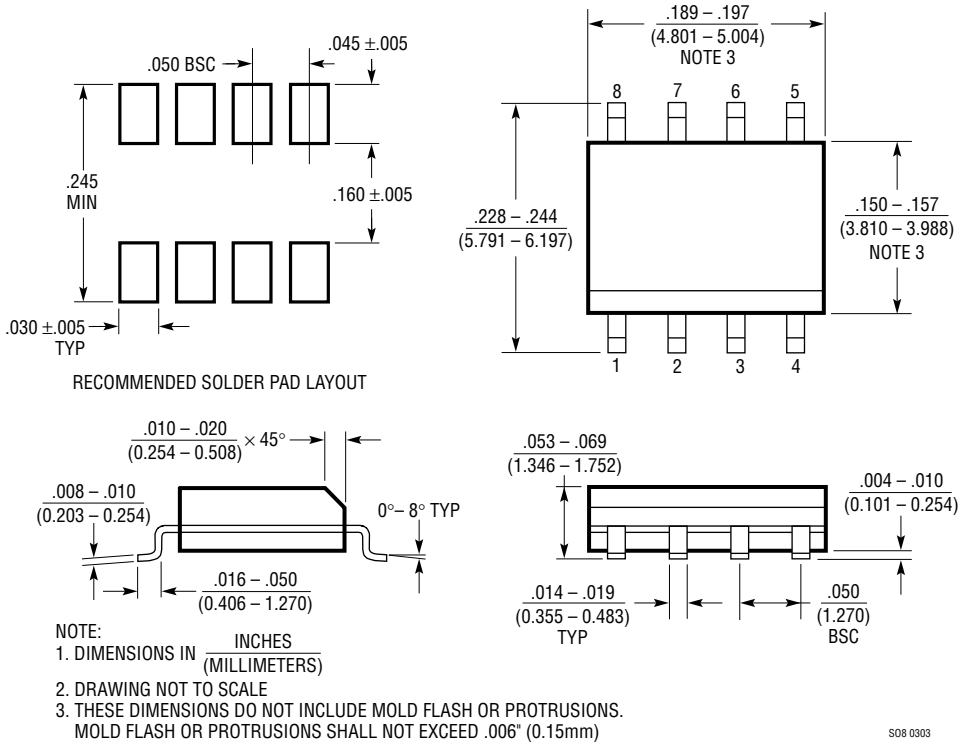
TYPICAL APPLICATION

12-Bit, 3V to 5V Single Supply, Rail-to-Rail Voltage Output DAC



PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

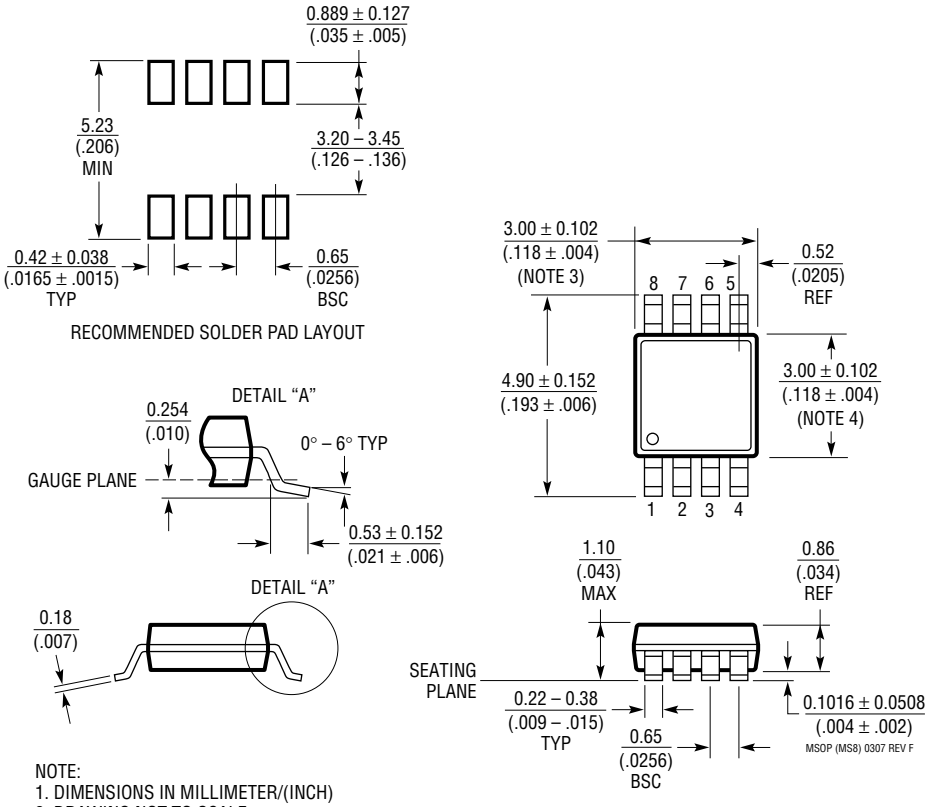


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

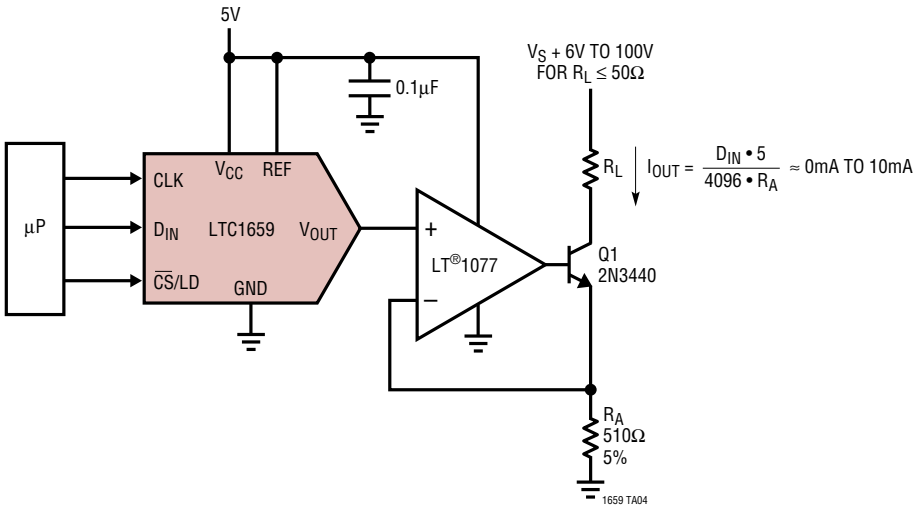


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Digitally Programmable Current Source



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC, V_{CC}: 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1450/LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	5V, Low Power Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V

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