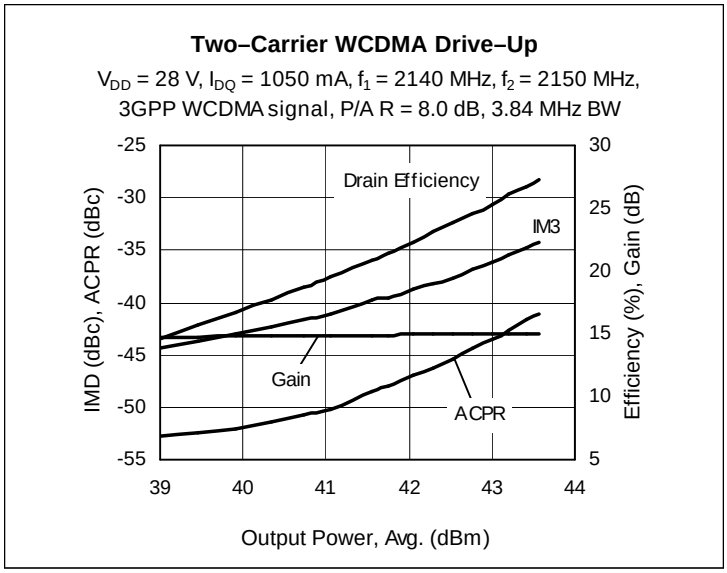
LDMOS RF Power Field Effect Transistor
90 W, 2110–2170 MHz

Description

The PTF210901 is an internally matched 90 W *GOLDMOS* FET intended for WCDMA applications from 2110 to 2170 MHz. Full gold metallization ensures excellent device lifetime and reliability.



Features

- Internal matching for wideband performance
- Typical two–carrier 3GPP WCDMA performance
  - Average output power = 19 W at –37 dBc
  - Efficiency = 25%
- Typical CW performance
  - Output power at P–1dB = 105 W
  - Gain = 15 dB
  - Efficiency = 53%
- Integrated ESD protection: Human Body Model, Class 1 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR at 28 V, 90 W (CW) output power



PTF210901E
Package 30248

ESD: Electrostatic discharge sensitive device — observe handling precautions!

RF Performance at T_{CASE} = 25°C unless otherwise indicated

WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 1050 mA, P_{OUT} = 19 W AVG
f_1 = 2140 MHz, f_2 = 2150 MHz, 3GPP signal, channel bandwidth 3.84 MHz, 8.0 dB peak/average @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Units
Intermodulation Distortion	IMD	—	–37	—	dBc
Gain	G_{ps}	—	15	—	dB
Drain Efficiency	η_D	—	25	—	%

Two–Tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 1050 mA, P_{OUT} = 90 W PEP, f = 2170 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Units
Gain	G_{ps}	13.5	15	—	dB
Drain Efficiency	η_D	36	38	—	%
Intermodulation Distortion	IMD	—	–30	–28	dBc

Electrical Characteristics at T_{CASE} = 25°C unless otherwise indicated

Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On–State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.1	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 1050 mA	V_{GS}	2.5	3.2	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	0.01	1.0	µA

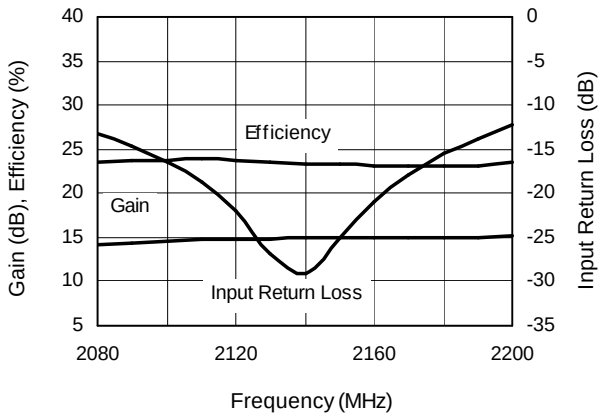
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	V
Gate–Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	389	W
Above 25°C derate by		2.22	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 90 W CW)	$R_{\theta JC}$	0.45	°C/W

Typical Performance in broadband test fixture

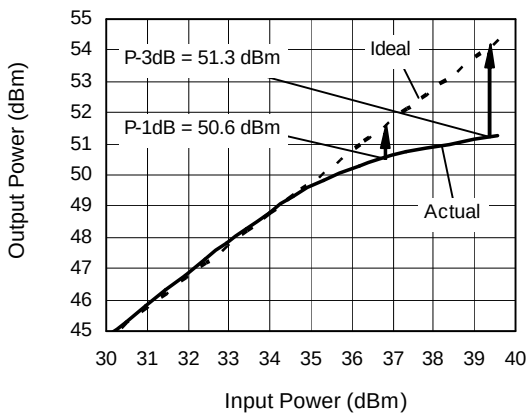
Broadband Circuit Performance

V_{DD} = 28 V, I_{DQ} = 1050 mA, P_{OUT} = 20 W CW



Power Sweep, Pulsed Conditions

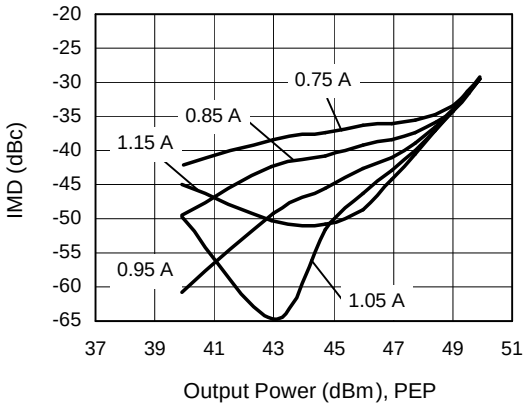
V_{DD} = 28 V, I_{DQ} = 1050 mA, f = 2140 MHz,
pulse period = 1 ms, 0.8% duty cycle



Typical Performance (cont.)

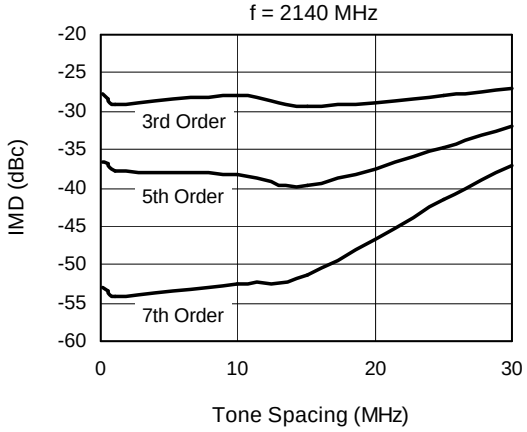
Intermodulation Distortion vs. Output Power for selected currents

V_{DD} = 28 V, f = 2140 MHz, tone spacing = 1 MHz



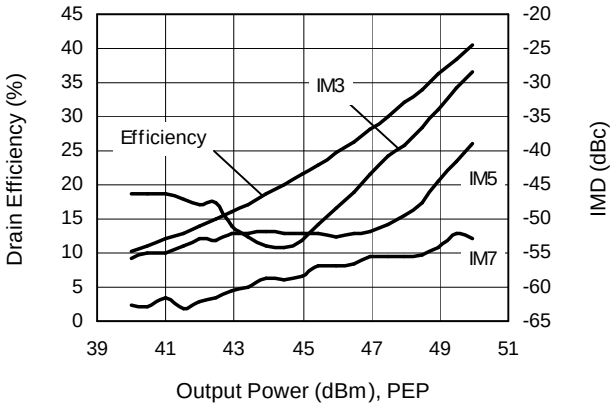
Intermodulation Distortion Products vs. Tone Spacing

V_{DD} = 28 V, I_{DQ} = 1050 mA, P_{OUT} = 90 W PEP, f = 2140 MHz



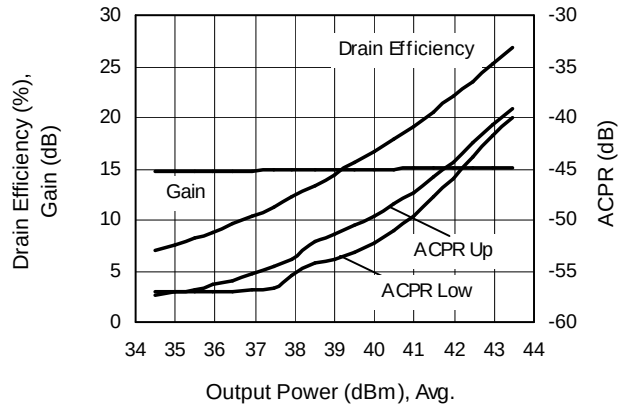
Two–Tone Drive–Up

V_{DD} = 28 V, I_{DQ} = 1050 mA, f = 2140 MHz, tone spacing = 1 MHz

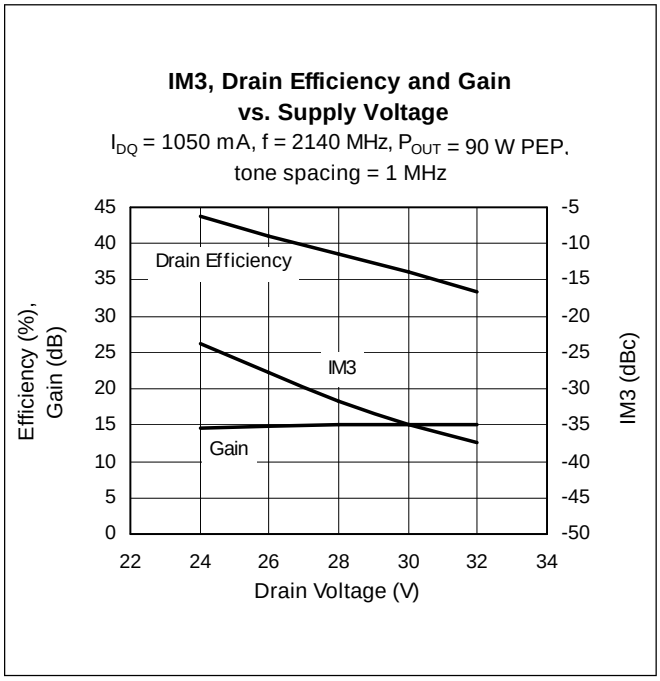


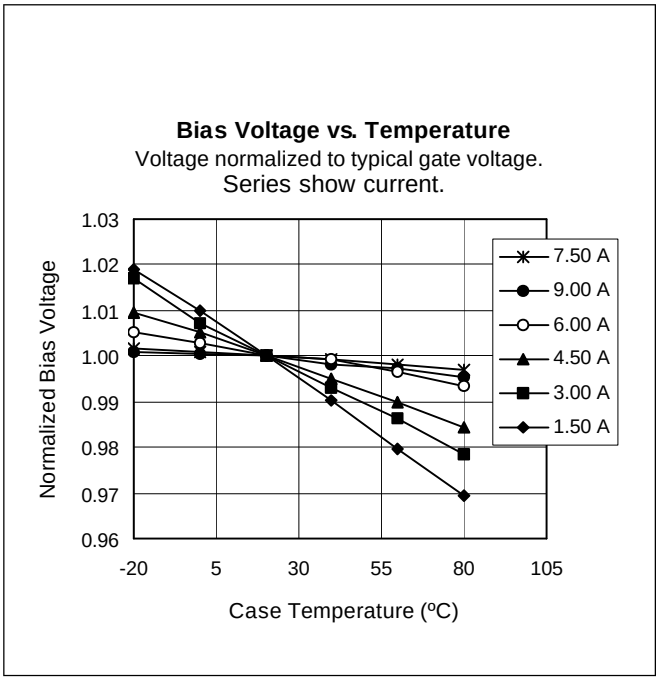
Single–Carrier WCDMA Drive–Up

V_{DD} = 28 V, I_{DQ} = 1050 mA, f = 2140 MHz, 3GPP WCDMA signal, Test Model 1 w/ 16 DPCH 67% clipping, P/A R = 8.7 dB, 3.84 MHz BW

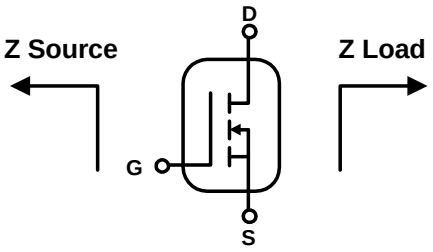


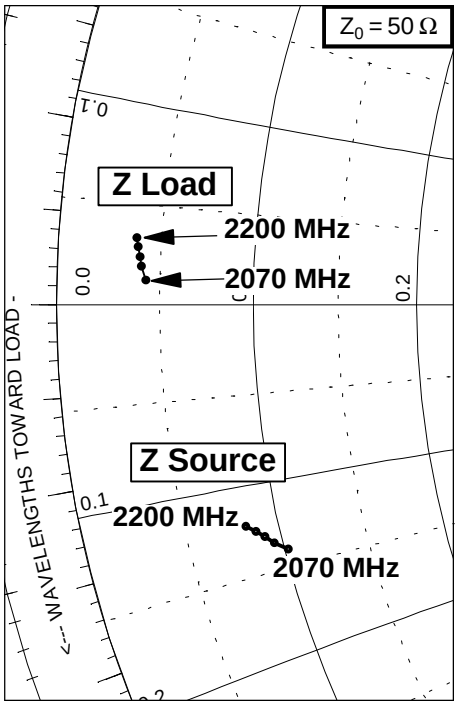
Typical Performance (cont.)





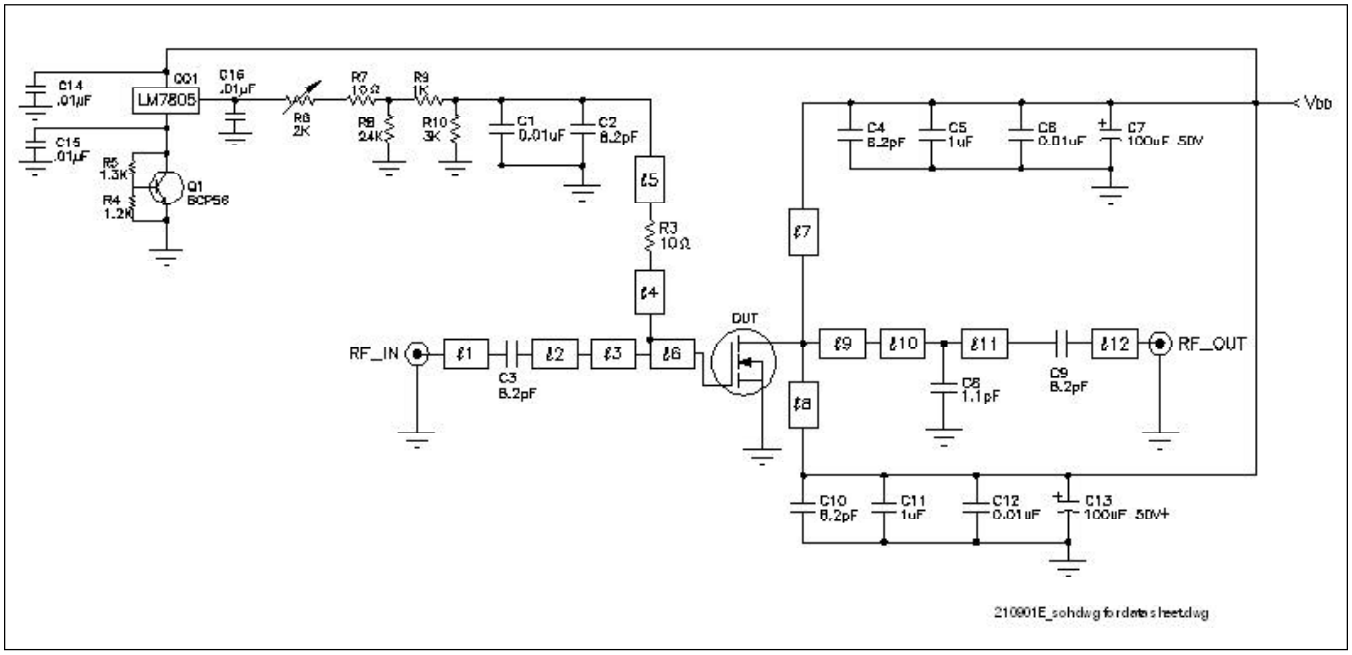
Broadband Circuit Impedance Data





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2070	5.11	–7.00	2.14	0.62
2110	4.78	–6.74	2.03	0.97
2140	4.57	–6.50	1.99	1.21
2170	4.35	–6.30	1.92	1.45
2200	4.12	–6.11	1.88	1.67

Test Circuit

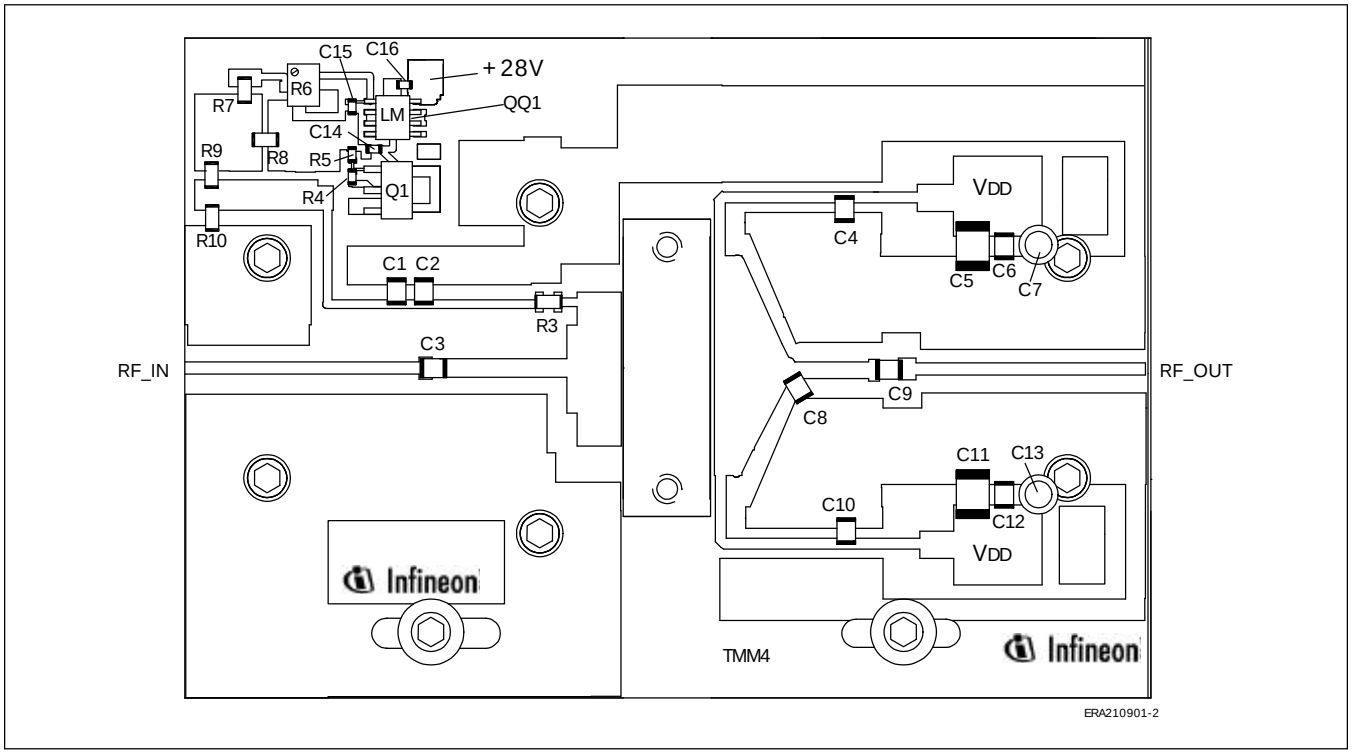


Reference Circuit Schematic for f = 2140 MHz

Circuit Information			
DUT	PTF210901E	LDMOS Transistor	
PCB	0.76 mm [0.030"] thick, ε_r = 4.5	2 oz. copper	TMM4

Microstrip	Value at 2140 MHz	Dimensions: L x W (mm.)	Dimensions: L x W (in.)
ℓ1	0.375 λ, 50 Ω	28.45 x 1.40	1.120 x 0.055
ℓ2	0.199 λ, 39.2 Ω	14.83 x 2.06	0.584 x 0.081
ℓ3	0.015 λ, 11.5 Ω	1.07 x 10.06	0.042 x 0.396
ℓ4	0.037 λ, 60.4 Ω	2.90 x 0.97	0.114 x 0.038
ℓ5	0.195 λ, 60.4 Ω	15.11 x 0.97	0.595 x 0.038
ℓ6	0.073 λ, 7.5 Ω	4.98 x 17.73	0.196 x 0.698
ℓ7, ℓ8	0.199 λ, 55.4 Ω	15.32 x 1.14	0.603 x 0.045
ℓ9	0.049 λ, 4.98 Ω	3.30 x 25.17	0.130 x 0.991
ℓ10	0.089 λ, 4.98 Ω	5.99 x 25.17	0.236 x 0.991
ℓ11	0.151 λ, 41.9 Ω	11.30 x 1.85	0.445 x 0.073
ℓ12	0.381 λ, 50 Ω	29.13 x 1.40	1.147 x 0.055

Test Circuit (cont.)



Reference Circuit[1] (not to scale)

Component	Description	Manufacturer	P/N or Comment
C1, C6, C12	Capacitor, 0.01 µF	Digi-Key	PCC1772CT-ND
C2, C3, C4, C9, C10	Capacitor, 8.2 pF	ATC	100B 8R2
C5, C11	Capacitor, 1 µF, ceramic, 50 V	ATC	920DC105KW100
C7, C13	Capacitor, 100 µF, 50 V, electrolytic	Digi-Key	P5182-ND
C8	Capacitor, 1.1 pF	ATC	100B OR6
C14, C15, C16	Capacitor, 0.01 µF	Digi-Key	PCC1772CT-ND
QQ1	Voltage regulator	Digi-Key	LM 7805
Q1	Transistor	Infineon	BCP56
R1, R2	Resistor, 12K ohm, 1/4 W, 1206	Digi-Key	P12KECT-ND
R3	Resistor, 10 ohm, 1/4 W, 1206	Digi-Key	P10ECT-ND
R4	Resistor, 1.2K ohm, 1/10 W, 0603	Digi-Key	P1.2KGCT-ND
R5	Resistor, 1.3K ohm, 1/10 W, 0603	Digi-Key	P1.3KGCT-ND
R6	Resistor, variable 2K ohm, 4 W	Digi-Key	3224 W-202ETR-ND
R7	Resistor, 10 ohm, 1/4 W, 1206	Digi-Key	P10ECT-ND
R8	Resistor, 24K ohm, 1/4 W, 1206	Digi-Key	P24KECT-ND
R9	Resistor, 1K ohm, 1/4 W, 1206	Digi-Key	P1.0KECT-ND
R10	Resistor, 3K ohm, 1/4 W, 1206	Digi-Key	P3.0KECT-ND

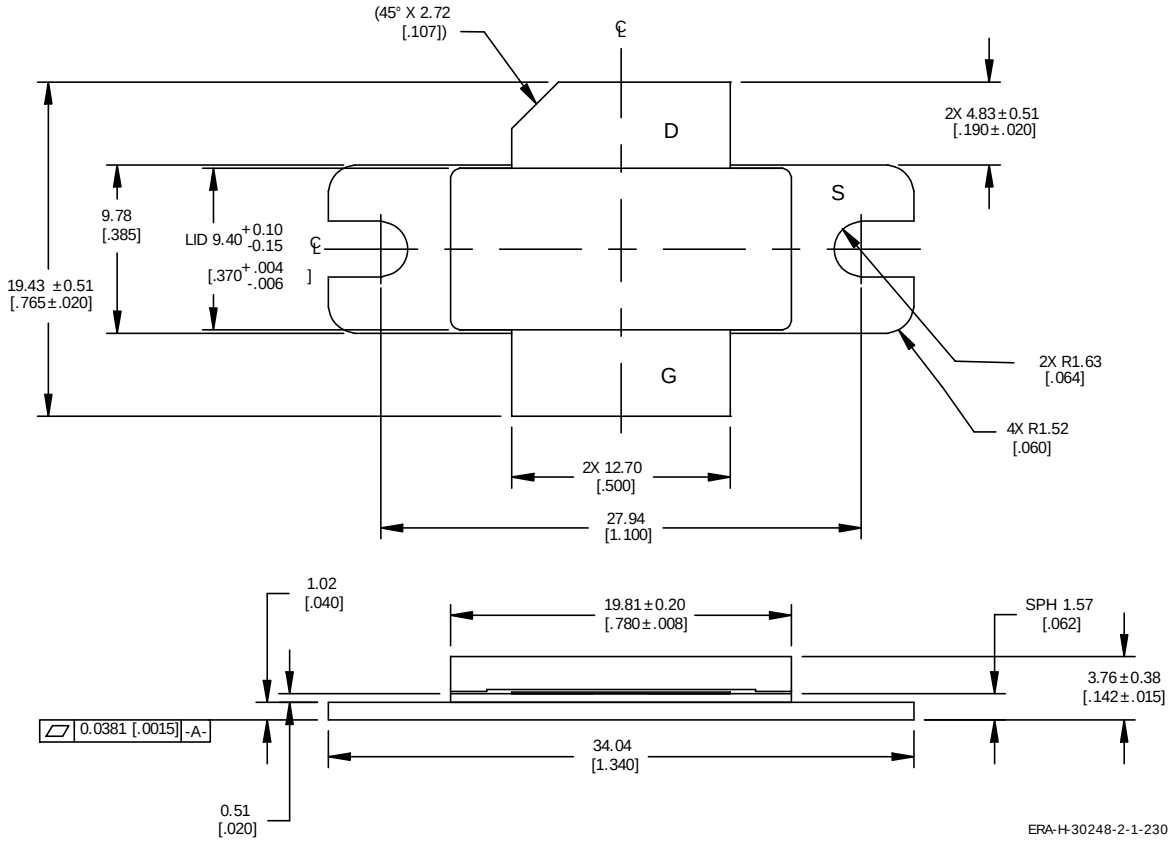
[1]Gerber Files for this circuit available on request.

Ordering Information

Type	Package Outline	Package Description	Marking
PTF210901E	30248	Thermally enhanced, with flange	PTF210901E

Package Outline Specifications

Package 30248



Notes: Unless otherwise specified

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. Pins: D = drain, S = source, G = gate
4. Lead thickness: 0.10± +0.051/–0.025 [.004 +.002/–.001]

Find the latest and most complete information about products and packaging at the Infineon Internet page http://www.infineon.com/products

PTF210901

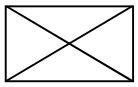
Revision History:	**2004-01-16**
Previous Version:	2003-12-22, Data Sheet
Page	Subjects (major changes since last revision)
5	Circuit schematic adjusted

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Edition 2004-01-16

Published by Infineon Technologies AG,
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